

SVX II Emulation Card

University of Michigan
Yimei Huang
July, 1999

1. Introduction

SVX II emulation card is designed to emulate the digital data transfer functions of SVX II chips. The chips work in four modes: initialization, acquisition, digitization and readout. The initialization mode is used at power up to serially load internal control registers and download a hit test pattern for diagnostic purpose. In the readout mode the digitized data is read out on an eight bit parallel bus. Because only these two modes have digital data transfer operations, the SVX II emulation board will provide emulation only on these two modes. Its functions and features are as follows:

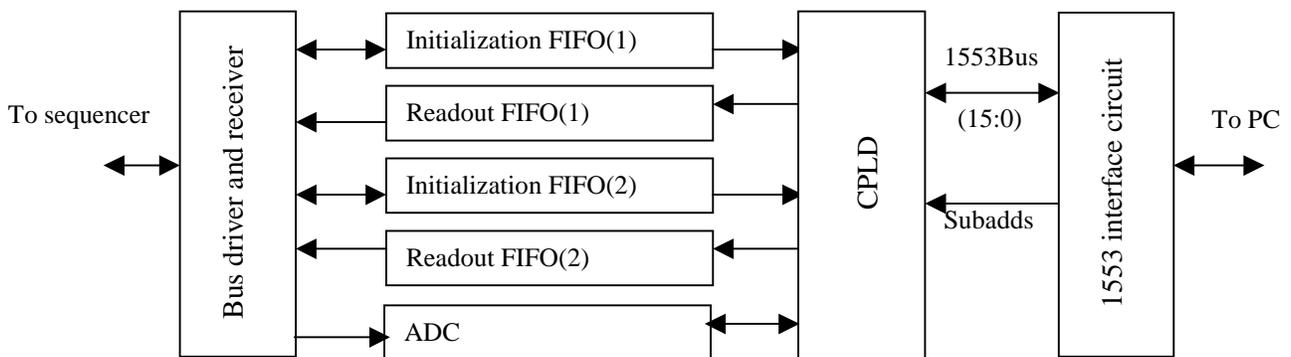
- Save programmable SVX II chip initialization bit streams from the sequencer, and read them out either back to sequencer or to the 1553 bus.
- Save fake or MC events through the 1553 bus, and then read them out to the sequencer.
- Do A/D conversion on power supplies to SVX II chips, and read out the results through 1553 bus.

2. Main functions and layout scheme

The card is made up of four blocks with identical circuit: A, B, C, and D. Each block has two pairs of initialize and readout FIFOs which emulate two strings of SVX II chips, an ADC chip which does A/D conversion on power supplies to each string, and a CPLD which generates all the control signals for its own block. Also each block has three kinds of connectors: 3M 50-pin connector, 3M 80-pin connector and the Hirose connector, so that it can be connected to the Low Mass cable as well as 3M cable, and can also talk to the interface card.

The card can either work as a whole, or can be cut and work as four little cards, each with the same functions. When working as little cards, each one has the 1553 circuit so that PC can access it. When working as a whole, only the 1553 circuit in block A is stuffed, and it controls the whole card.

SVX II Emulation Card Block Diagram (1/4 card unit)



3. 1553 registers

Each 1553 interface circuit has an Altera EPLD working in conjunction with a Harris HD6408 Manchester decoder and other associated circuit. One EPLD operates as two 1553 "RTs". Thirty active-low outputs (subad0_30 : subad0_1) for the first "RT" and thirty active-low outputs (subad1_30 : subad1_1) for the second "RT", each representing a subaddress, can be used as chip select lines. Sixteen parallel data bits are provided which performs basic reads and writes to 1553.

The following table defines the 1553 registers used by the emulation card.

<u>Subaddress</u>	<u>Function</u>
Subad0_a20	Select CPLD Register #1
Subad0_a21	Select CPLD Register #2
Subad0_a22	Read initialization FIFO(1) if Transmit = '1' Write readout FIFO(1) if Transmit = '0'
Subad0_a23	Read initialization FIFO(2) if Transmit = '1' Write readout FIFO(2) if Transmit = '0'

* Transmit = '1' signals that the card is transmitting data, and transmit = '0' signals that the card is receiving data. Subad0_1 to subad0_19 have been used by previous design.

When working as a whole card, subad0_a24 to subad0_a27 control the corresponding registers and FIFOs in block B, and so do subad1_a20 to subad1_a23 in block C, subad1_a27 to subad1_a30 in block D. All these subaddress lines come from 1553 circuit in the first quarter of the card, or block A. When working as little cards, only four subaddress lines per little card are used, which are subad0_20 to subad0_23.

The bits in CPLD register #1 and #2 in each ¼ card unit are defined as follows:

<i>Register #1</i>		
<u>Bit</u>	<u>Function</u>	
0 to 4	number of SVX II chips in first string	R/W
5	output mode select for initialization FIFO(1)	R/W
6 to 10	number of SVX II chips in second string	R/W
11	output mode select for initialization FIFO(2)	R/W
12 to 15	unused	

<i>Register #2</i>		
<u>Bit</u>	<u>Function</u>	
0 to 2	select one of eight channels of ADC	R/W
3	start ADC	R/W
4	Valid ADC result	RO
5 to 12	ADC result	RO
13	reset readout FIFO(1)	WO
14	reset readout FIFO(2)	WO
15	unused	

Bits 0 to 2 in register #2 correspond to the channel number of the ADC chip. They are assigned as

<u>Bits 2 to 0</u>	<u>signal</u>
000	AVDD2 for first string of SVX II chips
001	AVDD for first string of SVX II chips
010	DVDD for first string of SVX II chips
011	AVDD2 for second string of SVX II chips
100	AVDD for second string of SVX II chips
101	DVDD for second string of SVX II chips
110	grounded
111	grounded

4. Operation

1. Initialization mode

When the two mode lines from sequencer are declared as “00” at the falling edge of “chmode” signal, the string of SVX II chips is placed in initialization mode. Serial data start to be shifted into the initialize FIFO. Depending on the bits 0 to 4 or 6 to 10 in register #1, different length of the bit stream can be loaded. The bit 5 or 11 decides the output mode of the initialization FIFO.

For example, if the content of register #1 is “xxxx110000001001,” exactly 9×190 bits are serially shifted in from the sequencer before they are serially shifted back to sequencer for the first SVX II chip string. And exactly 16×190 bits are serially shifted in from the sequencer before they are ready to be parallel output to 1553 bus for the second string. The default value for bits 0 to 4 and 6 to 10 is 3, and the default for bits 5 and 11 is 0.

A write to register #1 will automatically reset both initialize FIFOs. Register #1 can only be written when modes are not declared as initialization mode. The operating sequence should be:

- Write register#1 through 1553 bus.
- Declare initialize mode.
- Load initialize FIFO with the bit stream coming from sequencer.
- After exact number of bits is shifted in, shift the same bit stream back to sequencer if bit 5(bit 11) in register#1 is set to ‘0’. Otherwise the initialize FIFO will be read out through 1553 bus if the subaddress line for that FIFO is at ‘0’ and transmit = ‘1’.

2. Readout mode

Before this mode is declared, both the readout FIFOs need to be downloaded with either fake data or MC data through 1553 bus. While the lower eight bits, bit 0 to 7, of the 1553 word are the data that will be send out to sequencer, bit 8 is used to signal the end of an event. Bit 8 of the last three 1553 words in each event need to be set to '1'. The depth of the FIFO is 4K. Because at most 258 bytes is readout for each SVX II chip (2 bytes per 128 channels and another two bytes for chip ID and status), at least 16 chip width data can be stored in each FIFO.

The data sent from the 1553 bus should have the structure as

<i>Bits 0 to 7</i>	<i>Bit 8</i>	<i>Bits 9 to 15</i>
<i>data</i>	<i>0</i>	<i>xxxxxx</i>
<i>data</i>	<i>0</i>	<i>xxxxxx</i>
<i>.</i>	<i>.</i>	<i>.</i>
<i>.</i>	<i>.</i>	<i>.</i>
<i>data</i>	<i>0</i>	<i>xxxxxx</i>
<i>data</i>	<i>1</i>	<i>xxxxxx</i>
<i>data</i>	<i>1</i>	<i>xxxxxx</i>
<i>data</i>	<i>1</i>	<i>xxxxxx (end of first event)</i>
<i>data</i>	<i>0</i>	<i>xxxxxx</i>
<i>data</i>	<i>0</i>	<i>xxxxxx</i>
<i>.</i>	<i>.</i>	<i>.</i>
<i>.</i>	<i>.</i>	<i>.</i>
<i>data</i>	<i>0</i>	<i>xxxxxx</i>
<i>data</i>	<i>1</i>	<i>xxxxxx</i>
<i>data</i>	<i>1</i>	<i>xxxxxx</i>
<i>data</i>	<i>1</i>	<i>xxxxxx (end of second event)</i>
<i>.</i>	<i>.</i>	<i>.</i>
<i>.</i>	<i>.</i>	<i>.</i>
<i>data</i>	<i>1</i>	<i>xxxxxx</i>
<i>data</i>	<i>1</i>	<i>xxxxxx</i>
<i>data</i>	<i>1</i>	<i>xxxxxx (end of nth event)</i>

When readout mode is declared, the data is sent out to the sequencer with DVALID signals. Readout will be disabled at the end of every event. To read the next event, the mode should be set to other modes, and then set back to readout mode again. Also the readout FIFO is retransmittable, which means the same data can be read and read again. A write of '1' to bit 13 or 14 in register #2 is needed to reset the readout FIFO before new events are downloaded. The operating sequence should be:

- Write '1' to bit 13 and bit 14 in register #2 through 1553 bus to reset both readout FIFOs.
- Load both readout FIFOs through 1553 bus.
- Declare readout mode.
- Output event stored in readout FIFO to sequencer. To read the next event, redeclare the readout mode again.
- Write '1' to bit 13 (bit 14) in register #2 before loading new data pattern to the readout FIFO.

3. ADC

Each $\frac{1}{4}$ card unit has an ADC that can do simple A/D conversions on AVDD, AVDD2, and DVDD for each channel. Because each $\frac{1}{4}$ card unit emulates two channels, six analog signals are sent to the ADC input. Bits 0 to 2 in register #2 select one of these six signals to do the A/D conversion. '1' in bit 3 tells the ADC to start A/D conversion. Once the conversion starts, this bit will be set back to '0', and bits 4 to 12 will be cleared. When the conversion is finished, the result will be put into bit 5 to 12 of register #2, and the bit 4 will be set to '1' at the same time. The operating sequence should be:

- Write bit 0 to 3 of register #2 through 1553 bus.
- Writing '1' to bit 3 of register #2 will start the A/D conversion, which in turn clears bit 3.
- Keep polling register #2 until bit4 changes from '0' to '1', which means the value at bits 5 to 12 is valid ADC result.
- Write bit 0 to 3 of register #2 again to start A/D conversion on another analog signal.