

STT Software Plan

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Outline

- Process Variables
- Comics
- Downloads
- Monitoring
- Versioning

Process Variables

- Define Process Variables (PVs)
 - Need Crate Memory Map
- Include Loading of EPICS on PowerPC
- Test EPICS' ability to access Pvs

- Time: 1.5 Weeks

Begin using Comics

- Use Comics to Download PVs
- Test Size Limitations
 - Use Comics to download large file (if possible)
 - Write VxWorks process to download large file
 - Time and Compare methods
 - Downloads to PPC memory
 - Downloads across VME
- Time: 2 weeks

Rare Downloads

- STT
 - LUT – Straight Forward Memory Transfer
- TFC
 - LUT and DSP Code – Pass through IDPM
- ALL
 - FPGA – Download through PCI to JTAG
- Time: Developed during Testing

Finalize Downloading

- Define Times to be Downloaded
- Define Order of Download
 - Rare Downloads
 - Common Downloads
 - Build Tree
 - Write Python Download code
- Time: 2 weeks at Integration

Monitoring

- Write GUIs to Display Monitoring Information
- Write VxWorks Monitoring Process
 - Begins on Collect Status Interrupt from FRC
 - Observes Protocols for Interacting with other Boards
- Time: 1st Pass End August

Versioning

- The Trigger database will contain an STT version
 - Based on all parts of STT
- Develop Python program to keep track of version
 - Store version information in pickle file
 - Name, version, location
 - Can be read in and individual versions checked at download
- Time: July

Simulator

- Silvia is on Vacation