

Report of implementation of the strip reader module in the  
APEX20K family using Quartus software  
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Table1: The report of the compilation of the strip\_reader module in Quartus.

Device name	EP20K300EBC652-1
Logic elements	2643/11520 (22%)
Pins	392/408 (96%)
Memory bits	49024 /147456 (33%)
ESBs	27/72 (38%)

Table 2: Comparison with the MAXPLUS-II simulation of the strip reader module.

Device name	EPF10K200EGC599-1
Logic elements	2042/9984 ( 20%)
Pins	420/464 (90%)
Memory bits	46976 (47 %)
EABs	16/24 ( 66%)

Thus from the above comparison we can find the approximate resources required for the whole design (Strip reader + Centroid Finder + Hit filter + L3 buffers)  
 This is with reference to the studies on fitting the design in three FLEX10KE chips

Table 3: Projected resources required for the electronics for one STC daughter card using APEX20K family

Device Family	Memory Bits	Logic cells	EABs
Total design in FLEX10KE	96,612	10,361	42
Projected resources required using APEX20KE	100,825	13,410	71



Table 4: The summary of resources available in the largest available FPLD in APEX20K family - EP20K1500E

Maximum system gates	2,392,000
Typical gates	1,500,000
Logic Elements	51,840
ESBs	216
Maximum RAM bits	442,368
Maximum macro-cells	3,456
Maximum user I/O pins	808

**According to the projected resources required three STC channels could fit in one EP20K1500E APEX20KE family FPLD.**



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