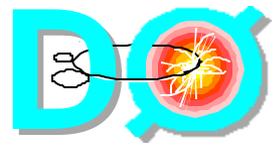


The FRC and the BC



**Georg Steinbrueck
Columbia University**

STT meeting 10/12/01



Timing problem prevented Qi and Tulika for 1.5 weeks to send more than one event from FRC->BC

Fixed as of yesterday!

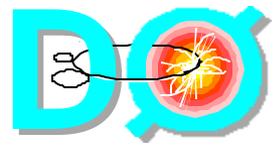
Able to send 16 events, only limited by buffer size

Some minor checks remain.

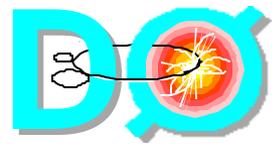
PUT_DONE/ GET_DONE (need second mb or just a wire to VCC/gnd in respective pins)

Some more tests with varying numbers of tracks.

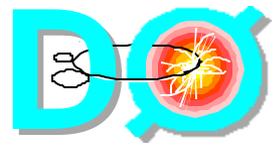
Then: Test another BC.



- **STT backplanes at hand. One is being installed in a crate as we speak.**
- **FRC and motherboard on the way from BU**
- **VBD by today**
- **Two SCL mezzanine cards at hand**
- **Bill has VTMs**
- **Have glink cable that can send fake CTT data (connected to sender)**
- **PC + Byteblaster (need to (re)install Max+PlusII**



- hints in email by Dan Edmunds
- plug in and test power
- Send SCL_ACK to tell SCLR to lock onto serial input data stream and to drop errors. This has to be done by the FRC on power up!
- Check if SCL_SYNCERROR dropped
- Will implement VME registers that can be written to/ read by CPU
- Latch one SCL word into VME register and read by CPU?
- Half test mode plans: Real SCL data and test CTT data
- Test SCL data and CTT data via VTM



Need BC for most tests.

Could do some tests without:

Have CPU write a word to VME register anywhere on FRC. Setup test register that sends SRDY when written to.

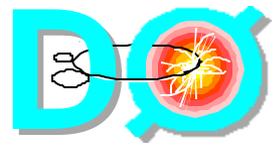
→ CPU initiated VBD read

Read back DONE (VBD->BM message)

Note: The VBD is a picky and stubborn beast.

Not well documented either!

Likely it will take a while to get this going, but can build on other peoples experience.



Some issues:

- r/o pointer list is NULL terminated -> addresses cannot be 0xppp`xx`0000
- WC and r/o pointer registers need to share the same most significant bits. VBD only checks lower bits for WC register.
- VBD does not care about data format.