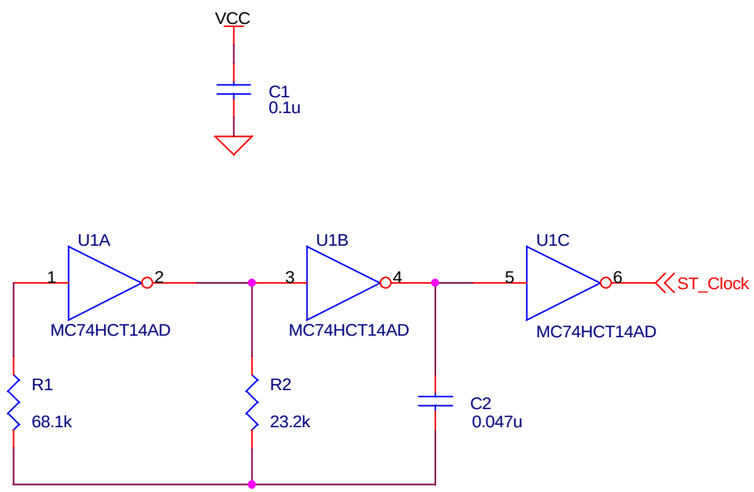

74HCT14 clock circuit was designed as suggested in the MOTOROLA High-Speed CMOS Data Book (pg. 2-26)

Electronics Design Laboratory

Tim J. Sobering
124 Burt Hall
Kansas State University
Manhattan, KS 66506-0400

Title: M011: State Machine Clock Generator

Size	Document Number:	REV
A	HEP008-M011	0.4

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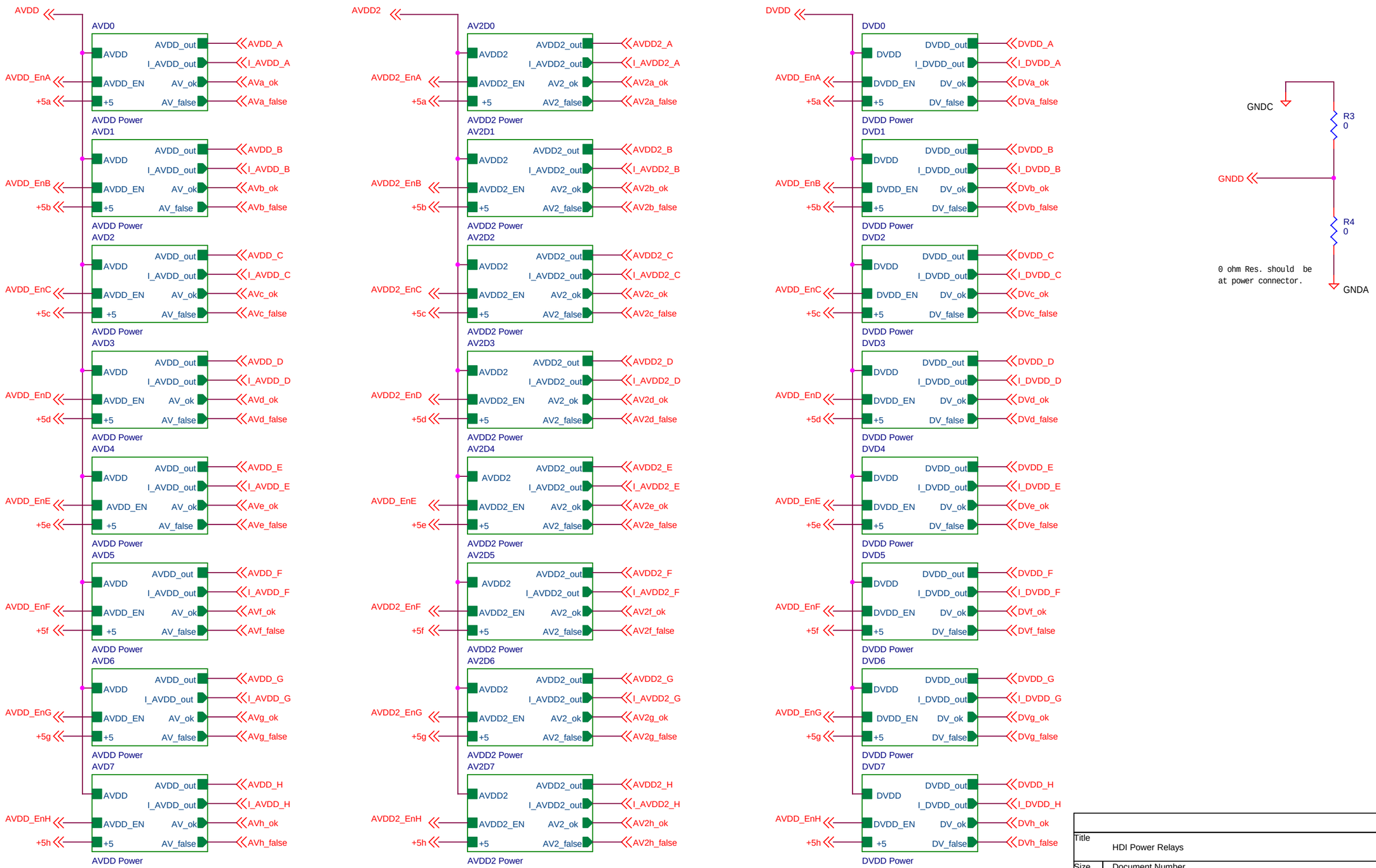
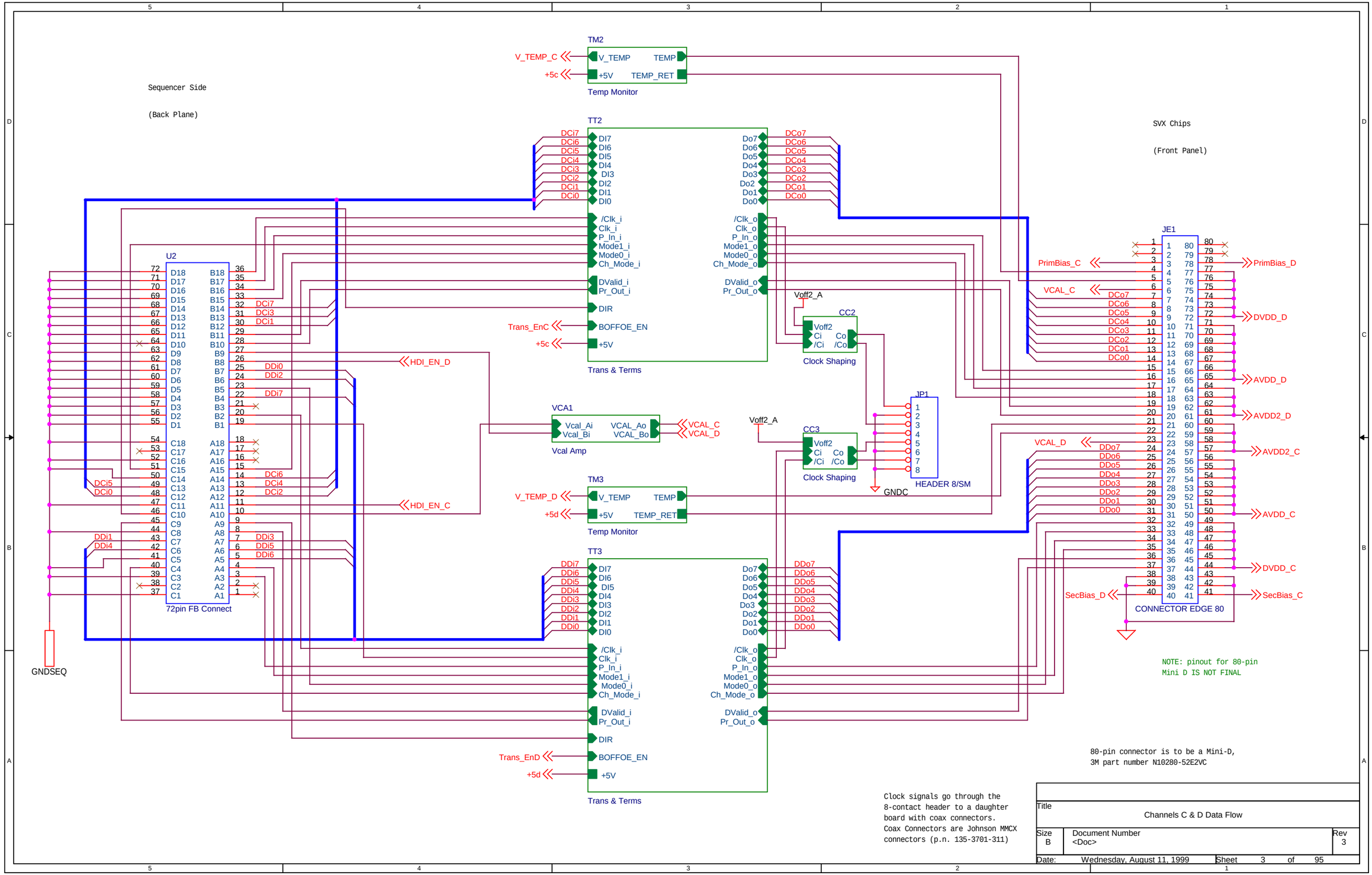
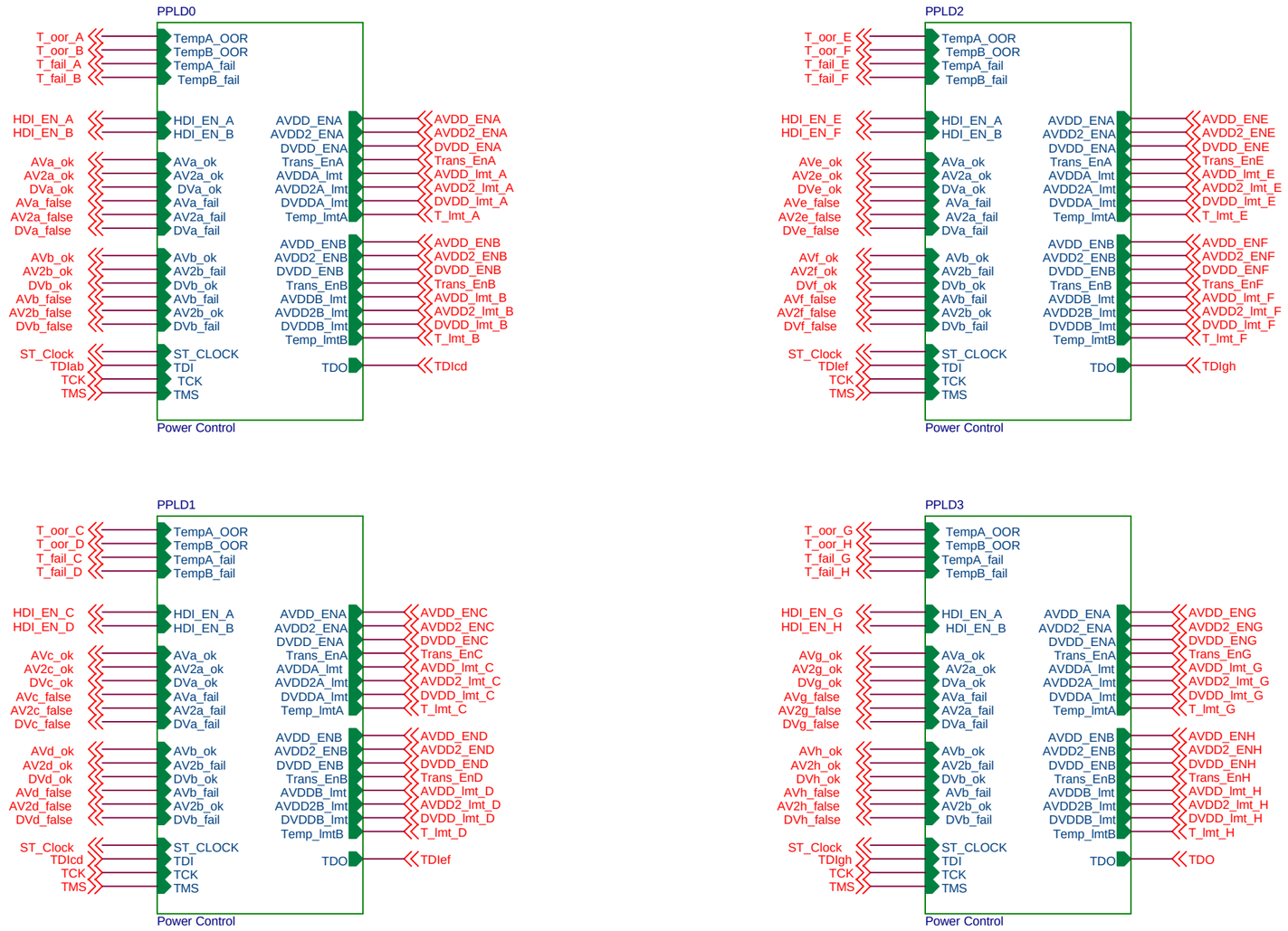
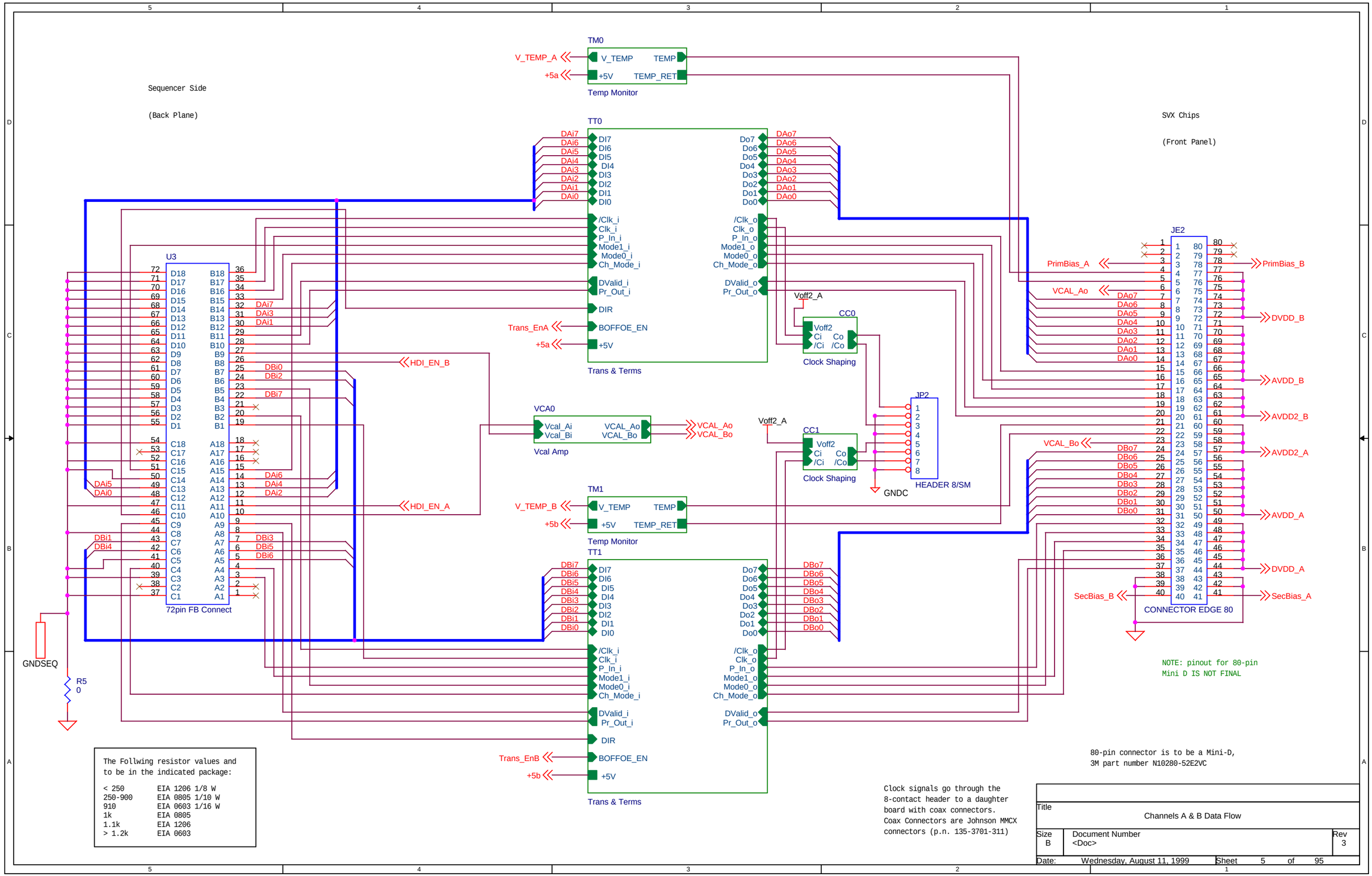


Title	HDI Power Relays	
Size B	Document Number <Doc>	Rev 3
Date: Wednesday, August 11, 1999	Sheet 2 of 95	


Sequencer Side
(Back Plane)
SVX Chips
(Front Panel)
TM2
V_TEMP_C
+5c
V_TEMP
TEMP
+5V
TEMP_RET
Temp Monitor
TT2
DCi7
DCi6
DCi5
DCi4
DCi3
DCi2
DCi1
DCi0
DI7
DI6
DI5
DI4
DI3
DI2
DI1
DI0
Do7
Do6
Do5
Do4
Do3
Do2
Do1
Do0
DCo7
DCo6
DCo5
DCo4
DCo3
DCo2
DCo1
DCo0
/Clk_i
Clk_i
P_In_i
Mode1_i
Mode0_i
Ch_Mode_i
DValid_i
Pr_Out_i
DIR
Trans_EnC
BOFFOE_EN
+5V
/Clk_o
Clk_o
P_In_o
Mode1_o
Mode0_o
Ch_Mode_o
DValid_o
Pr_Out_o
Trans & Terms
U2
72pin FB Connect
HDI_EN_D
HDI_EN_C
DDi0
DDi2
DDi7
DDi1
DDi4
DDi3
DDi5
DDi6
GNDSEQ
Voff2_A
CC2
Voff2
Ci
/Ci
Co
/Co
Clock Shaping
CC3
VCA1
Vcal_Ai
Vcal_Bi
VCAL_Ao
VCAL_Bo
VCAL_C
VCAL_D
Vcal Amp
JP1
HEADER 8/SM
GNDC
TM3
V_TEMP_D
+5d
TT3
Trans_EnD
JE1
PrimBias_C
PrimBias_D
VCAL_C
DVDD_D
AVDD_D
AVDD2_D
AVDD2_C
AVDD_C
DVDD_C
SecBias_D
SecBias_C
DDo7
DDo6
DDo5
DDo4
DDo3
DDo2
DDo1
DDo0
CONNECTOR EDGE 80
NOTE: pinout for 80-pin
Mini D IS NOT FINAL
80-pin connector is to be a Mini-D,
3M part number N10280-52E2VC
Clock signals go through the
8-contact header to a daughter
board with coax connectors.
Coax Connectors are Johnson MMCX
connectors (p.n. 135-3701-311)
Title
Channels C & D Data Flow
Size
B
Document Number
<Doc>
Rev
3
Date:
Wednesday, August 11, 1999
Sheet
3
of
95



Title	Power-On Control	
Size B	Document Number <Doc>	Rev 3
Date: Wednesday, August 11, 1999	Sheet 4 of 95	


Sequencer Side
(Back Plane)
SVX Chips
(Front Panel)
TM0
V_TEMP_A
+5a
V_TEMP
TEMP
+5V
TEMP_RET
Temp Monitor
TT0
DAi7
DAi6
DAi5
DAi4
DAi3
DAi2
DAi1
DAi0
DI7
DI6
DI5
DI4
DI3
DI2
DI1
DI0
Do7
Do6
Do5
Do4
Do3
Do2
Do1
Do0
DAo7
DAo6
DAo5
DAo4
DAo3
DAo2
DAo1
DAo0
/Clk_i
Clk_i
P_In_i
Mode1_i
Mode0_i
Ch_Mode_i
DValid_i
Pr_Out_i
DIR
Trans_EnA
BOFFOE_EN
+5V
/Clk_o
Clk_o
P_In_o
Mode1_o
Mode0_o
Ch_Mode_o
DValid_o
Pr_Out_o
Trans & Terms
U3
72pin FB Connect
HDI_EN_B
HDI_EN_A
DAi7
DAi3
DAi1
DBi0
DBi2
DBi7
DAi5
DAi0
DAi6
DAi4
DAi2
DBi1
DBi4
DBi3
DBi5
DBi6
GNDSEQ
R5
0
Voff2_A
CC0
Voff2
Ci
Co
/Ci
/Co
Clock Shaping
CC1
JP2
HEADER 8/SM
GNDC
VCA0
Vcal_Ai
Vcal_Bi
VCAL_Ao
VCAL_Bo
Vcal Amp
TM1
V_TEMP_B
+5b
TT1
Trans_EnB
JE2
PrimBias_A
VCAL_Ao
PrimBias_B
DVDD_B
AVDD_B
AVDD2_B
AVDD2_A
AVDD_A
DVDD_A
SecBias_B
SecBias_A
VCAL_Bo
DBo7
DBo6
DBo5
DBo4
DBo3
DBo2
DBo1
DBo0
CONNECTOR EDGE 80
NOTE: pinout for 80-pin
Mini D IS NOT FINAL
80-pin connector is to be a Mini-D,
3M part number N10280-52E2VC
The Follwing resistor values and
to be in the indicated package:
< 250 EIA 1206 1/8 W
250-900 EIA 0805 1/10 W
910 EIA 0603 1/16 W
1k EIA 0805
1.1k EIA 1206
> 1.2k EIA 0603
Clock signals go through the
8-contact header to a daughter
board with coax connectors.
Coax Connectors are Johnson MMCX
connectors (p.n. 135-3701-311)
Title
Channels A & B Data Flow
Size
B
Document Number
<Doc>
Rev
3
Date: Wednesday, August 11, 1999
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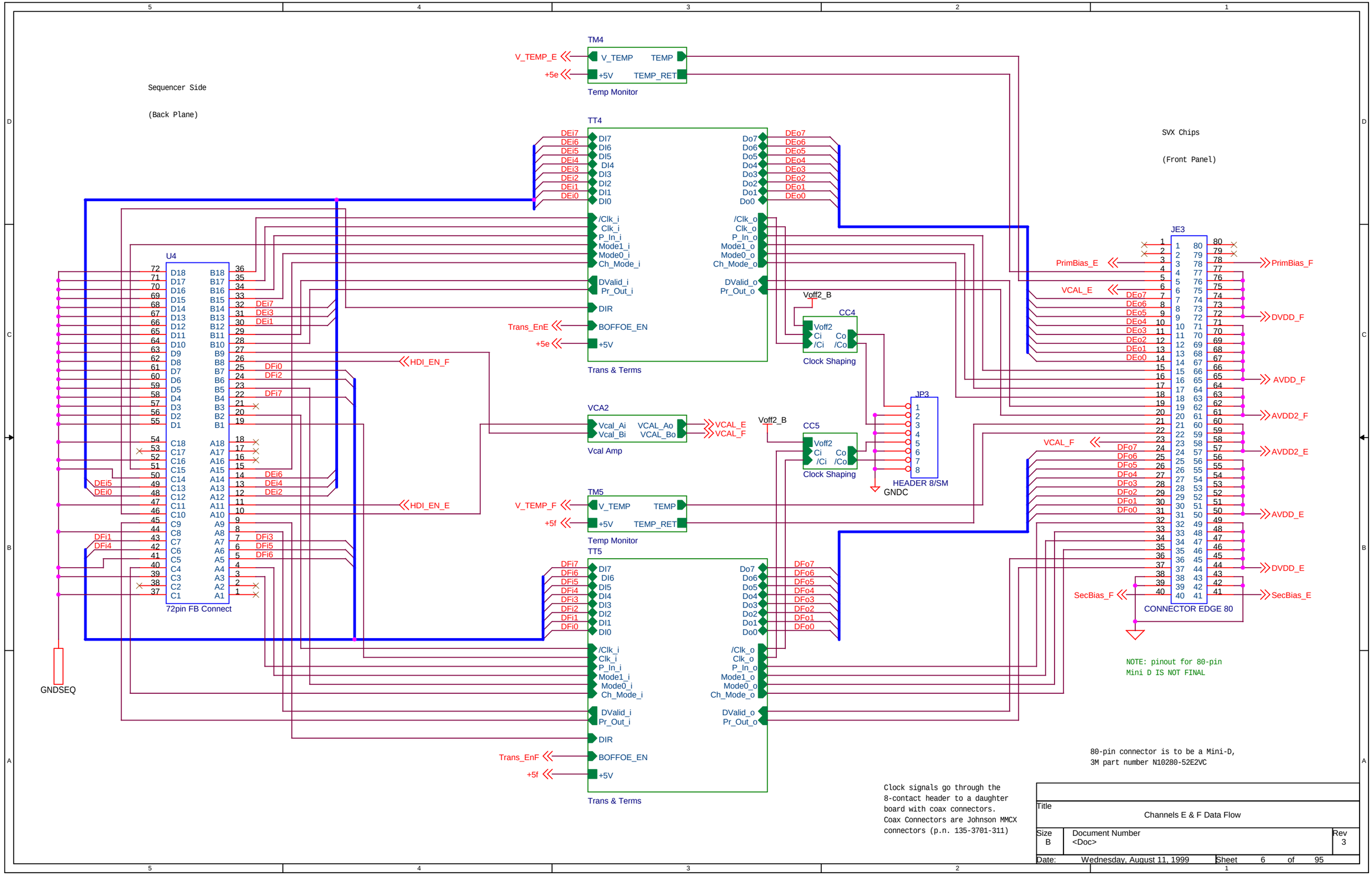
Sequencer Side
(Back Plane)
SVX Chips
(Front Panel)
TM4
V_TEMP_E
+5e
V_TEMP
TEMP
+5V
TEMP_RET
Temp Monitor
TT4
DEi7
DEi6
DEi5
DEi4
DEi3
DEi2
DEi1
DEi0
DI7
DI6
DI5
DI4
DI3
DI2
DI1
DI0
Do7
Do6
Do5
Do4
Do3
Do2
Do1
Do0
DEo7
DEo6
DEo5
DEo4
DEo3
DEo2
DEo1
DEo0
/Clk_i
Clk_i
P_In_i
Mode1_i
Mode0_i
Ch_Mode_i
DValid_i
Pr_Out_i
DIR
Trans_EnE
BOFFOE_EN
+5V
/Clk_o
Clk_o
P_In_o
Mode1_o
Mode0_o
Ch_Mode_o
DValid_o
Pr_Out_o
Trans & Terms
U4
72pin FB Connect
HDI_EN_F
HDI_EN_E
DEi7
DEi3
DEi1
DFi0
DFi2
DFi7
DEi6
DEi4
DEi2
DEi5
DEi0
DFi1
DFi4
DFi3
DFi5
DFi6
GNDSEQ
VCA2
Vcal_Ai
Vcal_Bi
VCAL_Ao
VCAL_Bo
VCAL_E
VCAL_F
Vcal Amp
Voff2_B
CC4
CC5
Voff2
Ci
/Ci
Co
/Co
Clock Shaping
JP3
HEADER 8/SM
GNDC
TM5
V_TEMP_F
+5f
TT5
Trans_EnF
JE3
PrimBias_E
PrimBias_F
DVDD_F
AVDD_F
AVDD2_F
AVDD2_E
AVDD_E
DVDD_E
SecBias_F
SecBias_E
DFo7
DFo6
DFo5
DFo4
DFo3
DFo2
DFo1
DFo0
CONNECTOR EDGE 80
NOTE: pinout for 80-pin
Mini D IS NOT FINAL
80-pin connector is to be a Mini-D,
3M part number N10280-52E2VC
Clock signals go through the
8-contact header to a daughter
board with coax connectors.
Coax Connectors are Johnson MMCX
connectors (p.n. 135-3701-311)
Title
Channels E & F Data Flow
Size
B
Document Number
<Doc>
Rev
3
Date:
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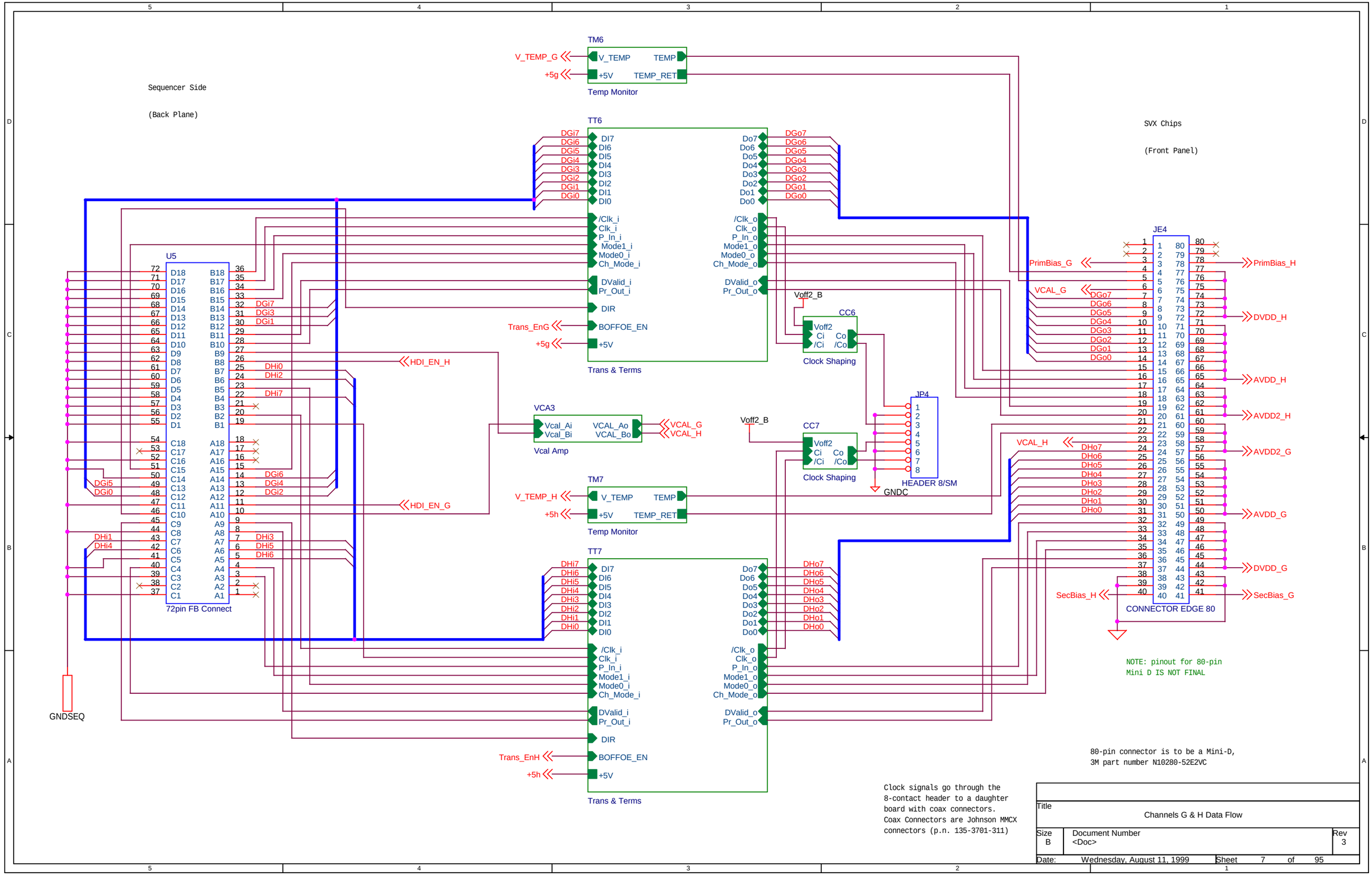
95


Sequencer Side
(Back Plane)
SVX Chips
(Front Panel)
TM6
V_TEMP_G
+5g
V_TEMP
TEMP
+5V
TEMP_RET
Temp Monitor
TT6
DGi7
DGi6
DGi5
DGi4
DGi3
DGi2
DGi1
DGi0
DI7
DI6
DI5
DI4
DI3
DI2
DI1
DI0
Do7
Do6
Do5
Do4
Do3
Do2
Do1
Do0
DGo7
DGo6
DGo5
DGo4
DGo3
DGo2
DGo1
DGo0
/Clk_i
Clk_i
P_In_i
Mode1_i
Mode0_i
Ch_Mode_i
DValid_i
Pr_Out_i
DIR
Trans_EnG
BOFFOE_EN
+5g
+5V
/Clk_o
Clk_o
P_In_o
Mode1_o
Mode0_o
Ch_Mode_o
DValid_o
Pr_Out_o
Trans & Terms
U5
72pin FB Connect
HDI_EN_H
HDI_EN_G
DGi7
DGi3
DGi1
DHi0
DHi2
DHi7
DGi6
DGi4
DGi2
DGi5
DGi0
DHi1
DHi4
DHi3
DHi5
DHi6
GNDSEQ
Voff2_B
CC6
Voff2
Ci
/Ci
Co
/Co
Clock Shaping
CC7
JP4
HEADER 8/SM
GNDC
VCA3
Vcal_Ai
Vcal_Bi
VCAL_Ao
VCAL_Bo
VCAL_G
VCAL_H
Vcal Amp
TM7
V_TEMP_H
+5h
Temp Monitor
TT7
DHi7
DHi6
DHi5
DHi4
DHi3
DHi2
DHi1
DHi0
DHo7
DHo6
DHo5
DHo4
DHo3
DHo2
DHo1
DHo0
Trans_EnH
JE4
PrimBias_G
PrimBias_H
VCAL_G
DVDD_H
AVDD_H
AVDD2_H
AVDD2_G
AVDD_G
DVDD_G
SecBias_H
SecBias_G
CONNECTOR EDGE 80
NOTE: pinout for 80-pin
Mini D IS NOT FINAL
80-pin connector is to be a Mini-D,
3M part number N10280-52E2VC
Clock signals go through the
8-contact header to a daughter
board with coax connectors.
Coax Connectors are Johnson MMCX
connectors (p.n. 135-3701-311)
Title
Channels G & H Data Flow
Size
B
Document Number
<Doc>
Rev
3
Date: Wednesday, August 11, 1999
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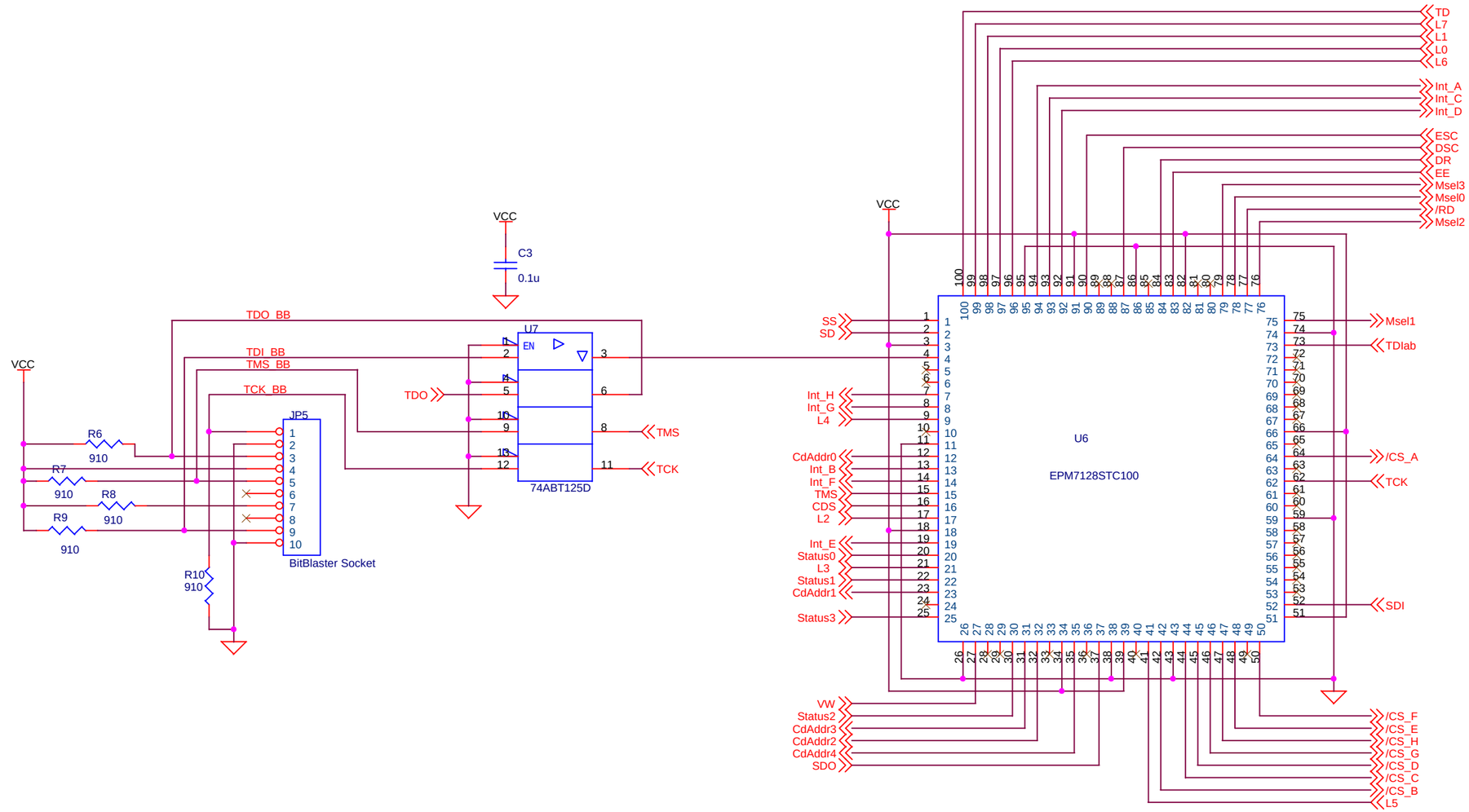
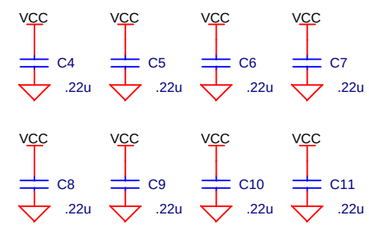
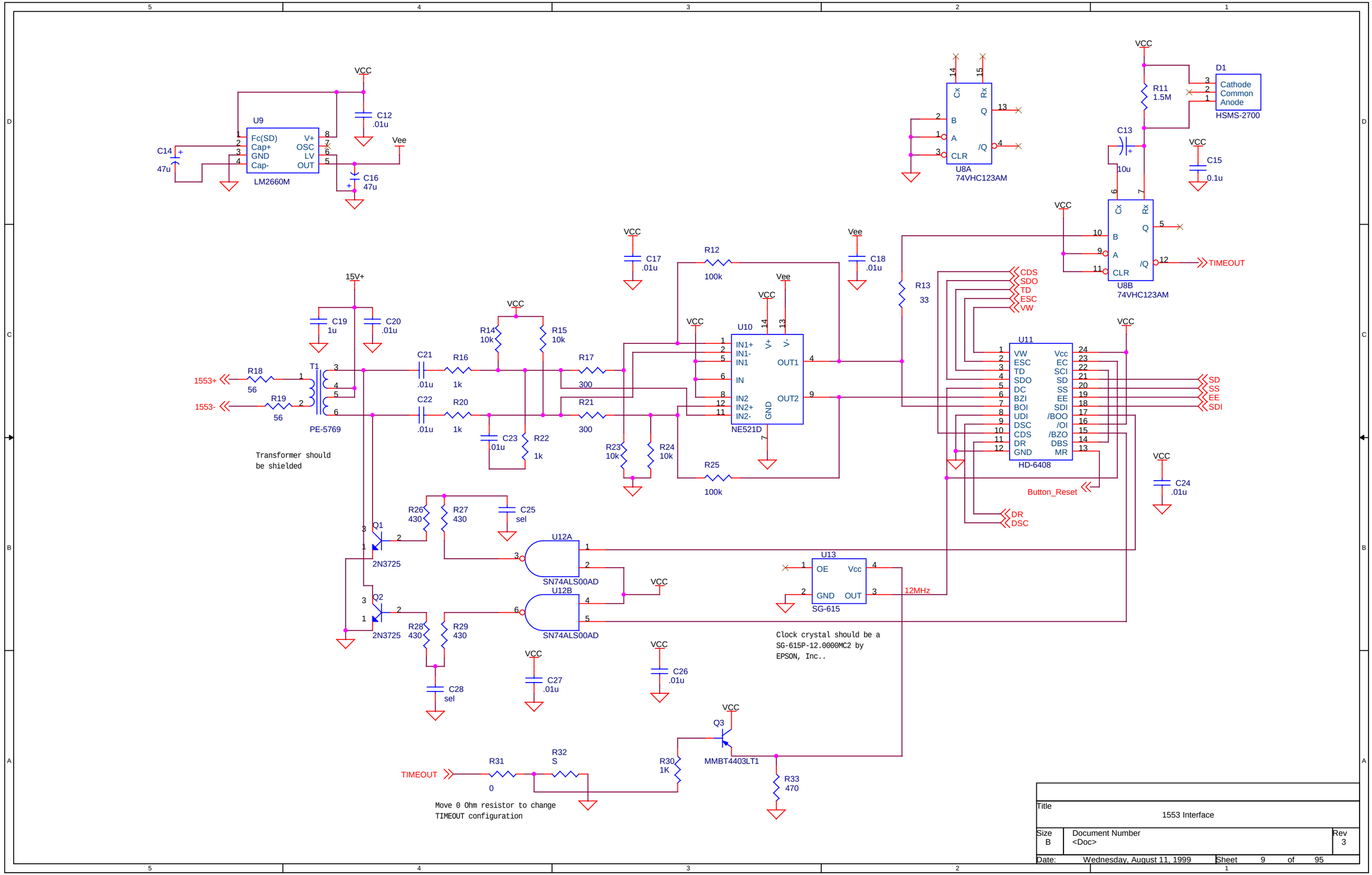


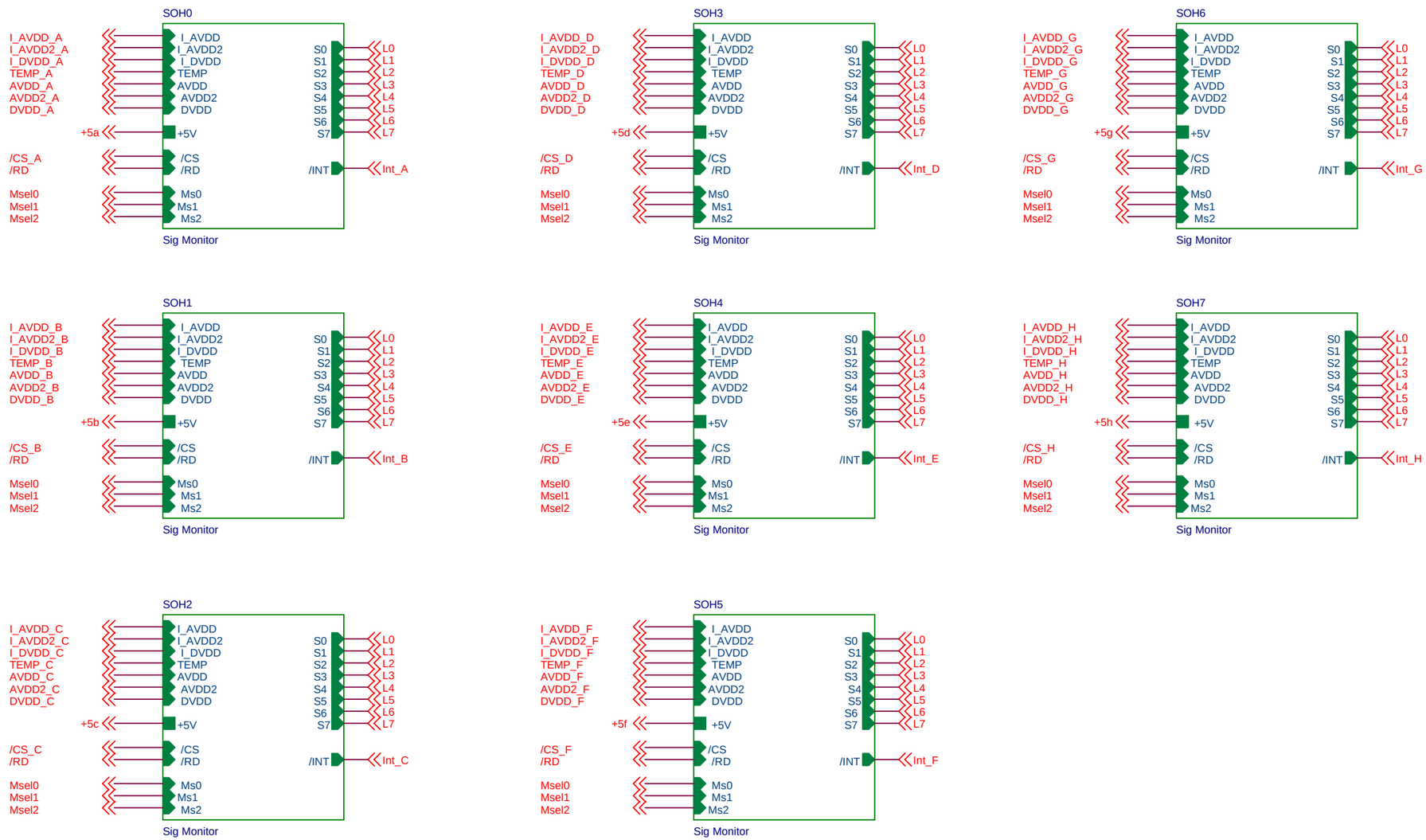


Capacitors should be located near the Vcc pins of the Altera chip (pins 3, 18, 34, 39, 51, 66, 82, and 91).

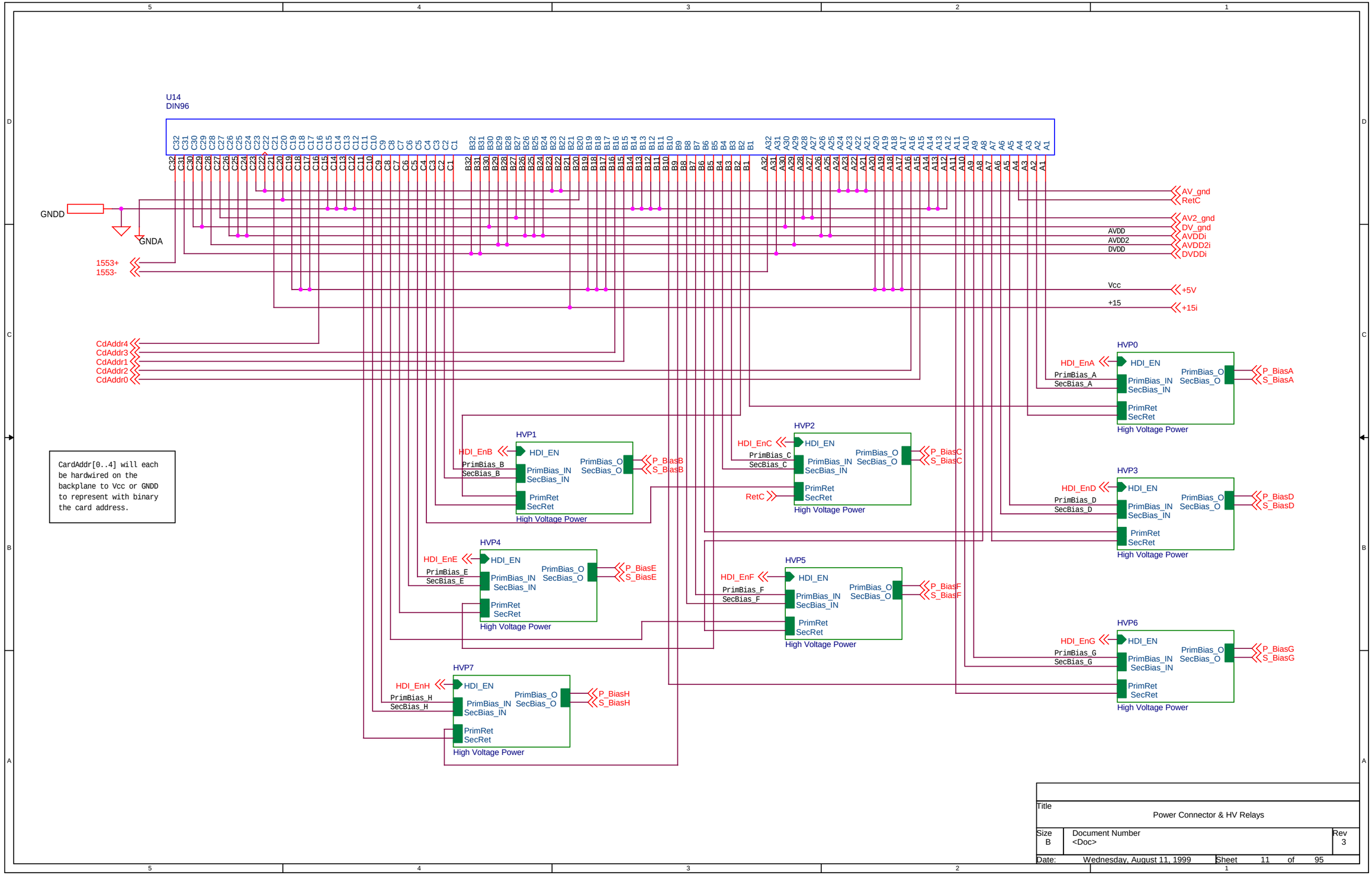
Title	1553 Altera Chip	
Size B	Document Number <Doc>	Rev 3
Date: Wednesday, August 11, 1999	Sheet 8 of 95	



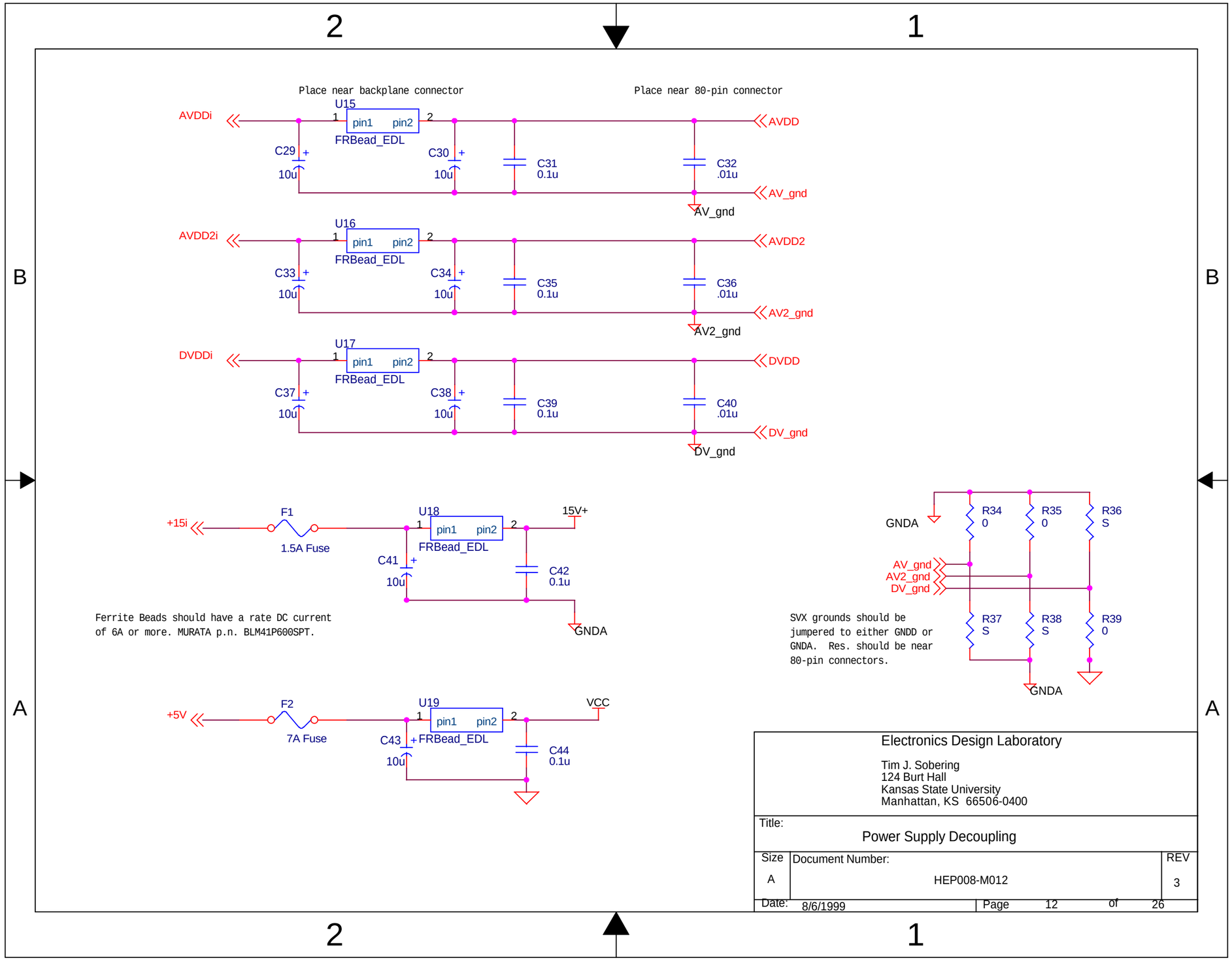
Title	1553 Interface	
Size B	Document Number <Doc>	Rev 3
Date: Wednesday, August 11, 1999	Sheet 9 of 95	



Title	State of Health A/D Circuitry	
Size B	Document Number <Doc>	Rev 3
Date: Wednesday, August 11, 1999	Sheet 10 of 95	



Title	Power Connector & HV Relays	
Size B	Document Number <Doc>	Rev 3
Date: Wednesday, August 11, 1999	Sheet 11 of 95	



Electronics Design Laboratory

Tim J. Sobering
124 Burt Hall
Kansas State University
Manhattan, KS 66506-0400

Title: Power Supply Decoupling

Size	Document Number:	REV
A	HEP008-M012	3

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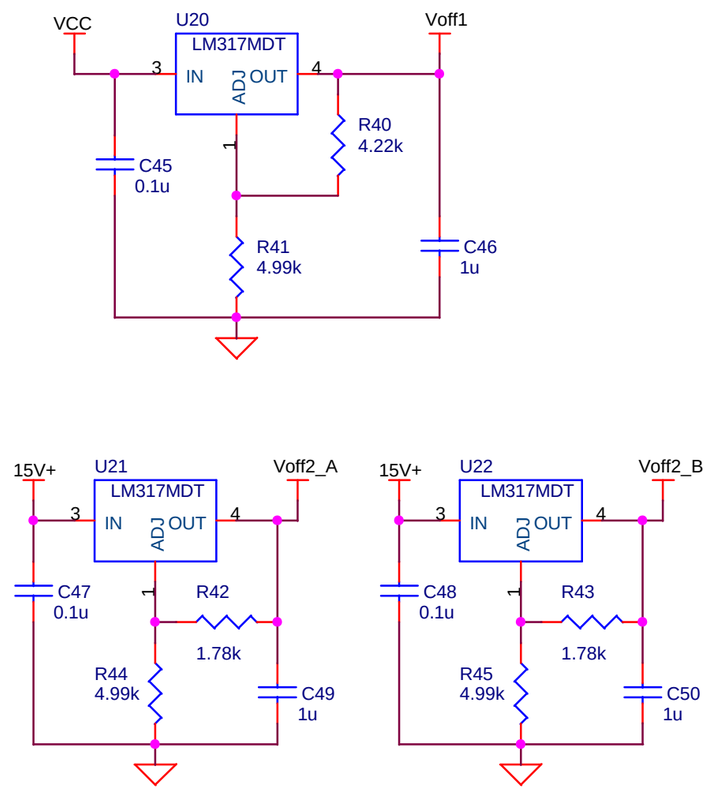
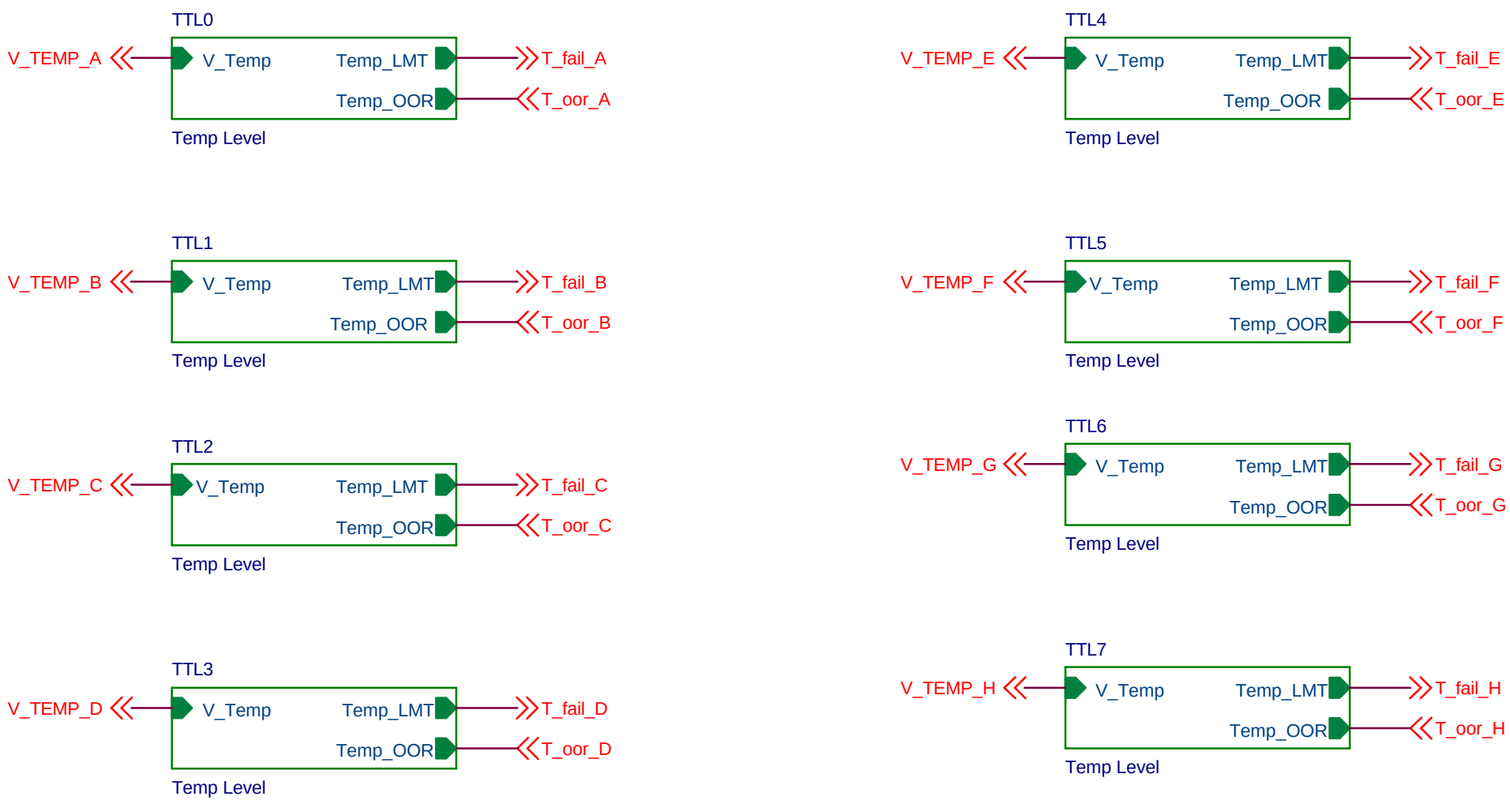
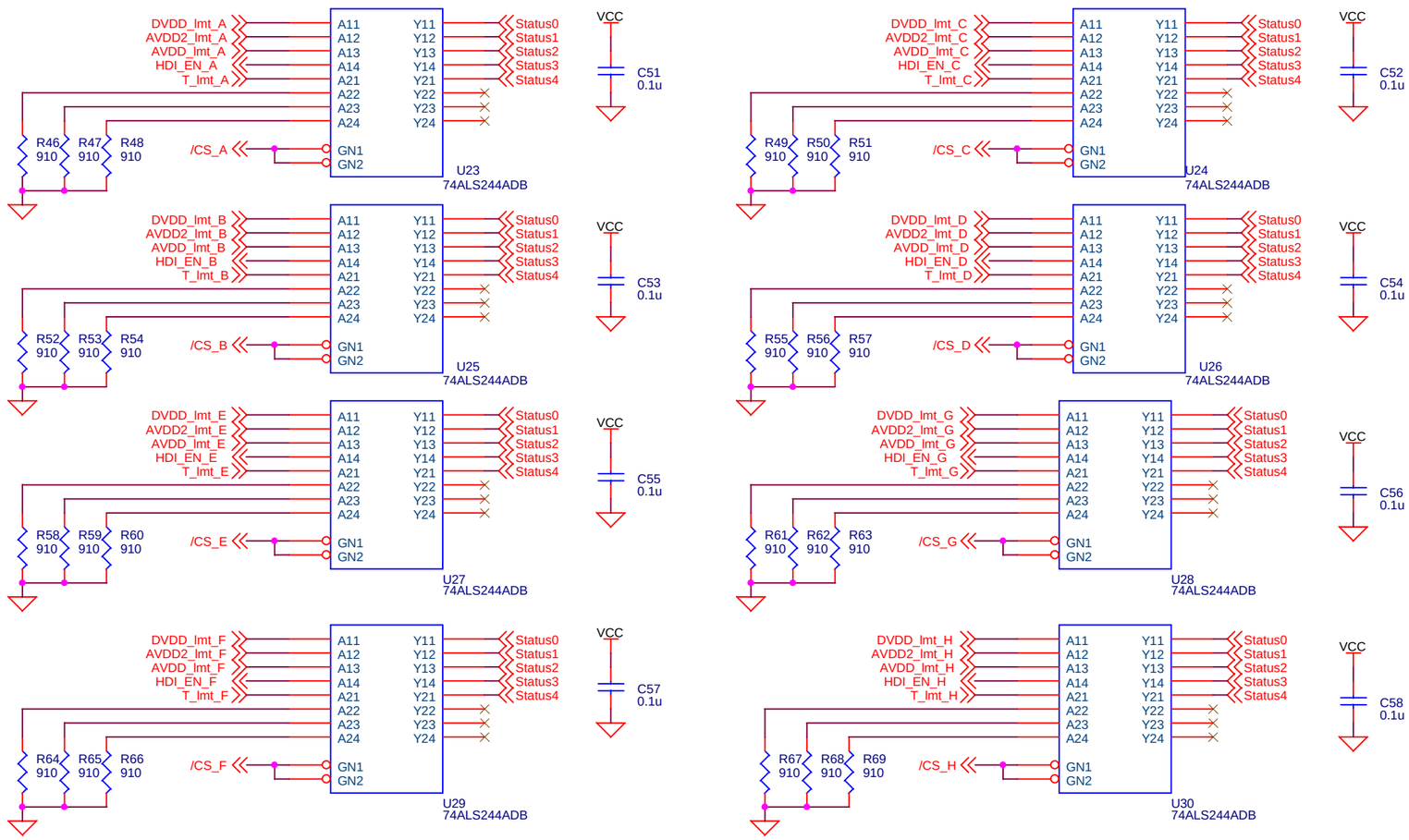


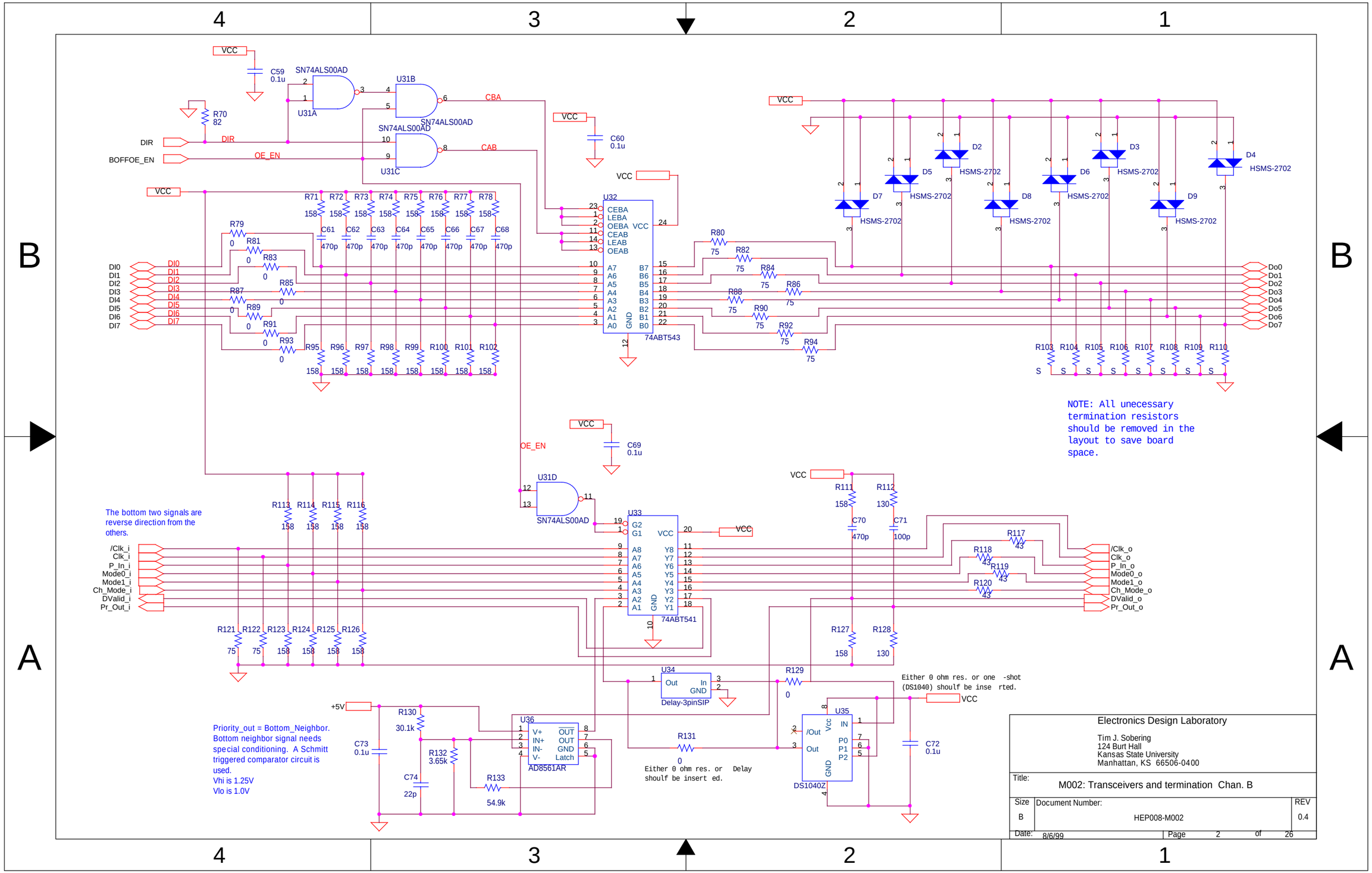
Title	Reference Voltages	
Size A	Document Number <Doc>	Rev 3
Date: Wednesday, August 11, 1999	Sheet 13 of 95	



Title	Temperature Level Trip Circuitry	
Size A	Document Number <Doc>	Rev 3
Date: Wednesday, August 11, 1999	Sheet 14 of 95	



Title	Status Bit Channel Selection	
Size B	Document Number <Doc>	Rev 4
Date: Wednesday, August 11, 1999	Sheet 15 of 95	


VCC
C59 0.1u
SN74ALS00AD
U31A
U31B
U31C
U31D
R70 82
DIR
BOFFOE_EN
OE_EN
CBA
CAB
C60 0.1u
C69 0.1u
U32
74ABT543
U33
74ABT541
U34
Delay-3pinSIP
U35
DS1040Z
U36
AD8561AR
HSMS-2702
D2
D3
D4
D5
D6
D7
D8
D9
DI0
DI1
DI2
DI3
DI4
DI5
DI6
DI7
Do0
Do1
Do2
Do3
Do4
Do5
Do6
Do7
/Clk_i
Clk_i
P_In_i
Mode0_i
Mode1_i
Ch_Mode_i
DValid_i
Pr_Out_i
/Clk_o
Clk_o
P_In_o
Mode0_o
Mode1_o
Ch_Mode_o
DValid_o
Pr_Out_o
NOTE: All unecessary termination resistors should be removed in the layout to save board space.
The bottom two signals are reverse direction from the others.
Priority_out = Bottom_Neighbor. Bottom neighbor signal needs special conditioning. A Schmitt triggered comparator circuit is used.
Vhi is 1.25V
Vlo is 1.0V
+5V
Either 0 ohm res. or one -shot (DS1040) shoulf be inse rted.
Either 0 ohm res. or Delay shoulf be insert ed.
Electronics Design Laboratory
Tim J. Sobering
124 Burt Hall
Kansas State University
Manhattan, KS 66506-0400
Title:
M002: Transceivers and termination Chan. B
Size
B
Document Number:
HEP008-M002
REV
0.4
Date: 8/6/99
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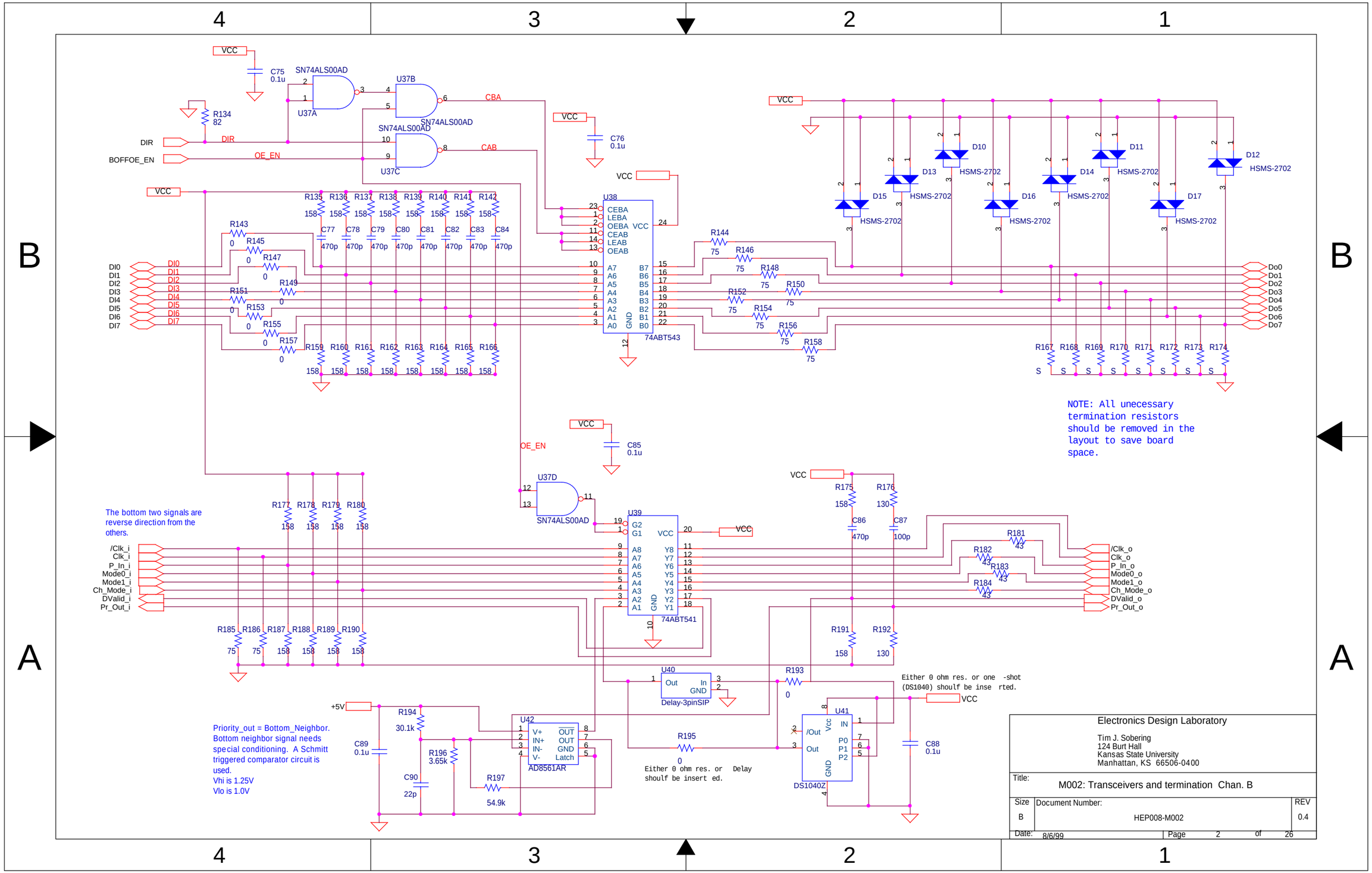
VCC
C75 0.1u
SN74ALS00AD
U37A
U37B
U37C
U37D
CBA
CAB
R134 82
DIR
BOFFOE_EN
OE_EN
C76 0.1u
C85 0.1u
U38
74ABT543
U39
74ABT541
U40
Delay-3pinSIP
U41
DS1040Z
U42
AD8561AR
D10
D11
D12
D13
D14
D15
D16
D17
HSMS-2702
DI0
DI1
DI2
DI3
DI4
DI5
DI6
DI7
Do0
Do1
Do2
Do3
Do4
Do5
Do6
Do7
/Clk_i
Clk_i
P_In_i
Mode0_i
Mode1_i
Ch_Mode_i
DValid_i
Pr_Out_i
/Clk_o
Clk_o
P_In_o
Mode0_o
Mode1_o
Ch_Mode_o
DValid_o
Pr_Out_o
NOTE: All unecessary termination resistors should be removed in the layout to save board space.
The bottom two signals are reverse direction from the others.
Priority_out = Bottom_Neighbor. Bottom neighbor signal needs special conditioning. A Schmitt triggered comparator circuit is used.
Vhi is 1.25V
Vlo is 1.0V
+5V
Either 0 ohm res. or one -shot (DS1040) shoulf be inse rted.
Either 0 ohm res. or Delay shoulf be insert ed.
Electronics Design Laboratory
Tim J. Sobering
124 Burt Hall
Kansas State University
Manhattan, KS 66506-0400
Title:
M002: Transceivers and termination Chan. B
Size
B
Document Number:
HEP008-M002
REV
0.4
Date: 8/6/99
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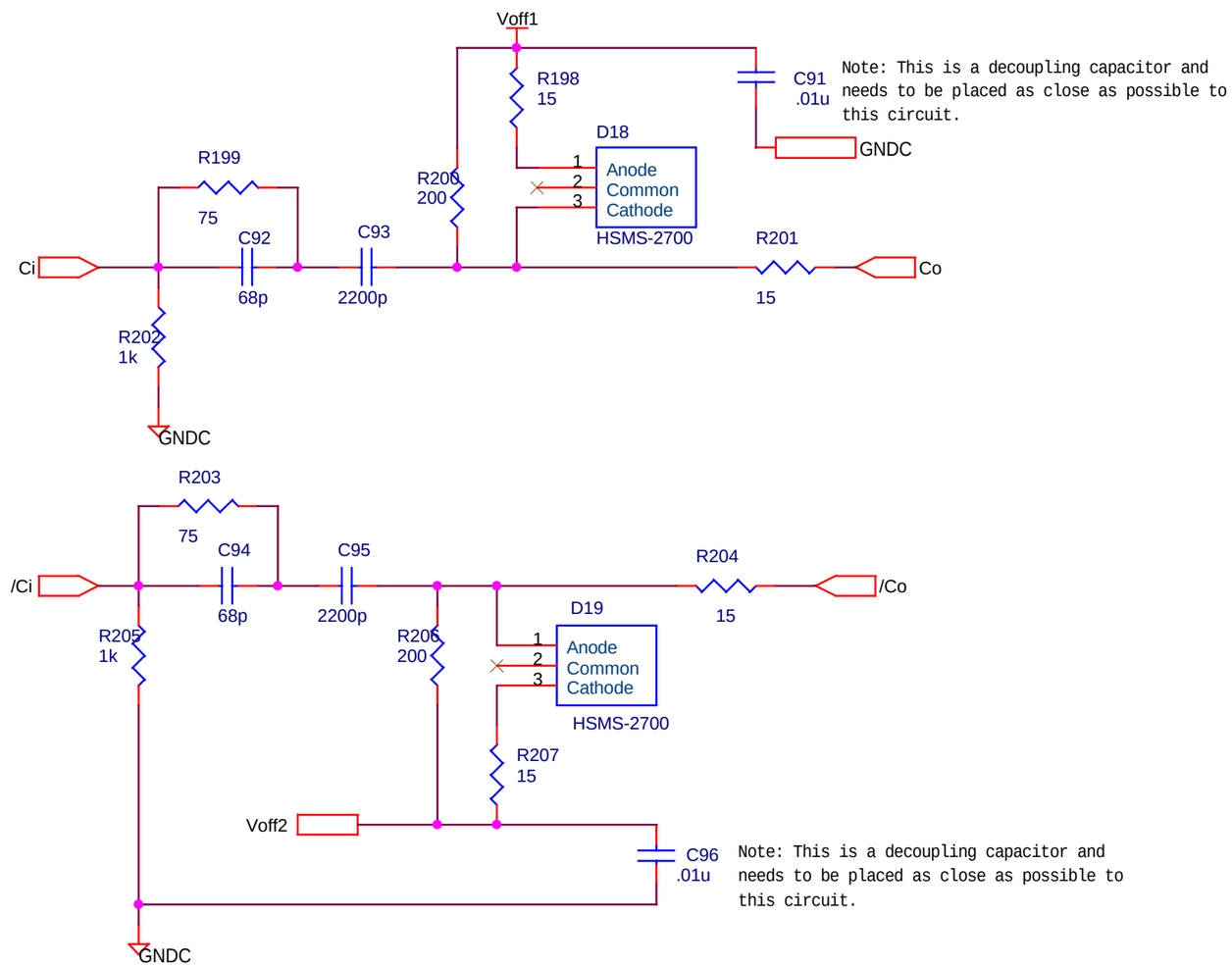
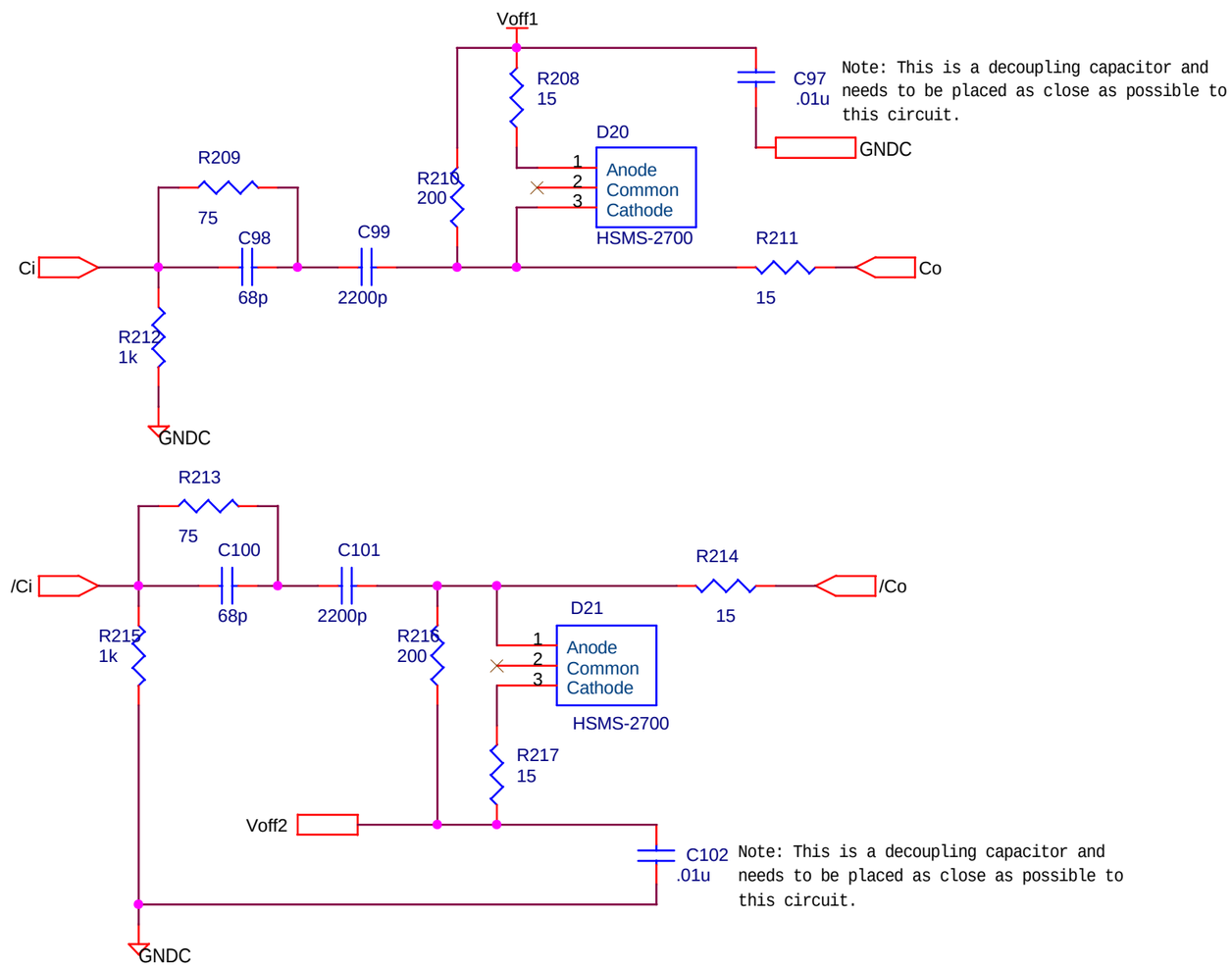
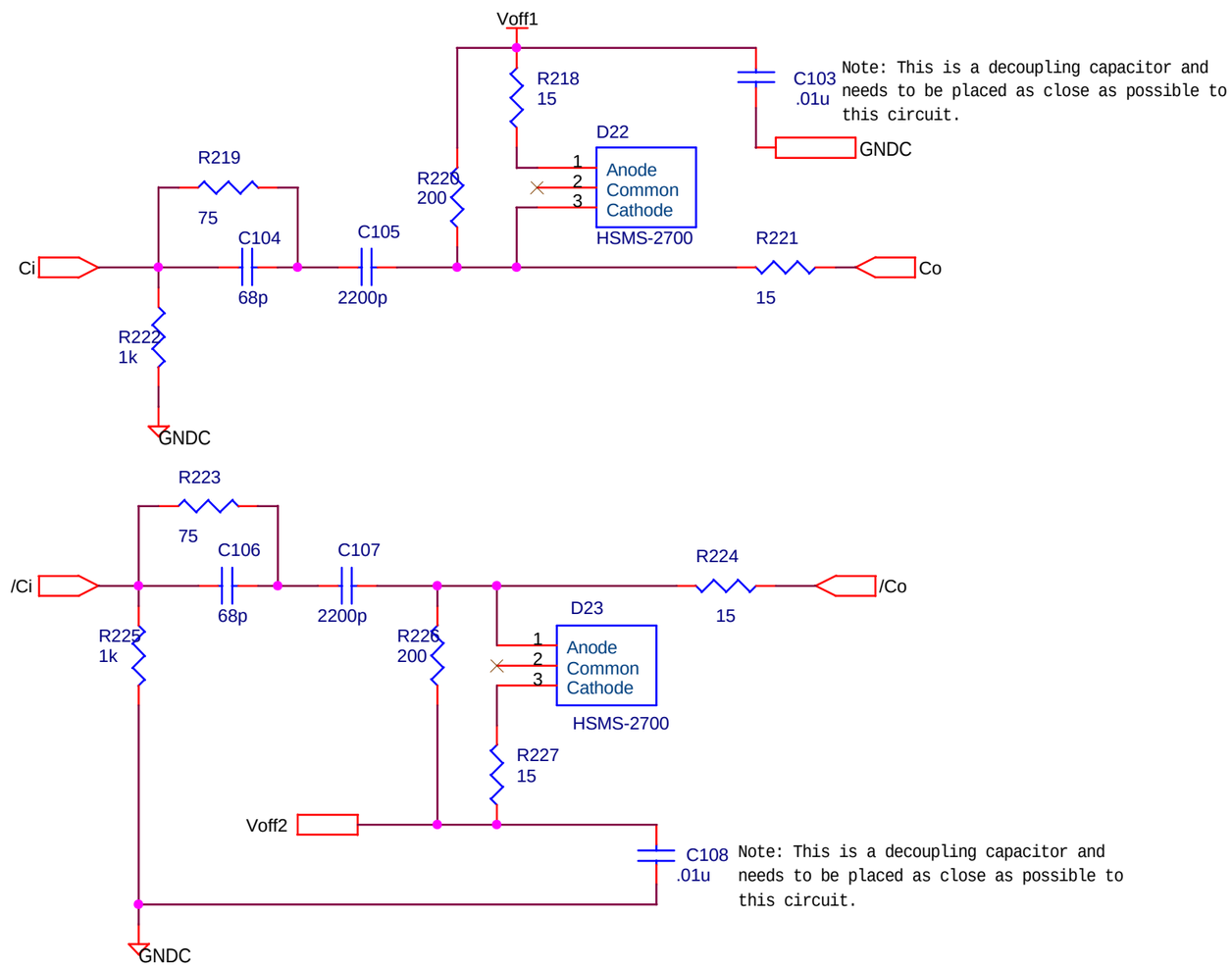


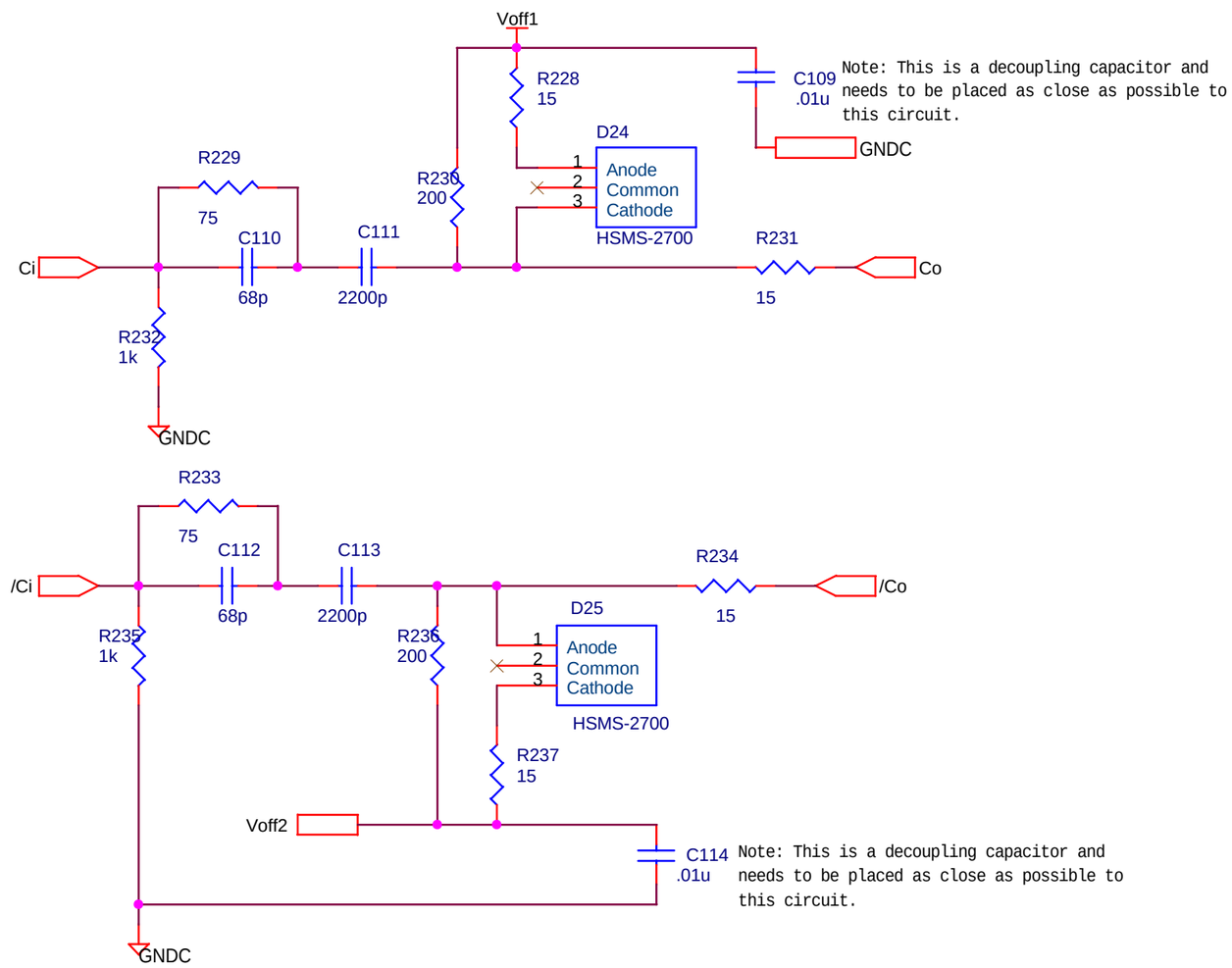
Title	Clock Pulse Waveform Shaping	
Size A	Document Number <Doc>	Rev 3
Date: Wednesday, August 11, 1999	Sheet 18 of 95	



Title	Clock Pulse Waveform Shaping	
Size A	Document Number <Doc>	Rev 3
Date: Wednesday, August 11, 1999	Sheet 19 of 95	



Title	Clock Pulse Waveform Shaping	
Size A	Document Number <Doc>	Rev 3
Date: Wednesday, August 11, 1999	Sheet 20 of 95	



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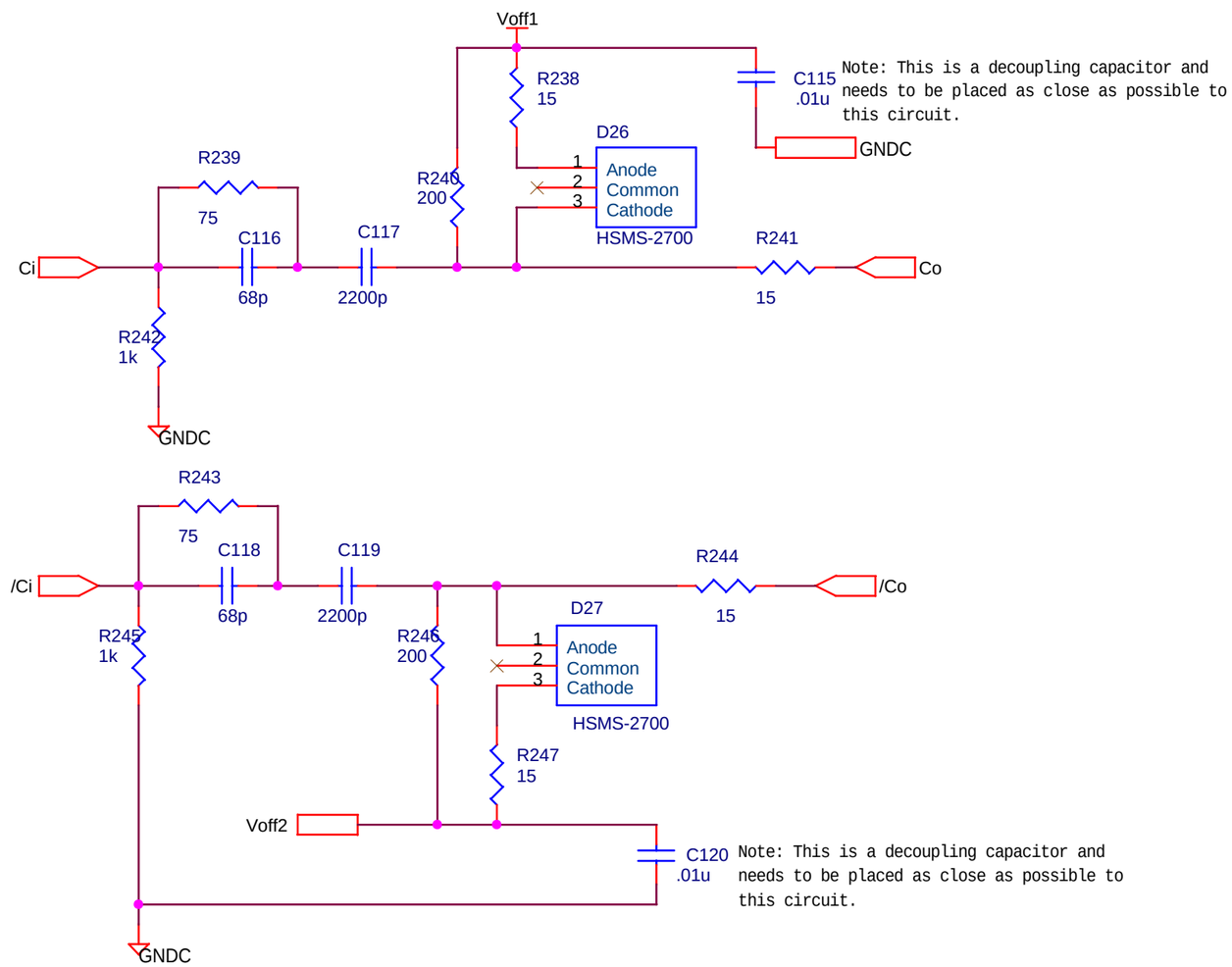
Size A	Document Number <Doc>	Rev 3
Date: Wednesday, August 11, 1999	Sheet 21 of 95	



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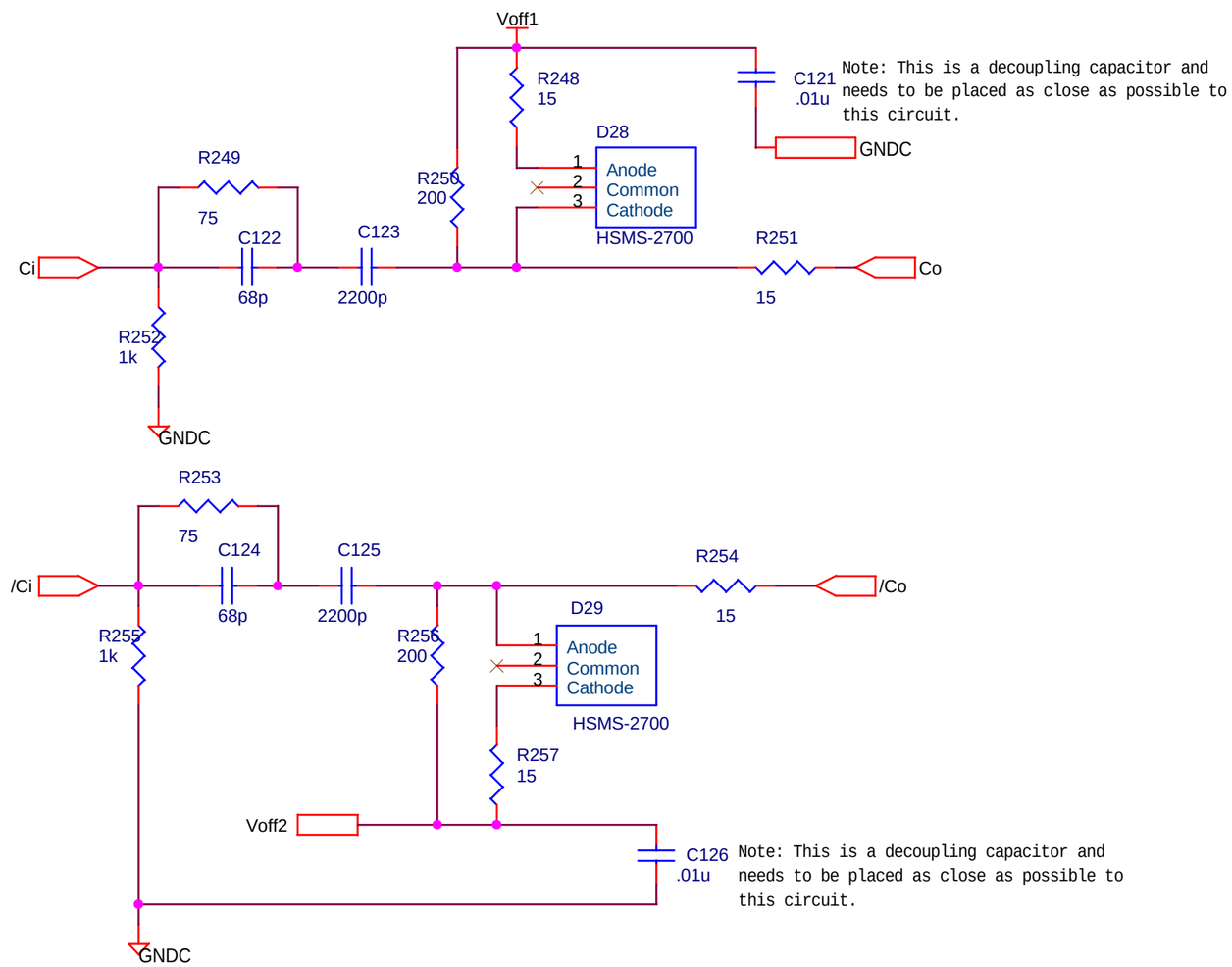
Size A	Document Number <Doc>	Rev 3
Date: Wednesday, August 11, 1999	Sheet 22 of 95	



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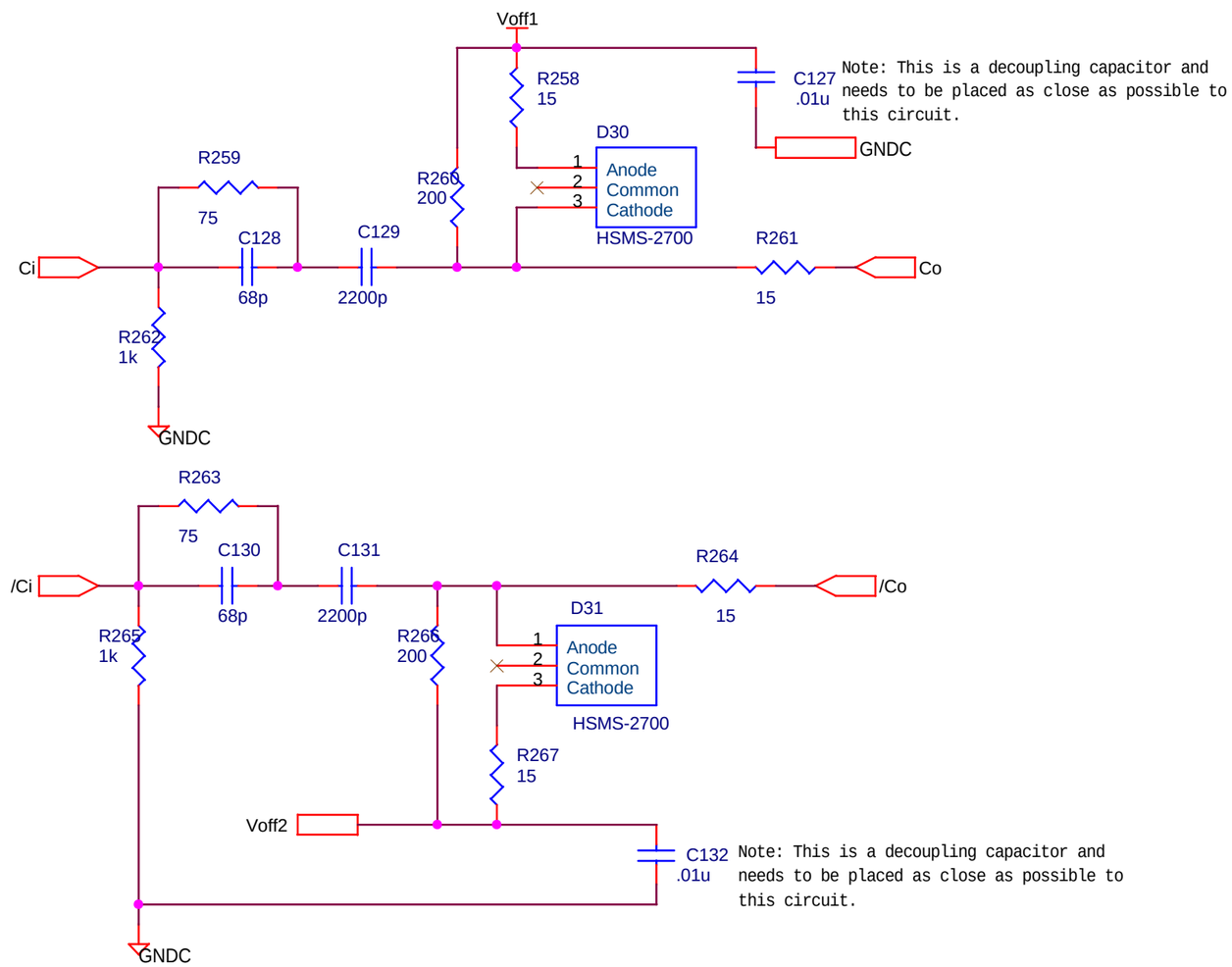
Size A	Document Number <Doc>	Rev 3
Date: Wednesday, August 11, 1999	Sheet 23 of 95	



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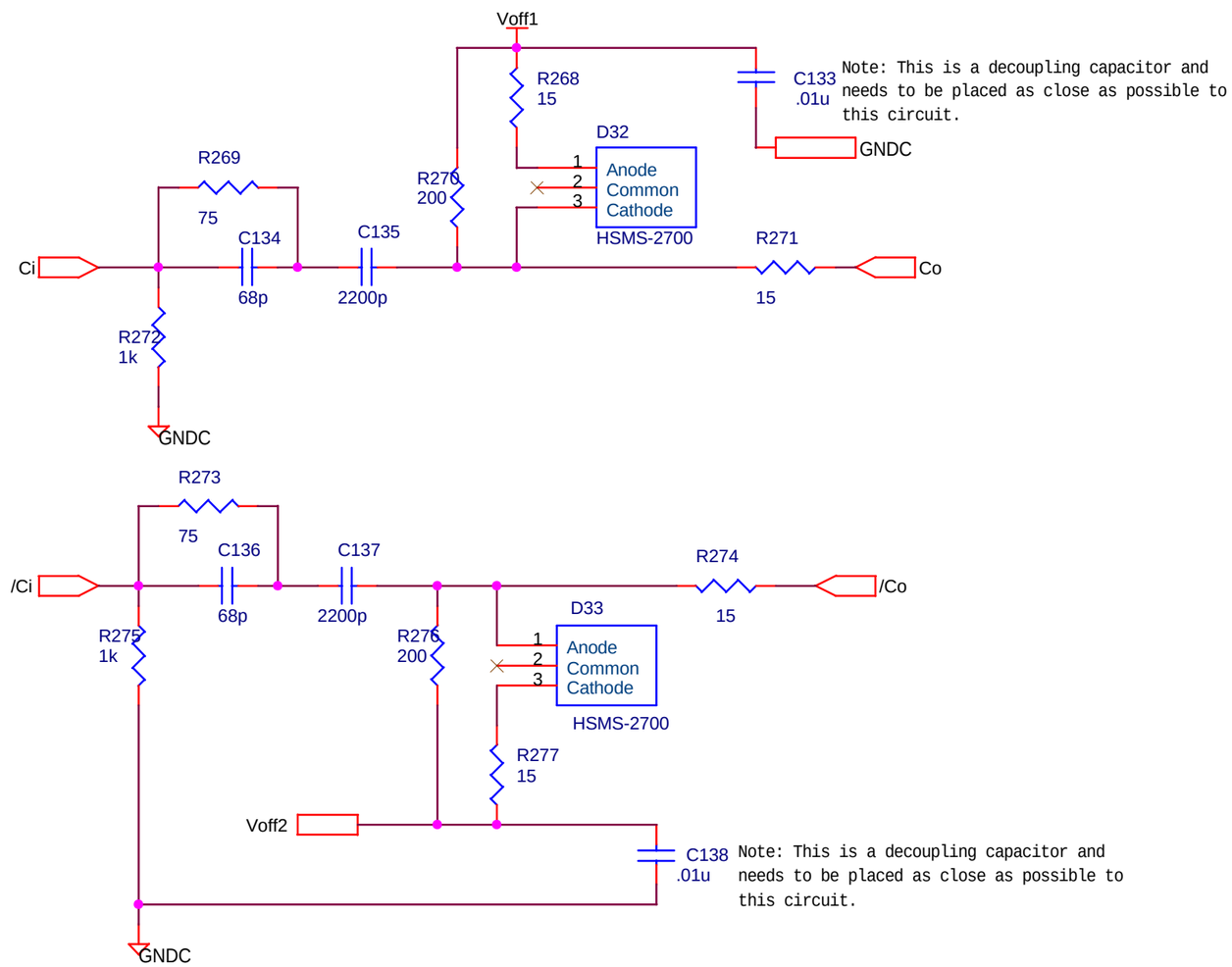
Size A	Document Number <Doc>	Rev 3
Date: Wednesday, August 11, 1999	Sheet 24 of 95	



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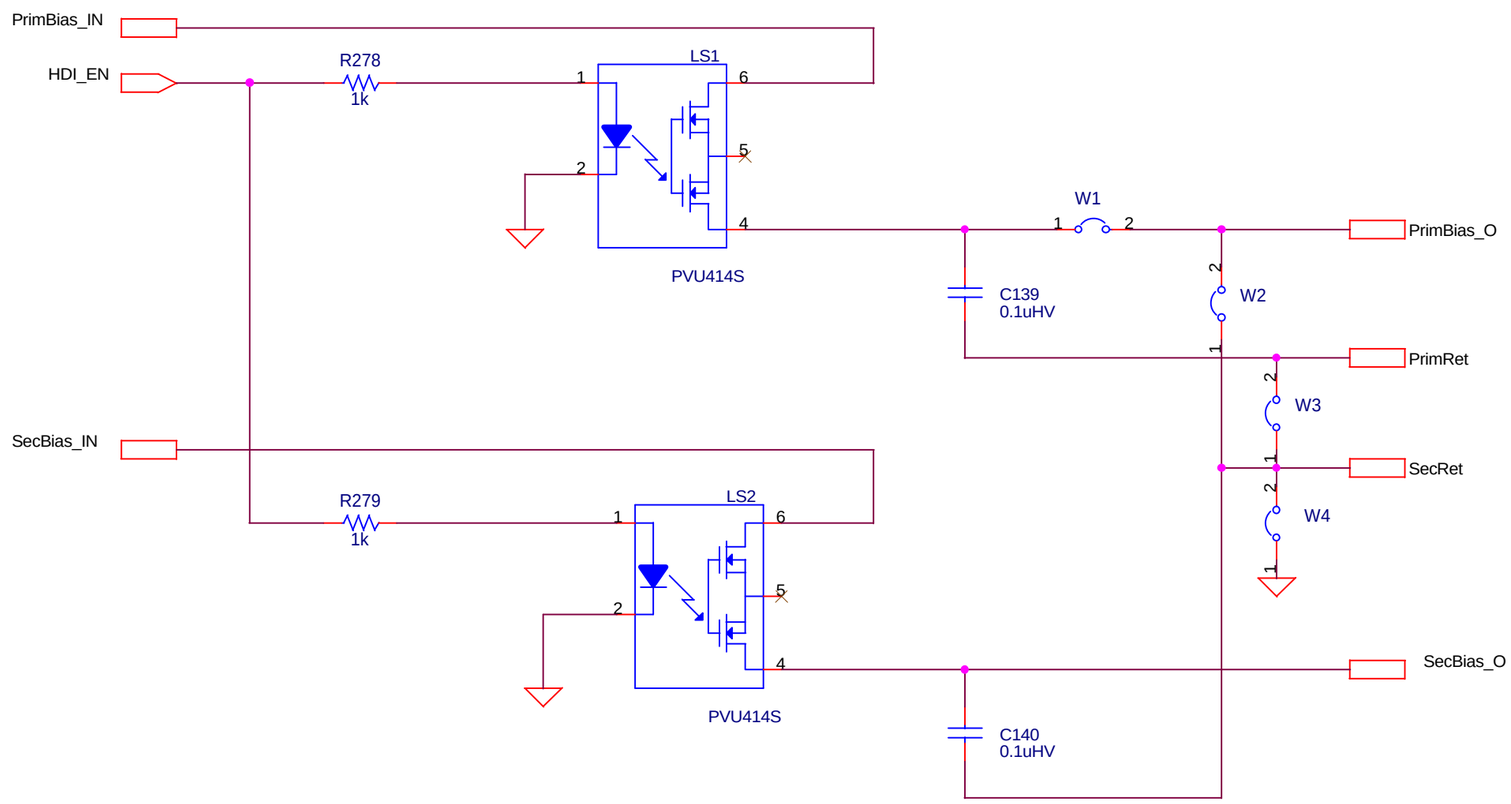
Size A	Document Number <Doc>	Rev 3
Date: Wednesday, August 11, 1999	Sheet 25 of 95	



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Tim J. Sobering
124 Burt Hall
Kansas State University
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Title: High Voltage Power Switching

Size	Document Number:	REV
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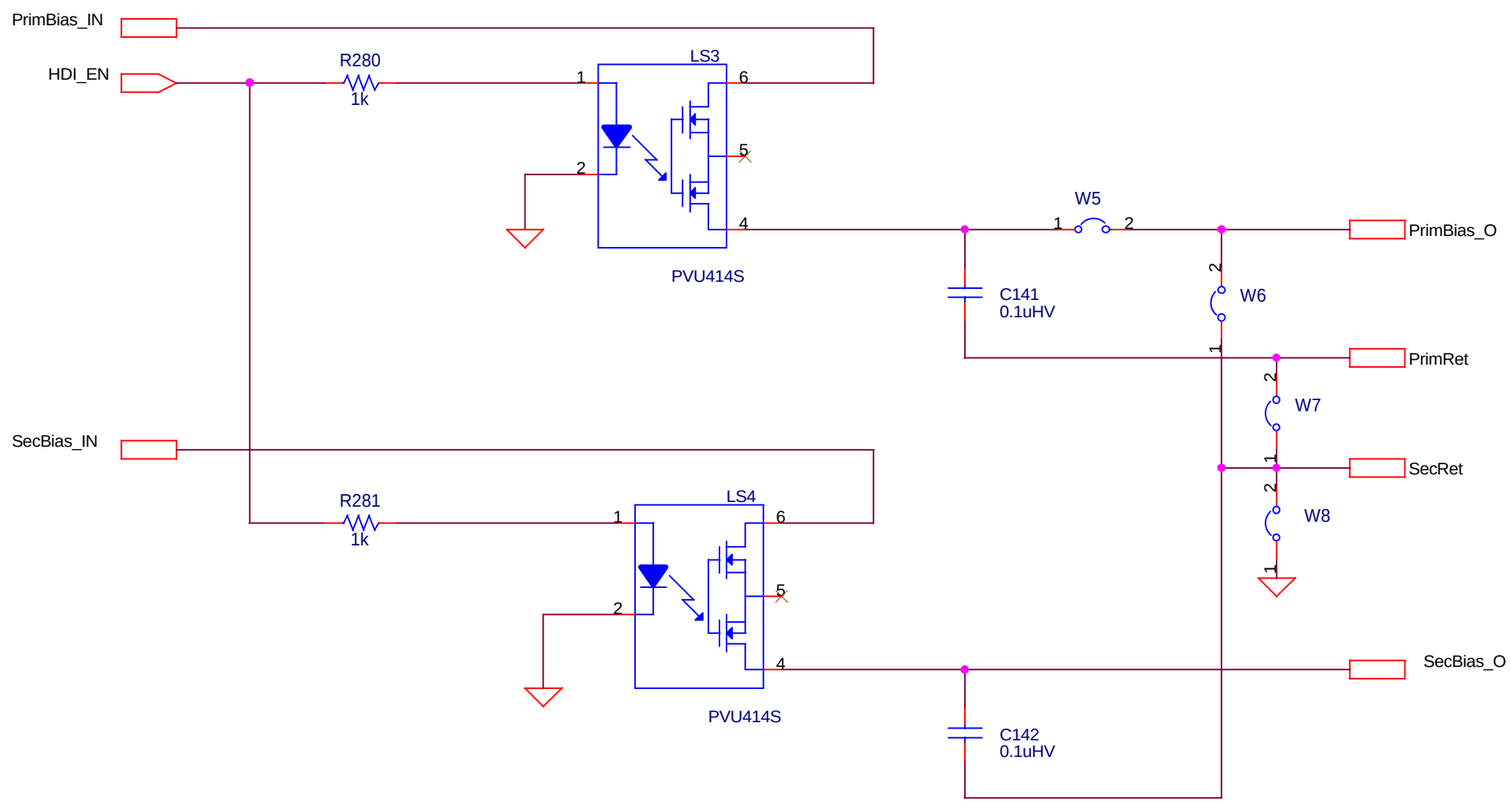

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124 Burt Hall
Kansas State University
Manhattan, KS 66506-0400

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Size	Document Number:	REV
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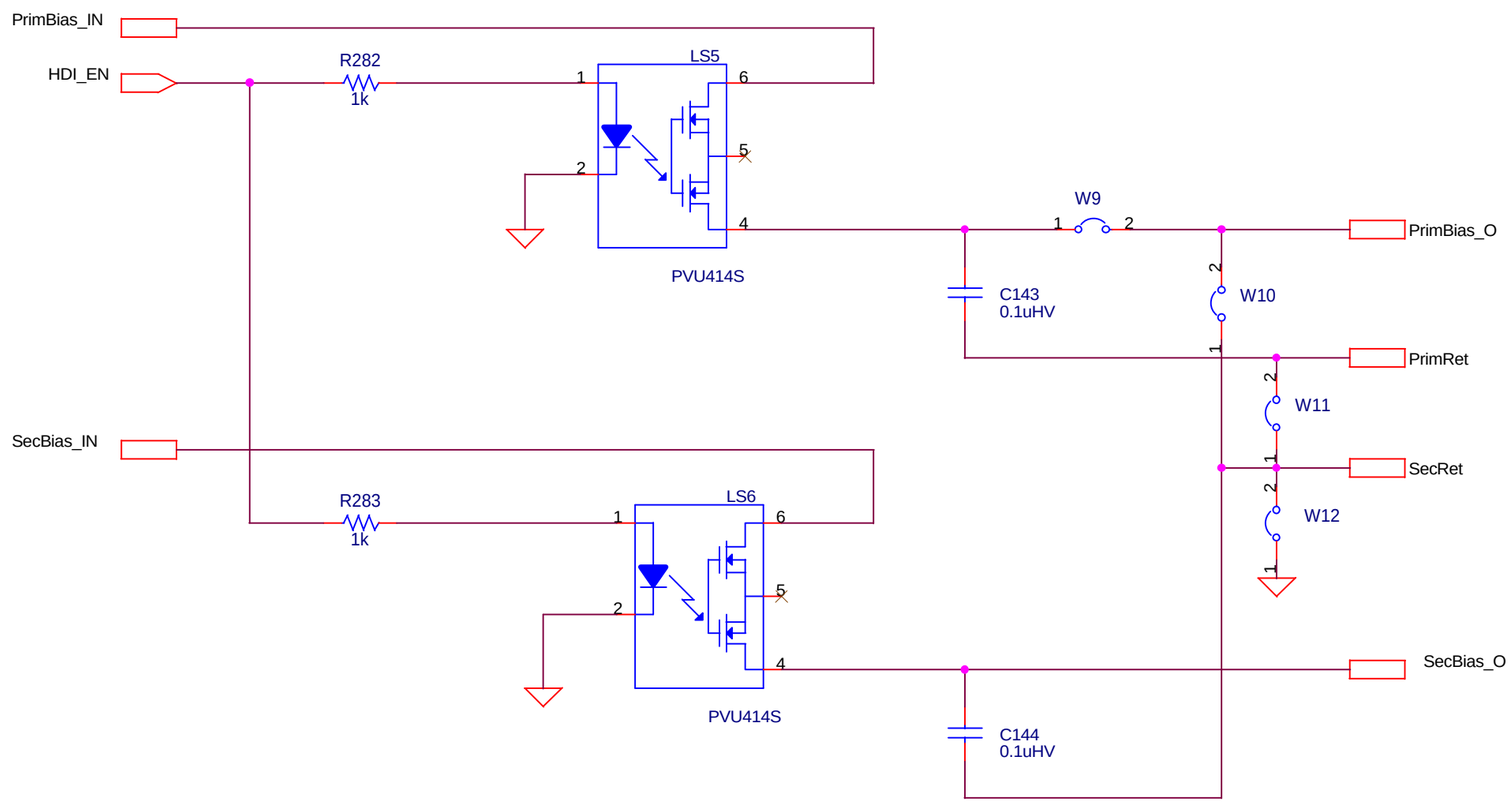

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124 Burt Hall
Kansas State University
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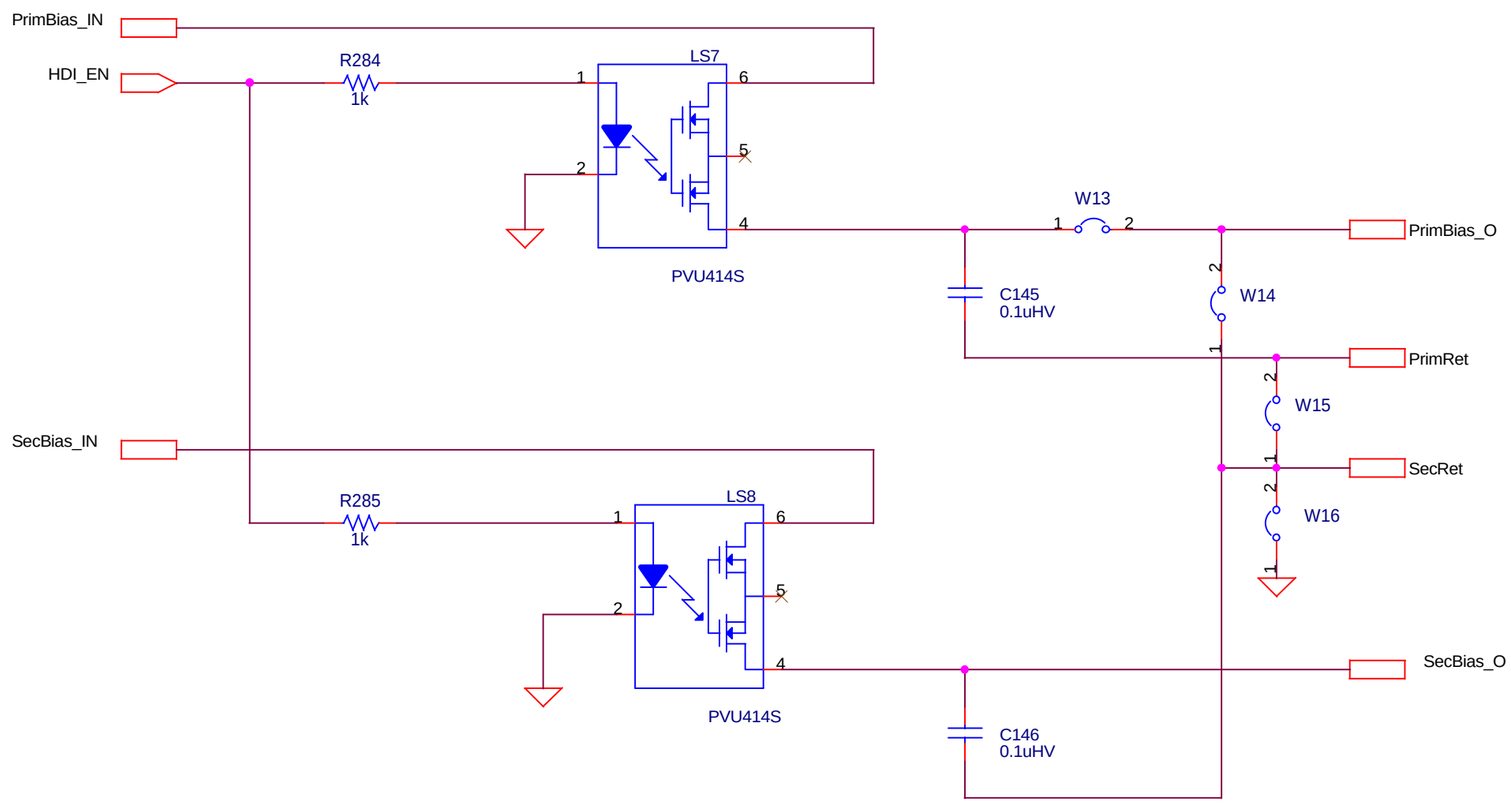

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124 Burt Hall
Kansas State University
Manhattan, KS 66506-0400

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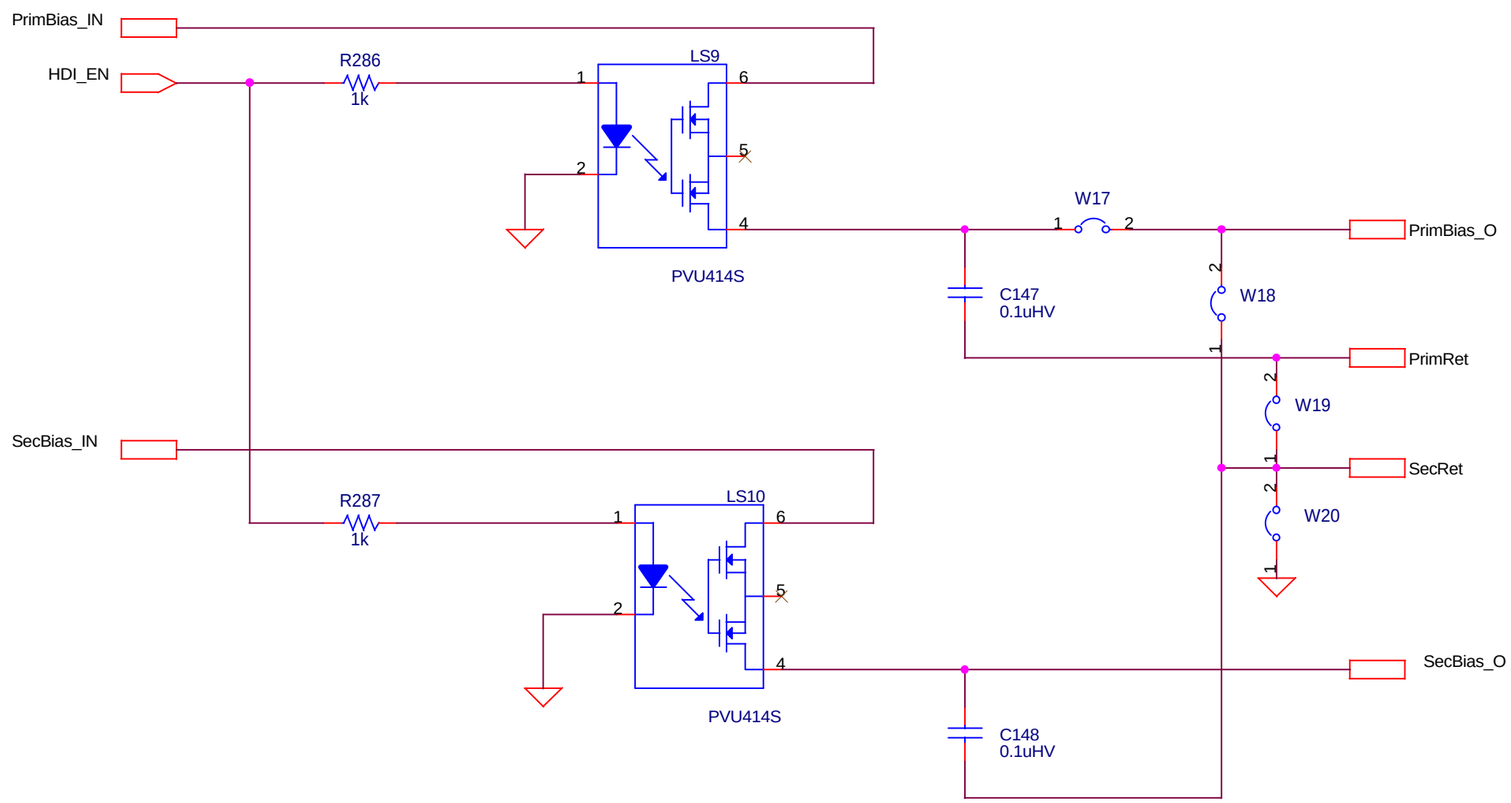

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124 Burt Hall
Kansas State University
Manhattan, KS 66506-0400

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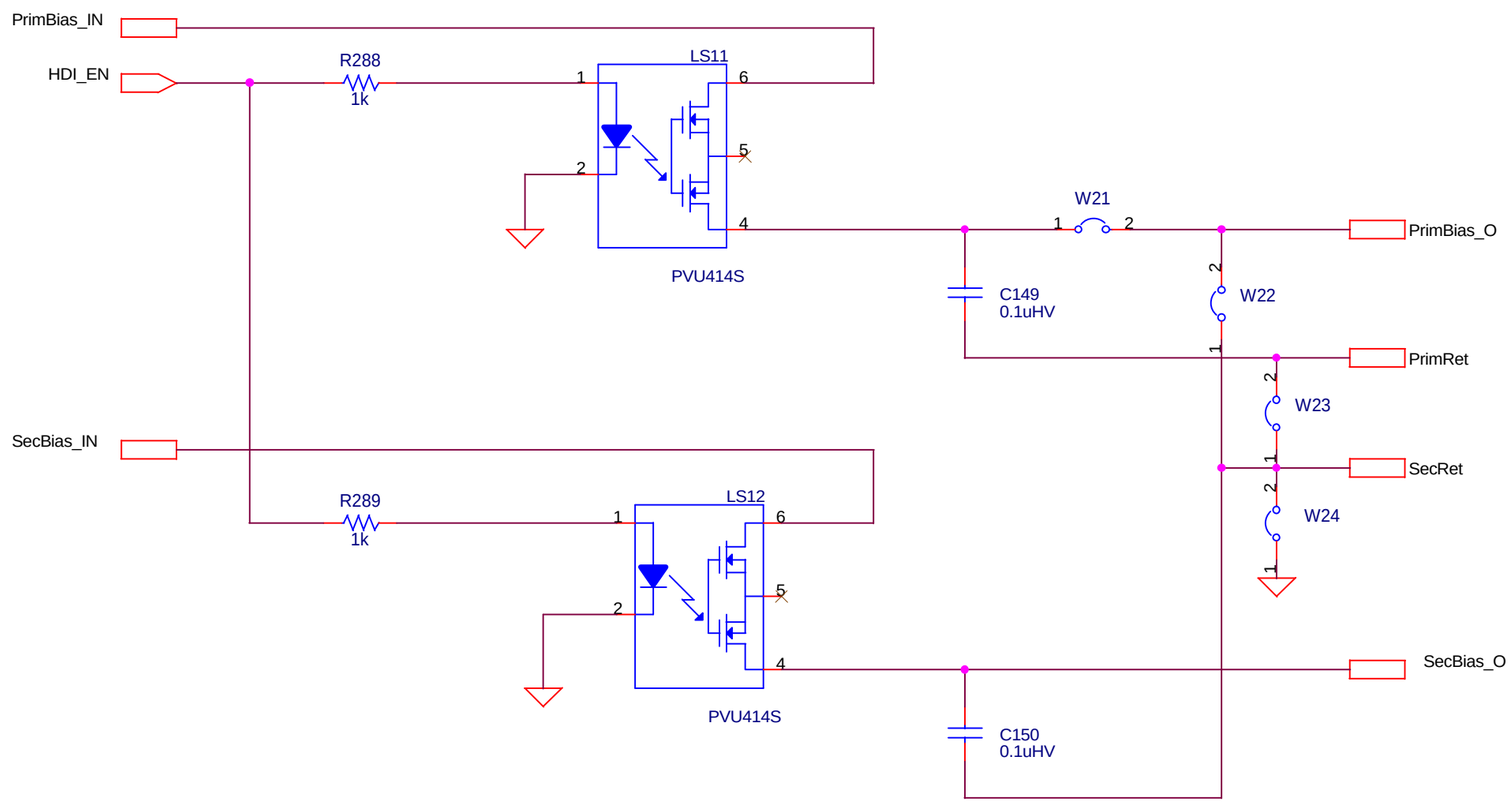

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124 Burt Hall
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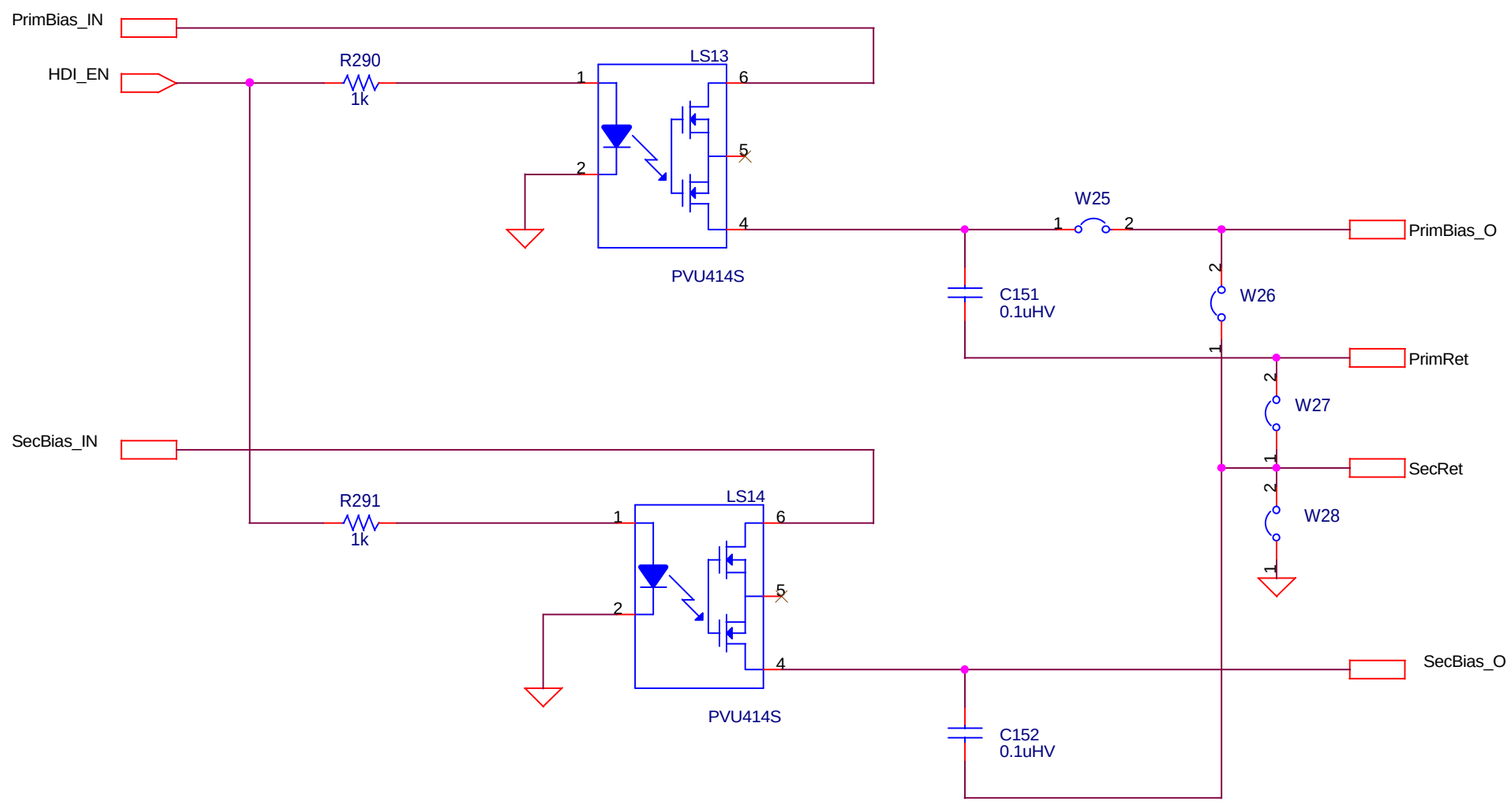

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124 Burt Hall
Kansas State University
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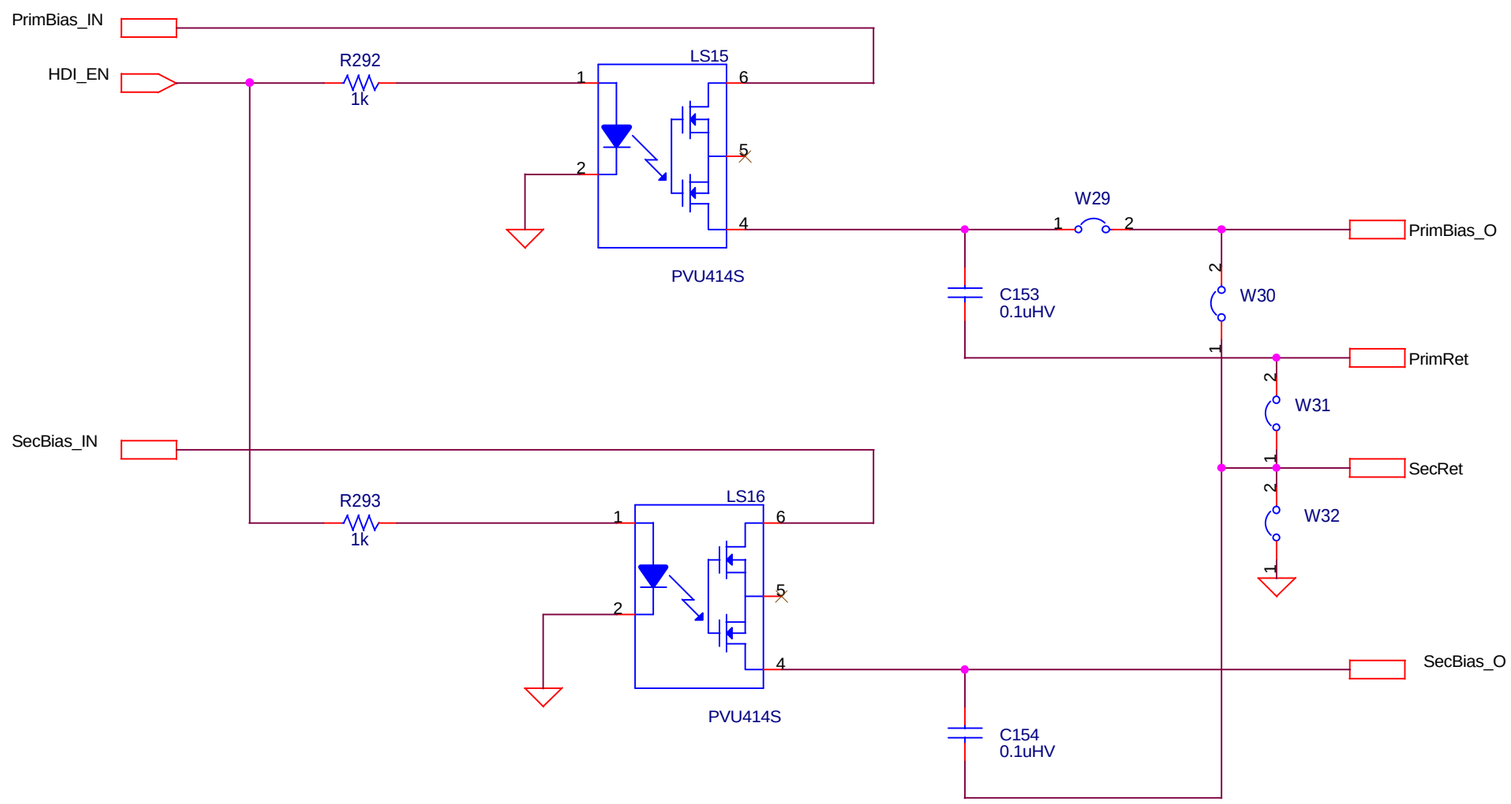

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Size	Document Number:	REV
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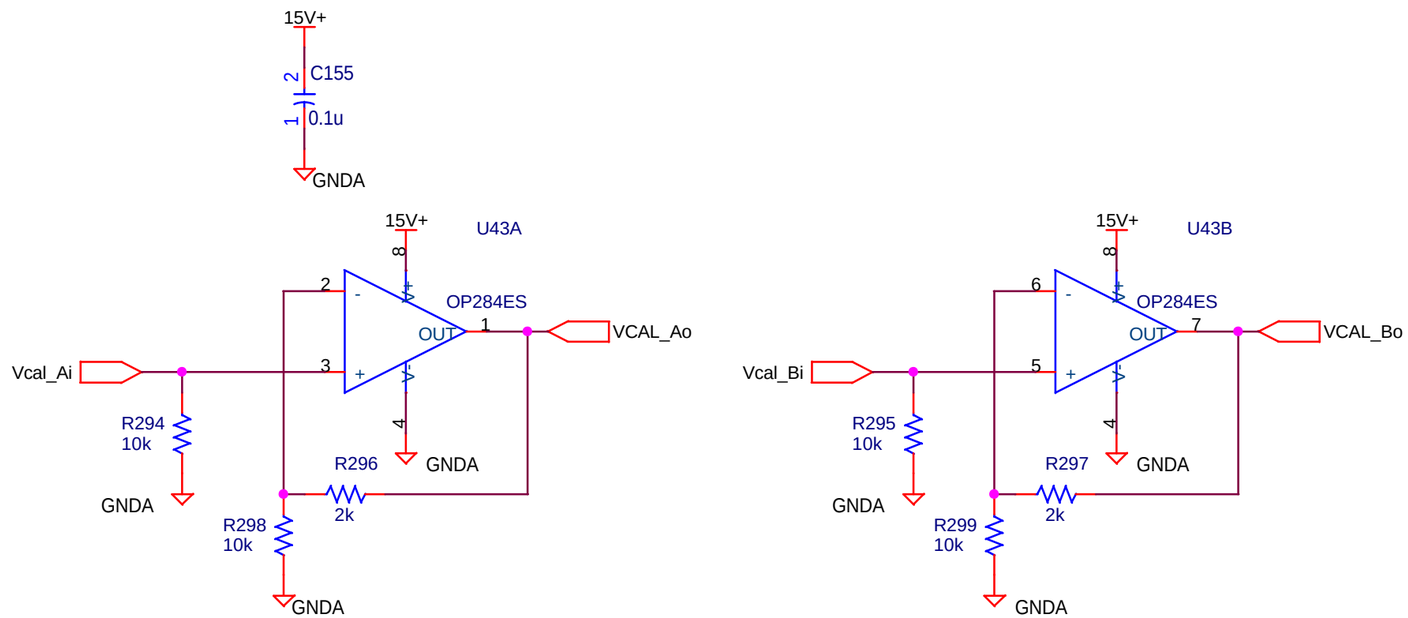

Title
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Size	Document Number	Rev
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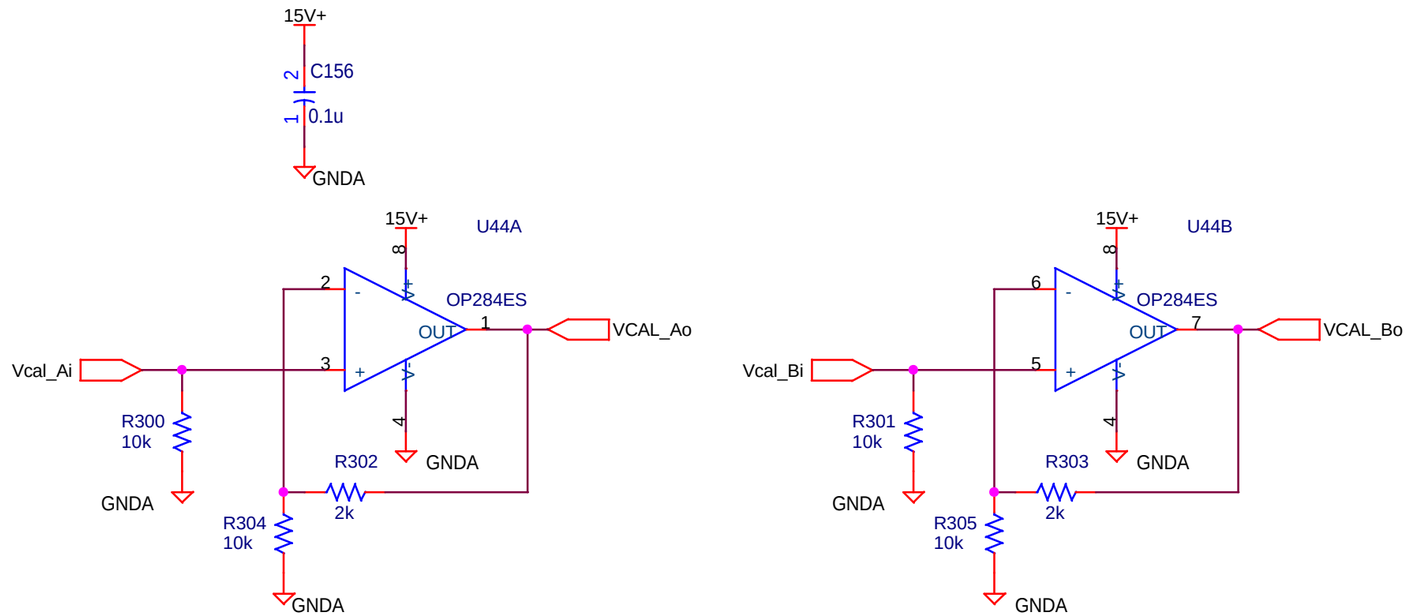
Date: Wednesday, August 11, 1999 Sheet 34 of 95



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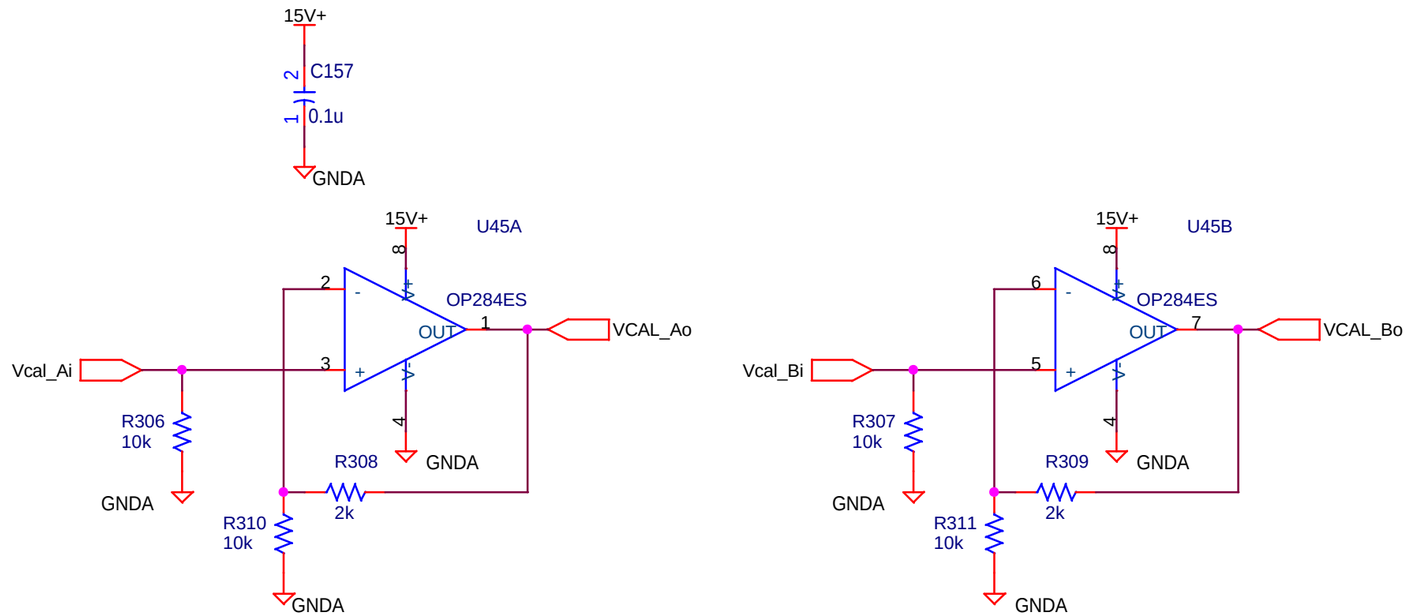
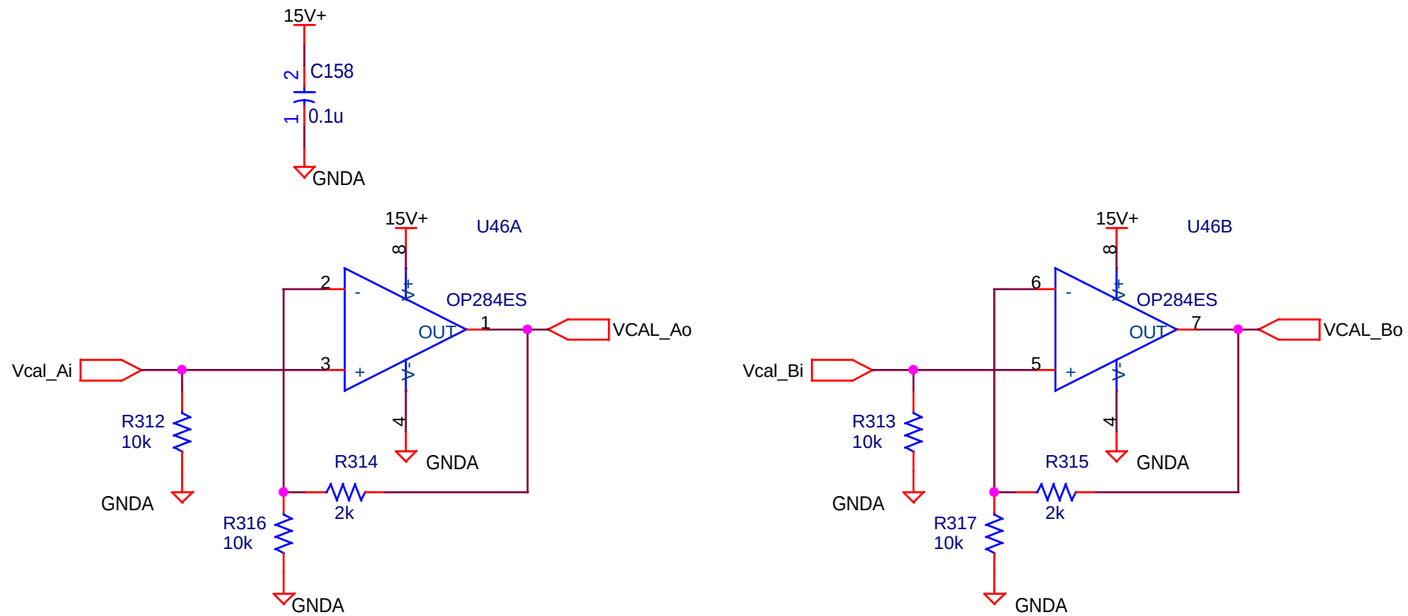
Size A	Document Number <Doc>	Rev 3
Date: Wednesday, August 11, 1999	Sheet 35 of 95	



Title
Amplifiers for Vcal signal

Size	Document Number	Rev
A	<Doc>	3

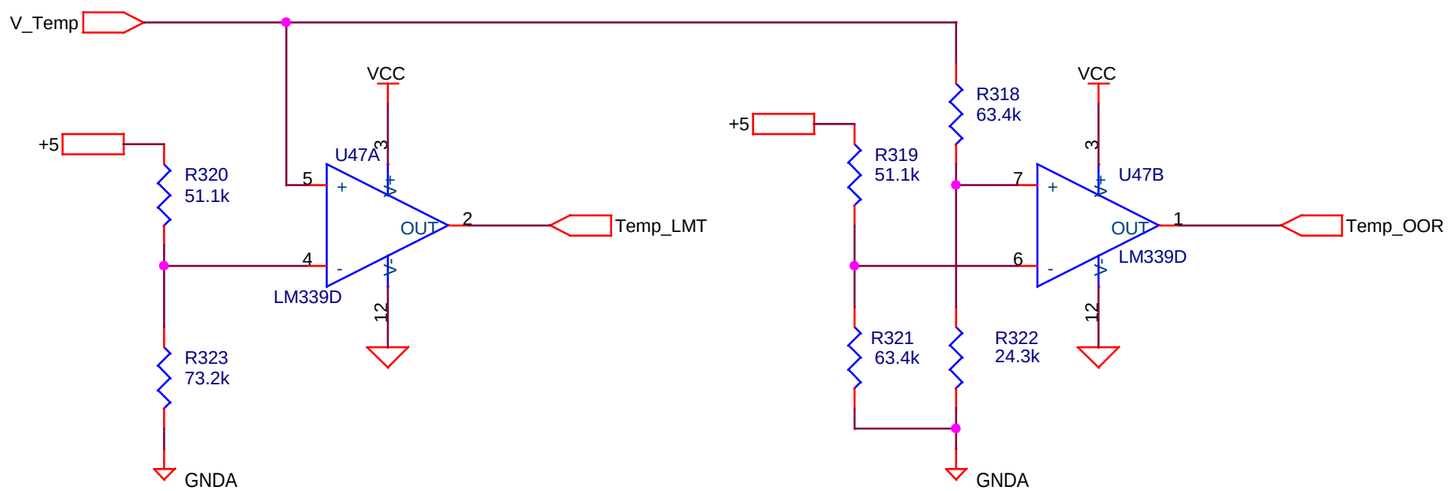
Date: Wednesday, August 11, 1999 Sheet 36 of 95



Title
Amplifiers for Vcal signal

Size	Document Number	Rev
A	<Doc>	3

Date: Wednesday, August 11, 1999 Sheet 37 of 95



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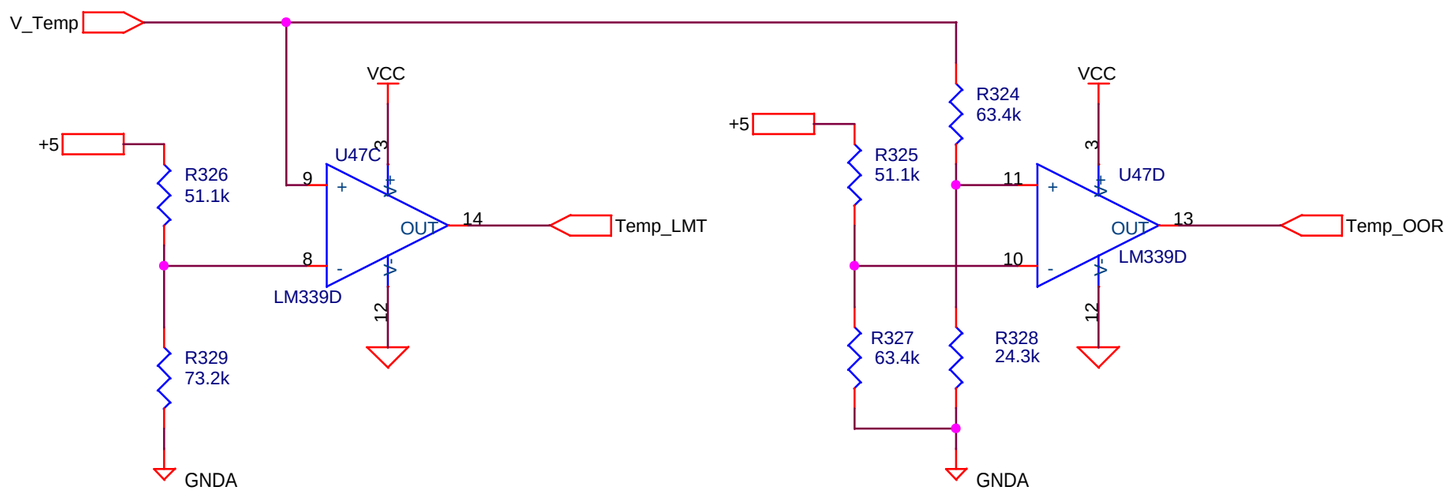
Size A	Document Number <Doc>	Rev 3
Date: Wednesday, August 11, 1999	Sheet 38 of 95	



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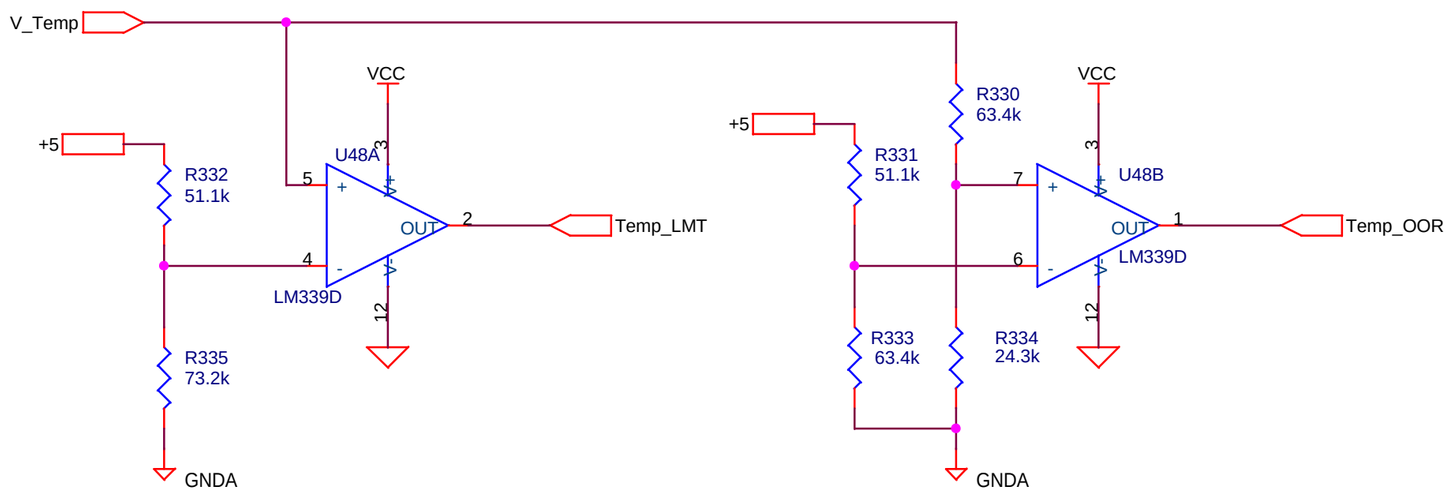
Size A	Document Number <Doc>	Rev 3
Date: Wednesday, August 11, 1999	Sheet 39 of 95	



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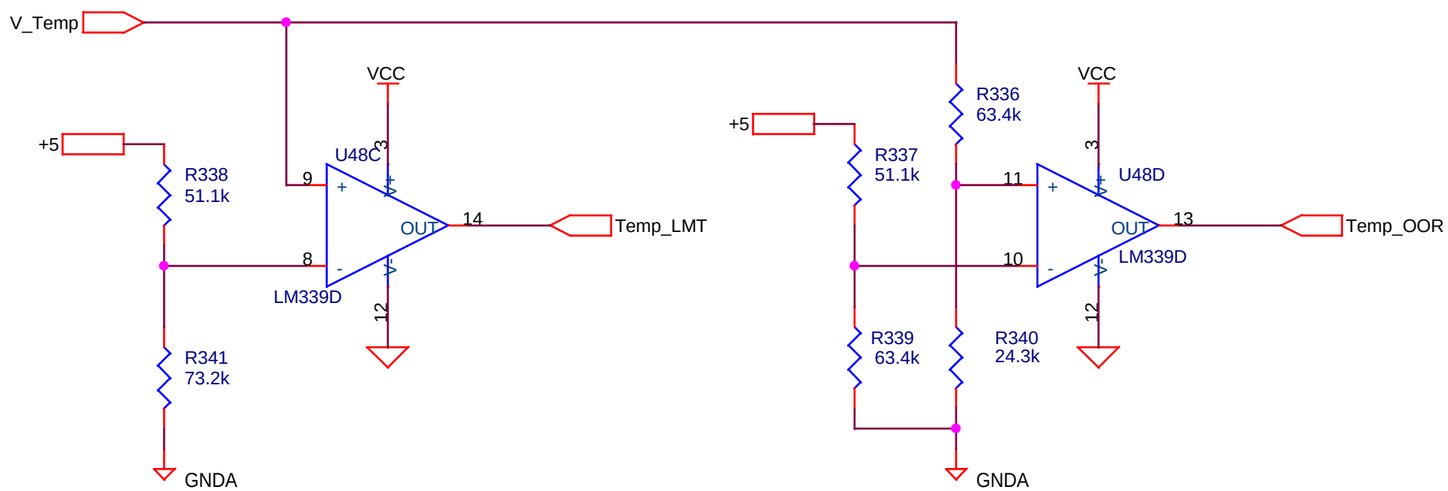
Size A	Document Number <Doc>		Rev 3
Date: Wednesday, August 11, 1999		Sheet 40 of 95	



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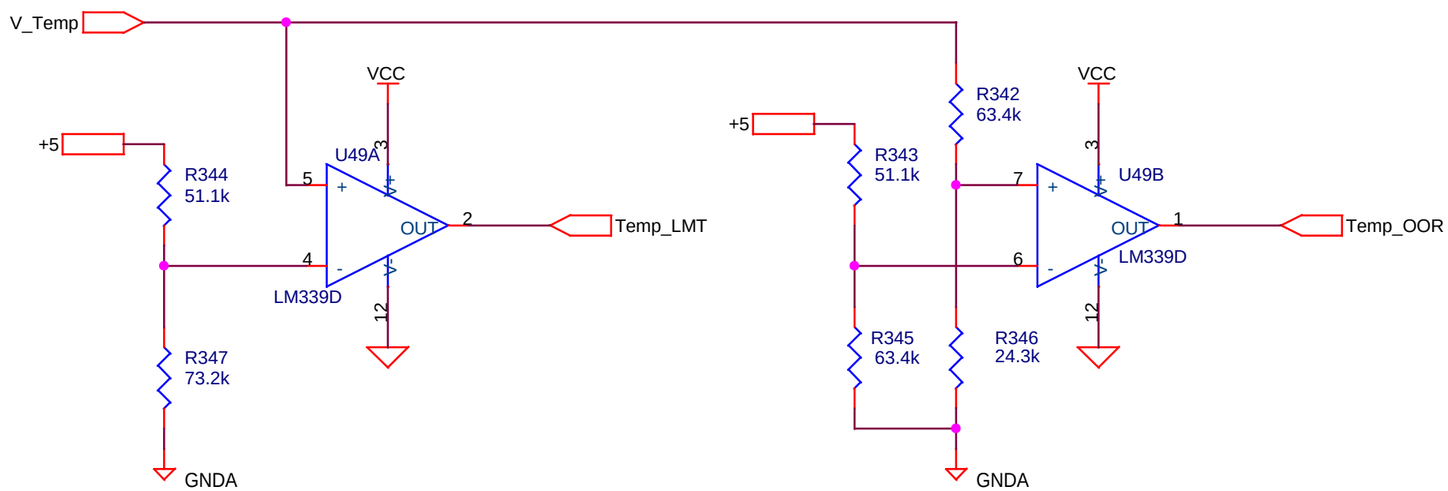

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Size	Document Number	Rev
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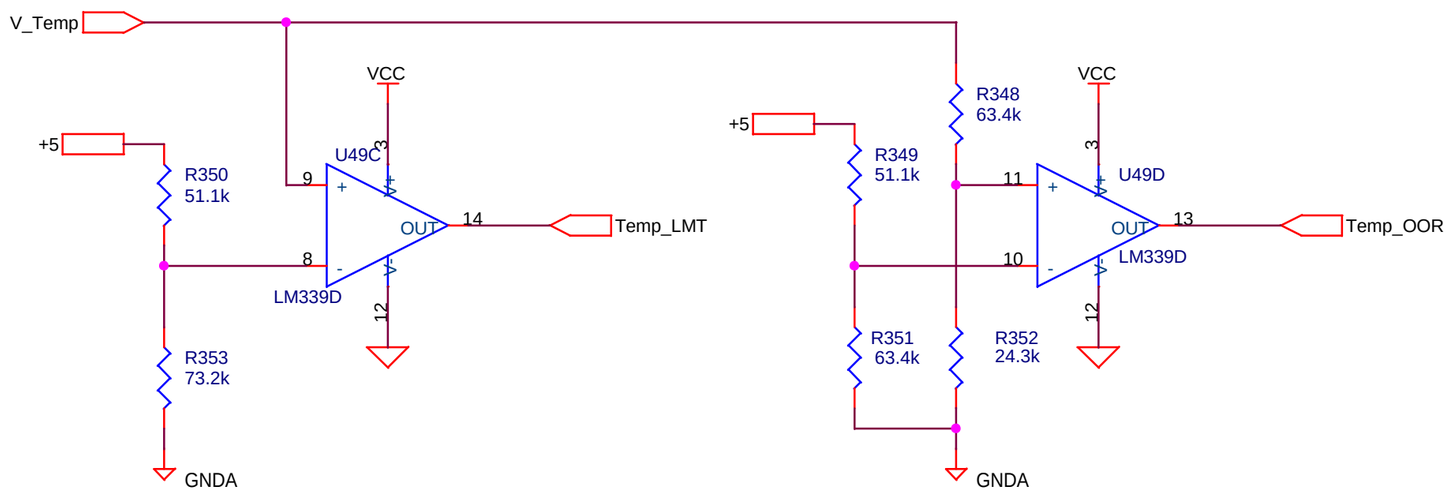

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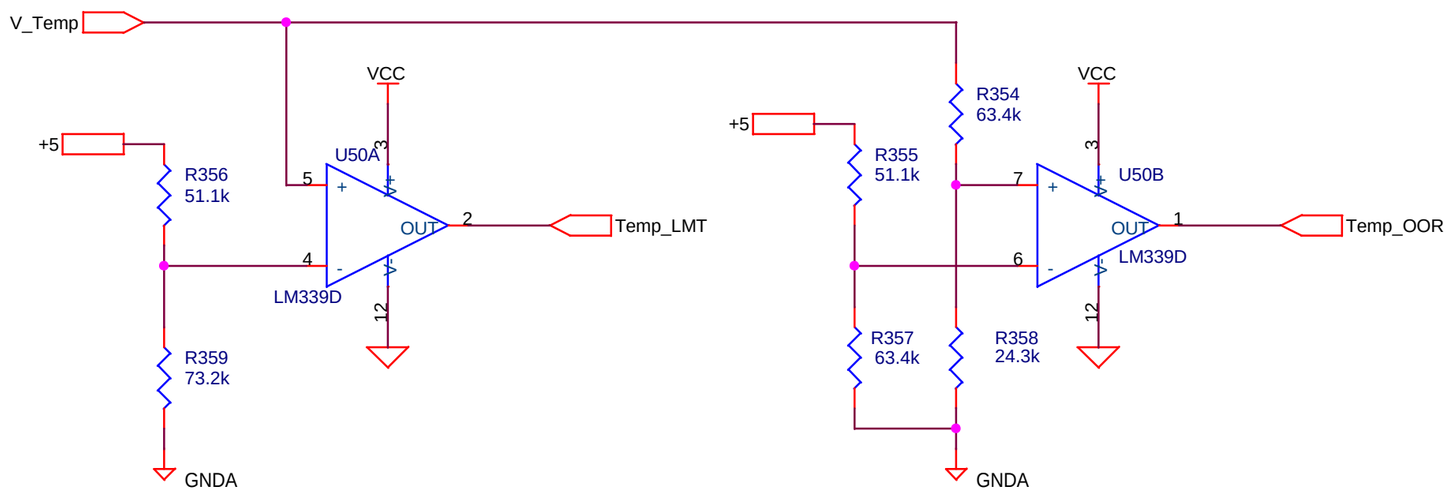
Size A	Document Number <Doc>	Rev 3
Date: Wednesday, August 11, 1999	Sheet 43 of 95	



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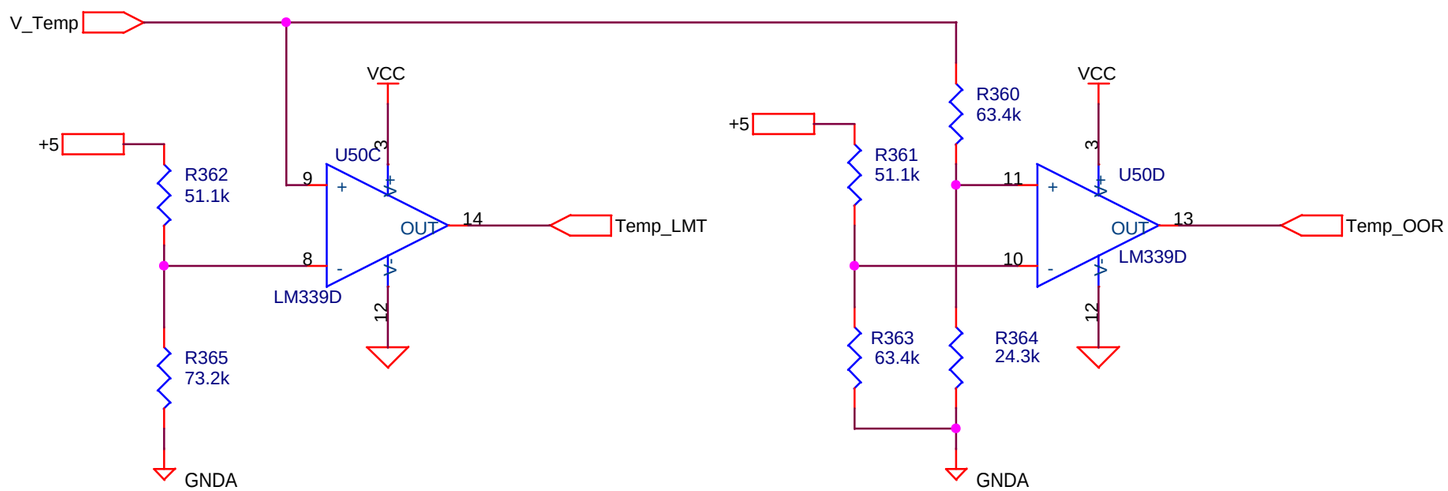
Date: Wednesday, August 11, 1999	Sheet 44 of 95	



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Tempatrue Level Indicator

Size	Document Number	Rev
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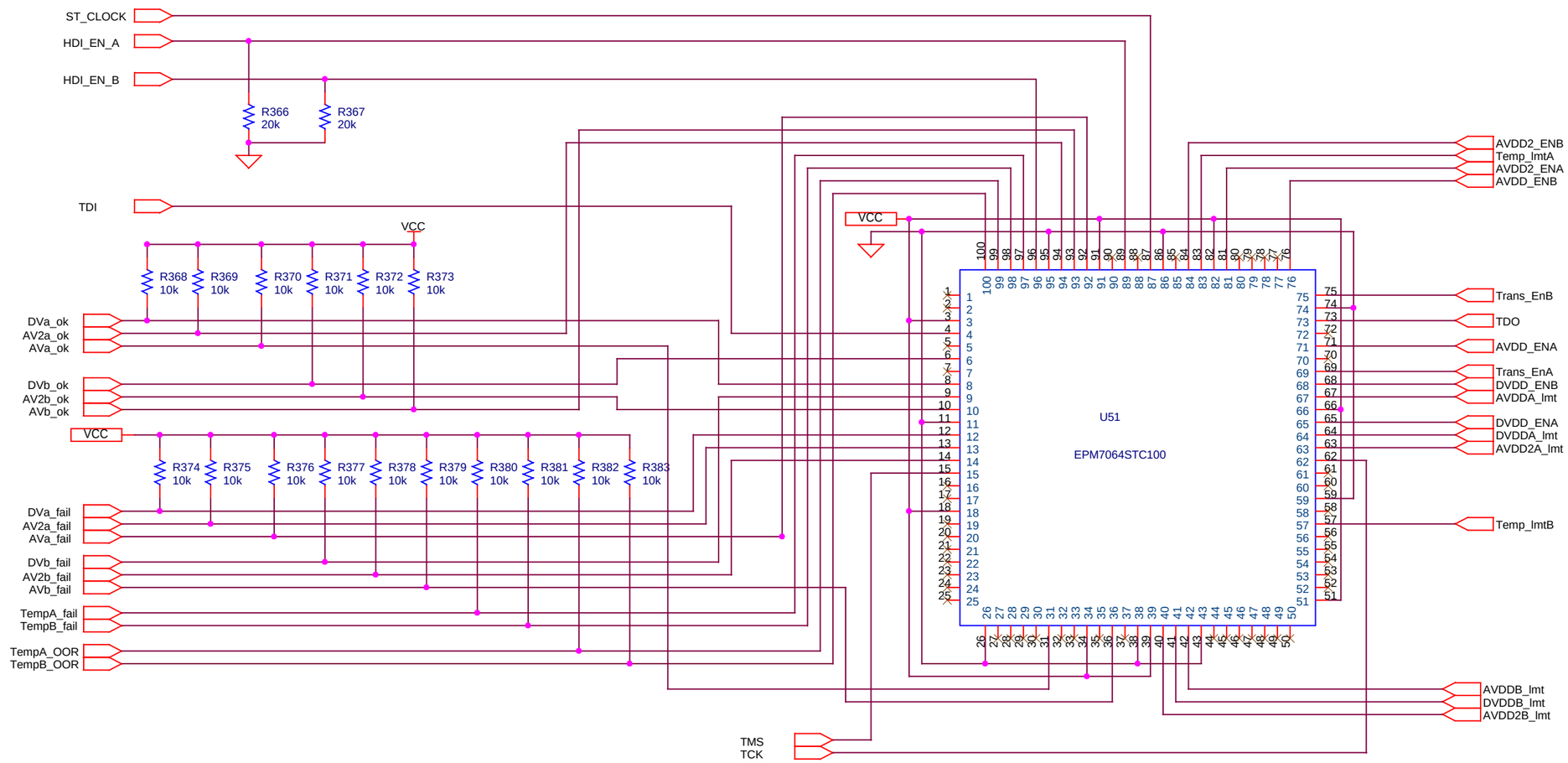
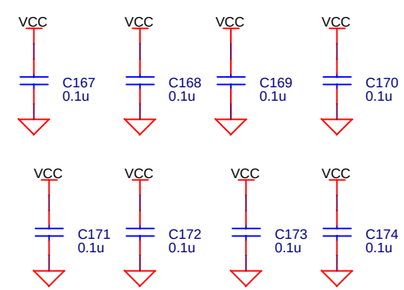
Date: Wednesday, August 11, 1999 Sheet 45 of 95





Capacitors are for VCC pins 3, 18, 34, 39, 51, 66, 82, and 91 on the Altera chip. Pins 11, 26, 38, 43, 59, 74, 86, and 95 are tied to ground, as programmed by R. Taylor.

The enable signals are anticipated to be active high.

EMP7064STC100 is a 44-pin smd device (Altera). It can be programmed on board with an Altera Bit-Blaster.

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Tim J. Sobering
124 Burt Hall
Kansas State University
Manhattan, KS 66506-0400

Title: M013: Chan. A Power Control

Size	Document Number:	REV
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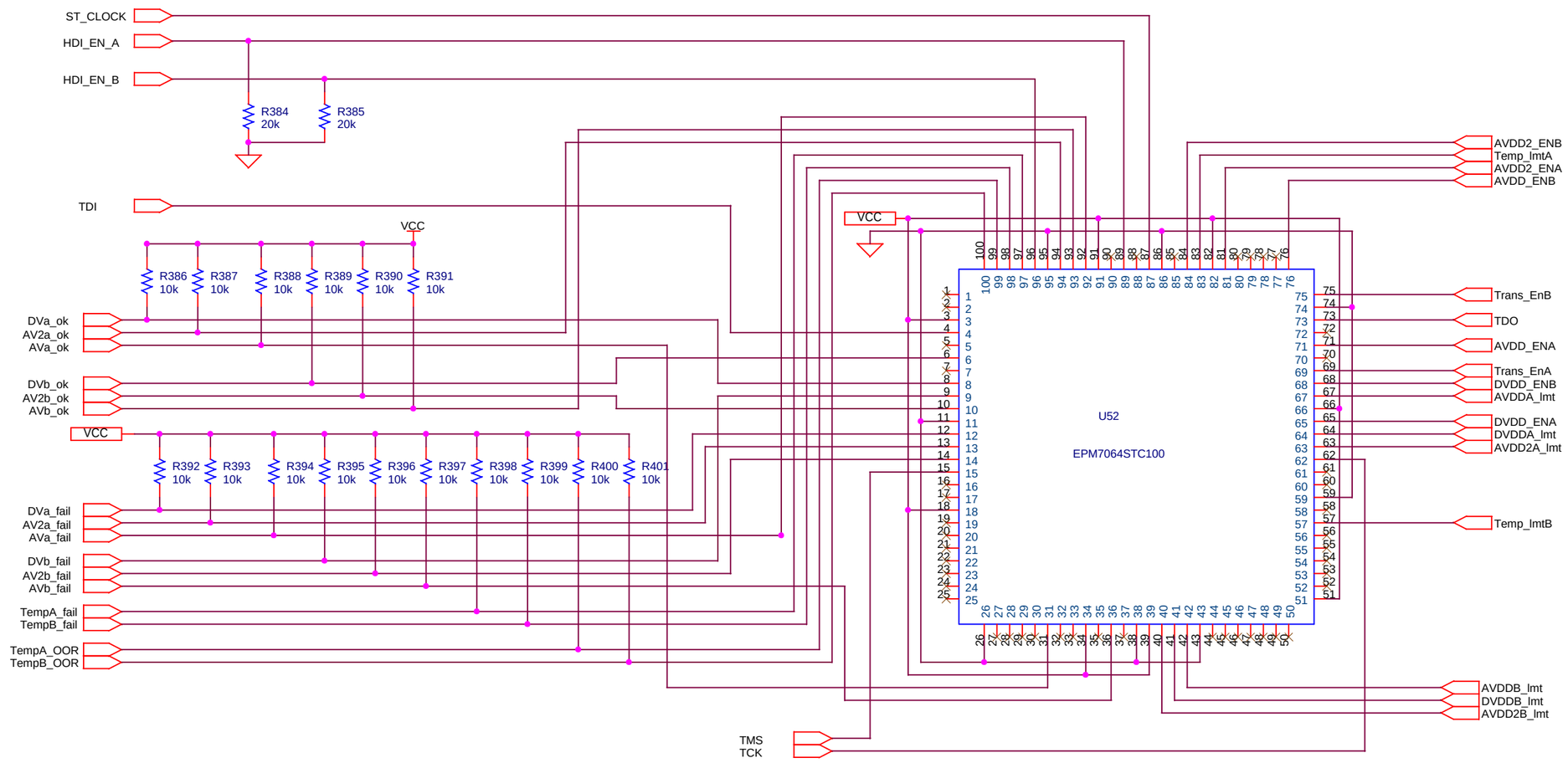

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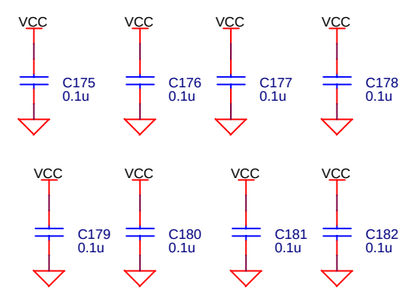

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Tim J. Sobering
124 Burt Hall
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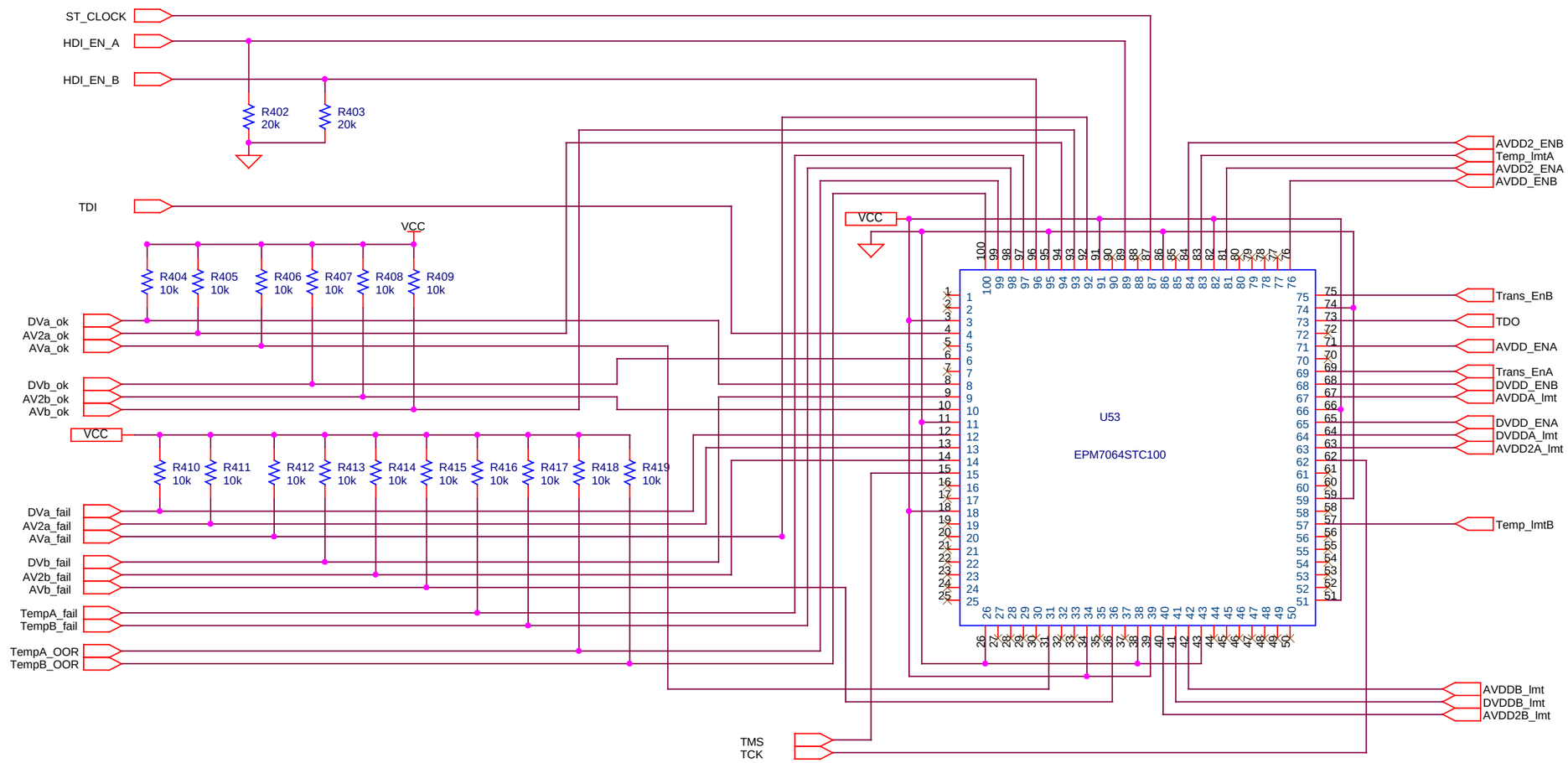

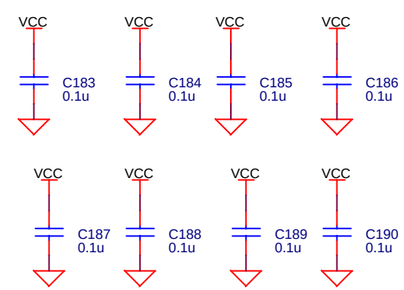

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Size	Document Number:	REV
A	HEP008-M013	3

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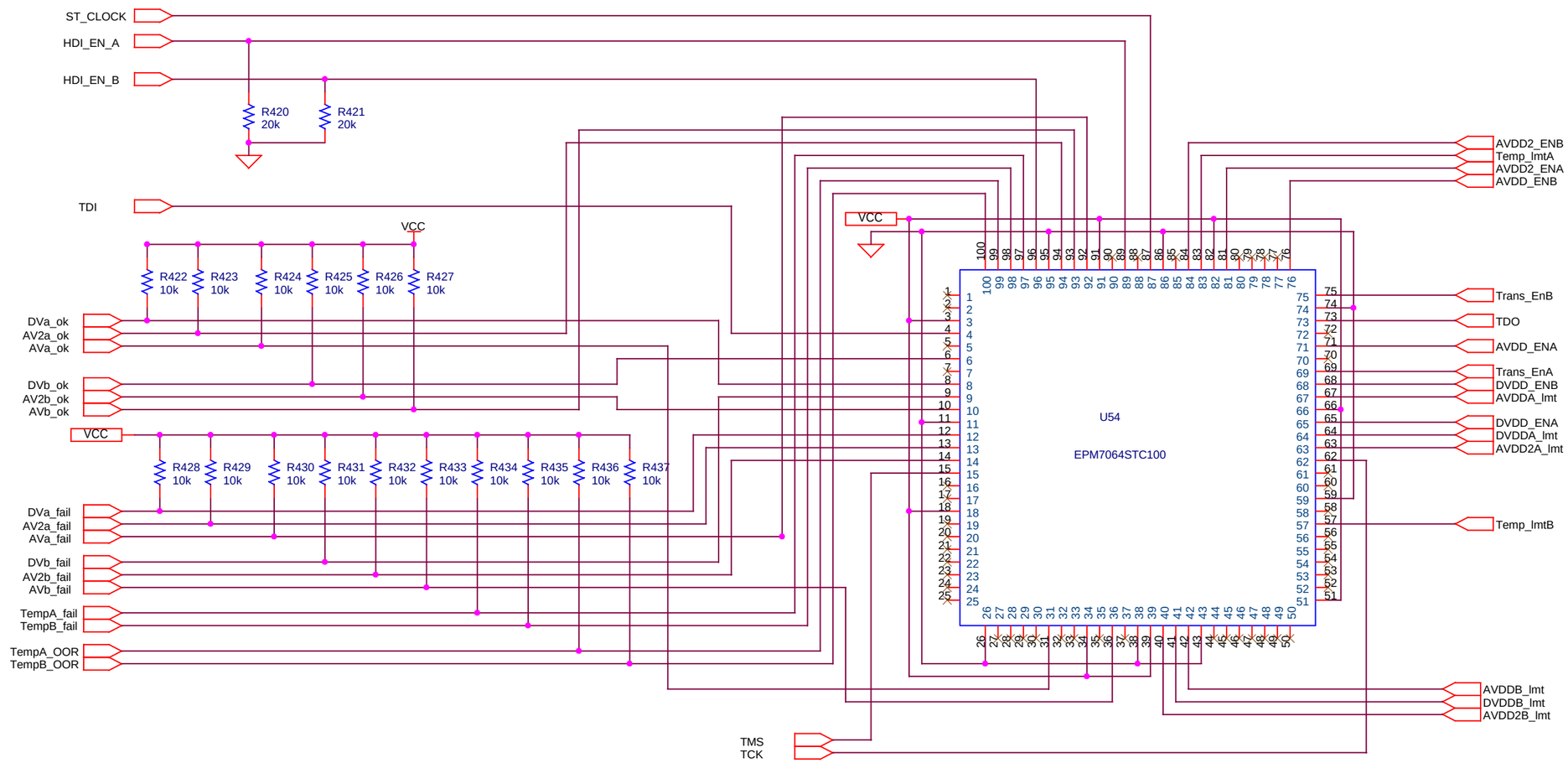

Capacitors are for VCC pins 3, 18, 34, 39, 51, 66, 82, and 91 on the Altera chip. Pins 11, 26, 38, 43, 59, 74, 86, and 95 are tied to ground, as programmed by R. Taylor.

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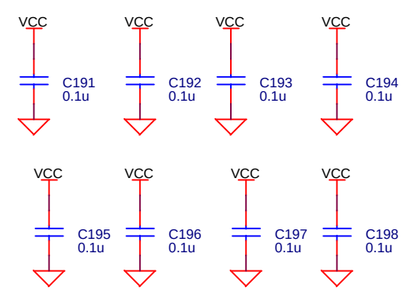

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124 Burt Hall
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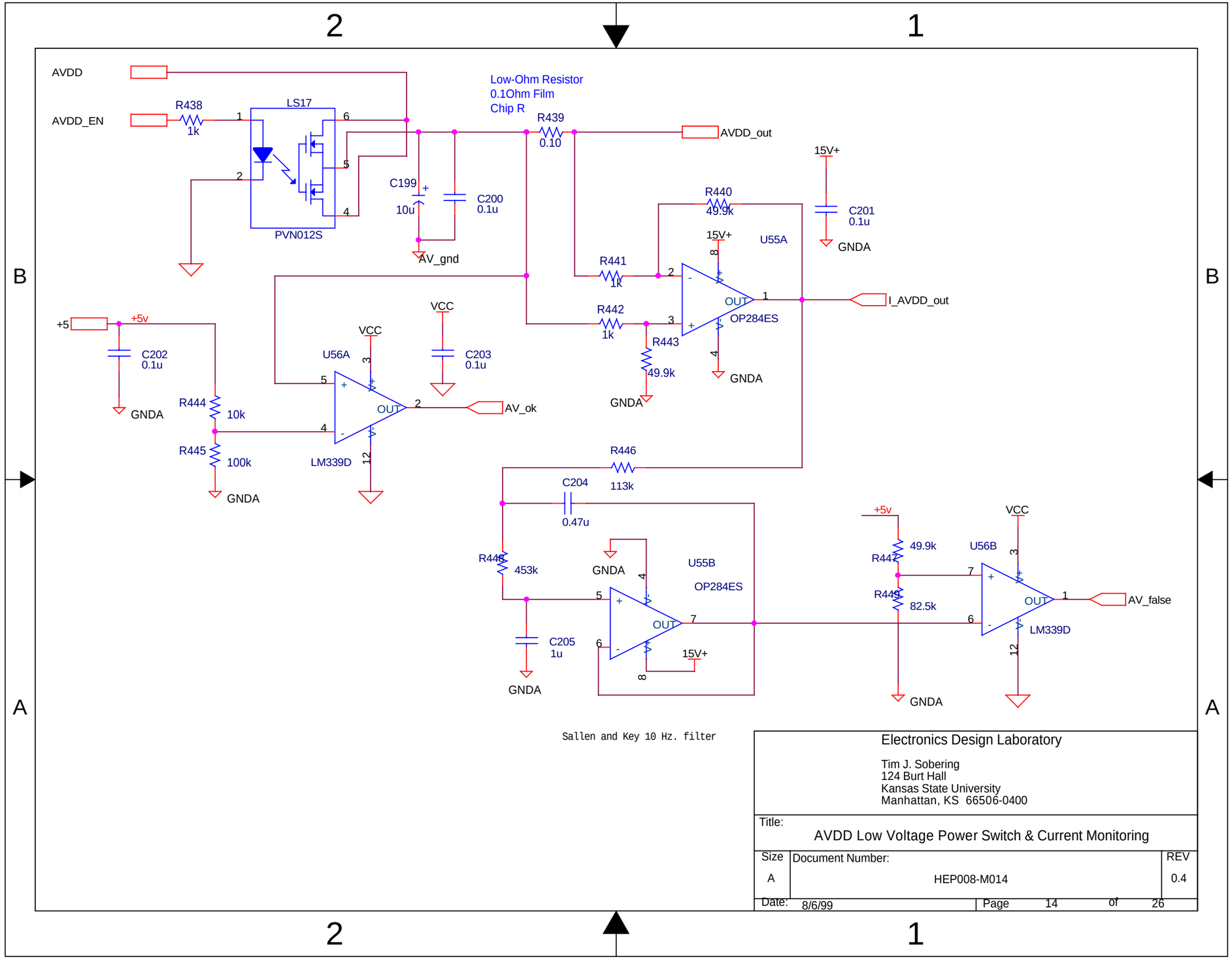
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AVDD_EN
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LS17
PVN012S
Low-Ohm Resistor
0.1Ohm Film
Chip R
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C199
10u
C200
0.1u
AV_gnd
15V+
C201
0.1u
GNDA
R440
49.9k
U55A
R441
1k
R442
1k
R443
49.9k
OP284ES
I_AVDD_out
+5
+5v
C202
0.1u
VCC
U56A
C203
0.1u
R444
10k
R445
100k
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C204
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1u
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R449
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Sallen and Key 10 Hz. filter
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Kansas State University
Manhattan, KS 66506-0400
Title:
AVDD Low Voltage Power Switch & Current Monitoring
Size
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Document Number:
HEP008-M014
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Date: 8/6/99
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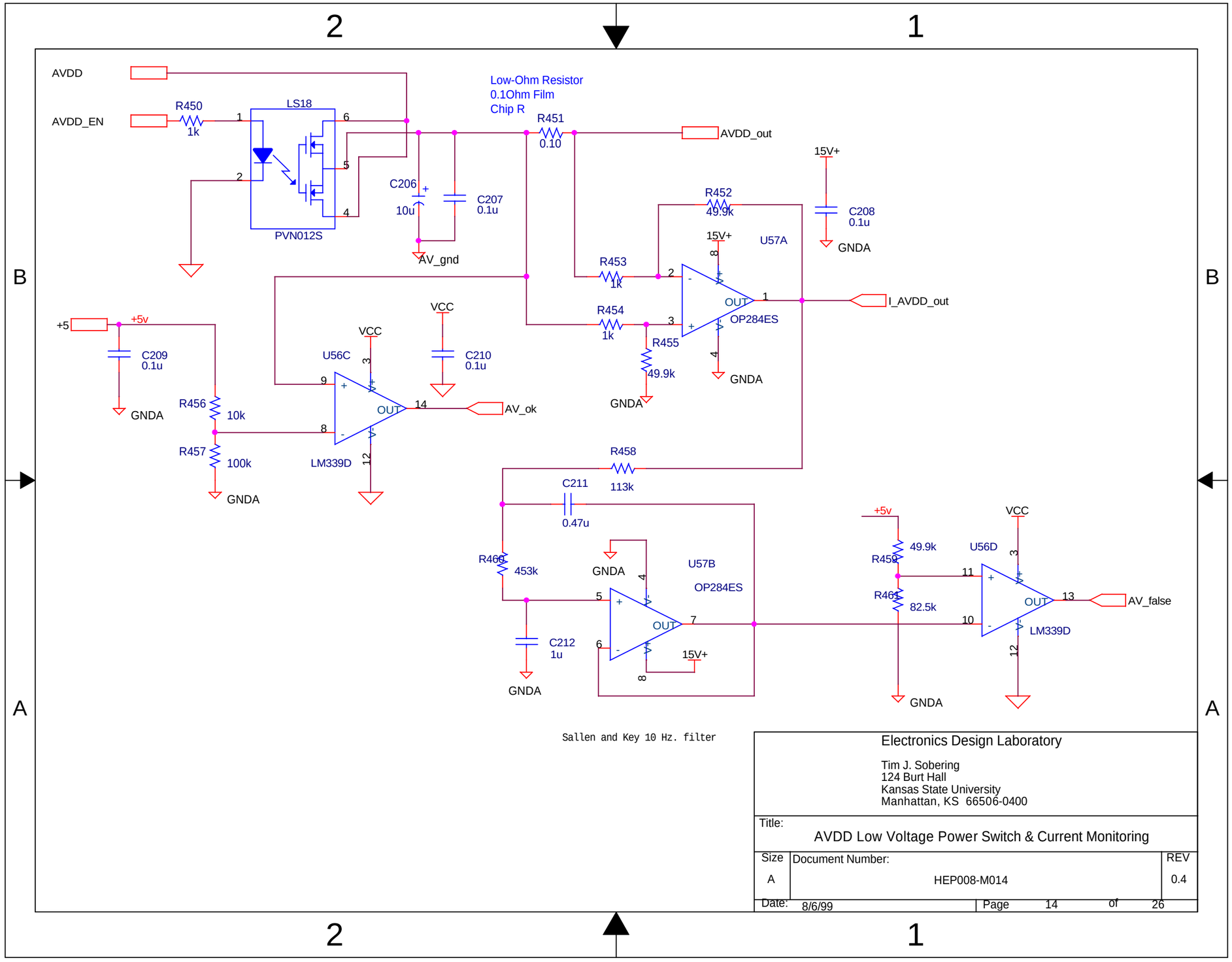

Sallen and Key 10 Hz. filter

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124 Burt Hall
Kansas State University
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Title: AVDD Low Voltage Power Switch & Current Monitoring

Size	Document Number:	REV
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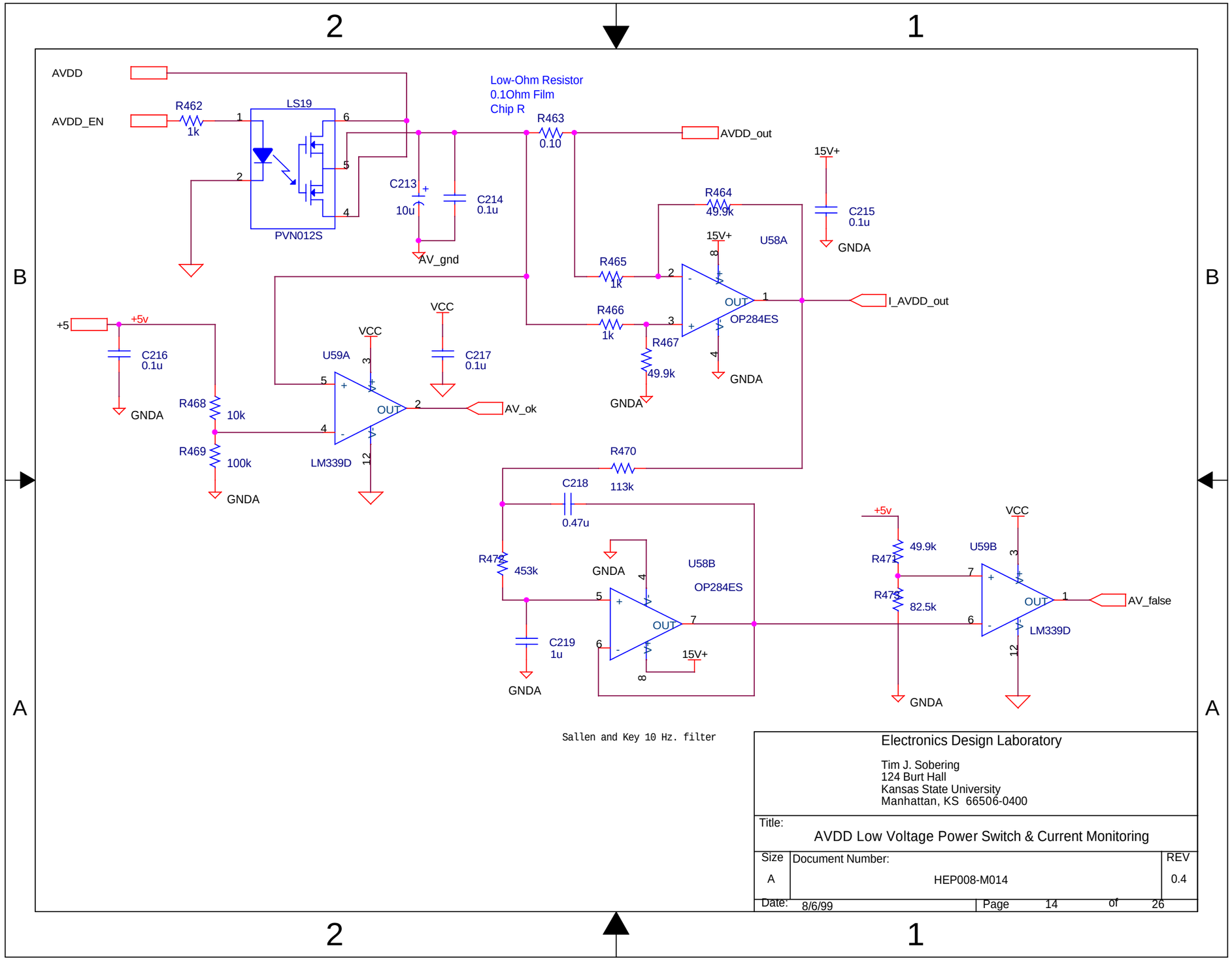

Sallen and Key 10 Hz. filter

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124 Burt Hall
Kansas State University
Manhattan, KS 66506-0400

Title: AVDD Low Voltage Power Switch & Current Monitoring

Size	Document Number:	REV
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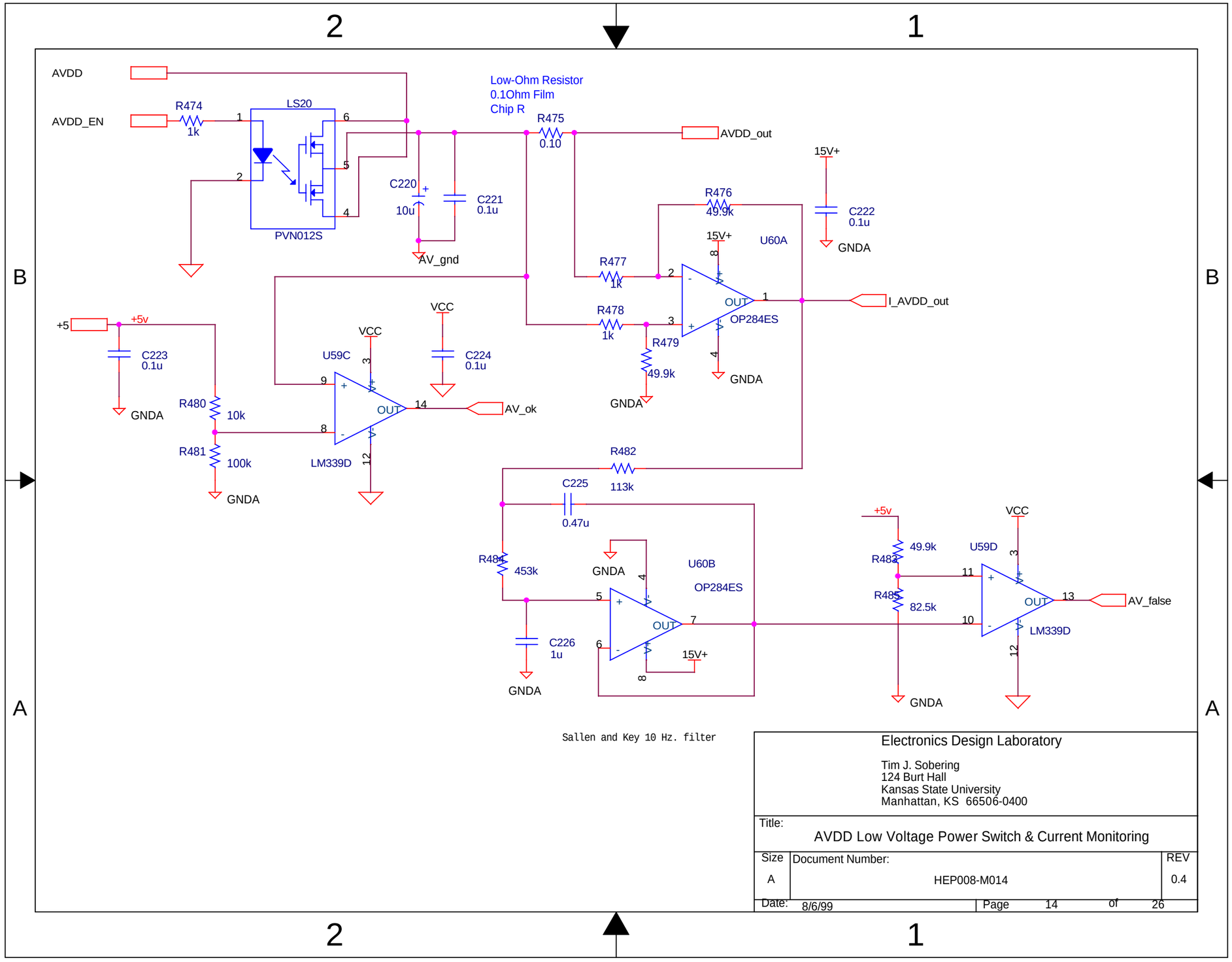

Sallen and Key 10 Hz. filter

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Manhattan, KS 66506-0400

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Size	Document Number:	REV
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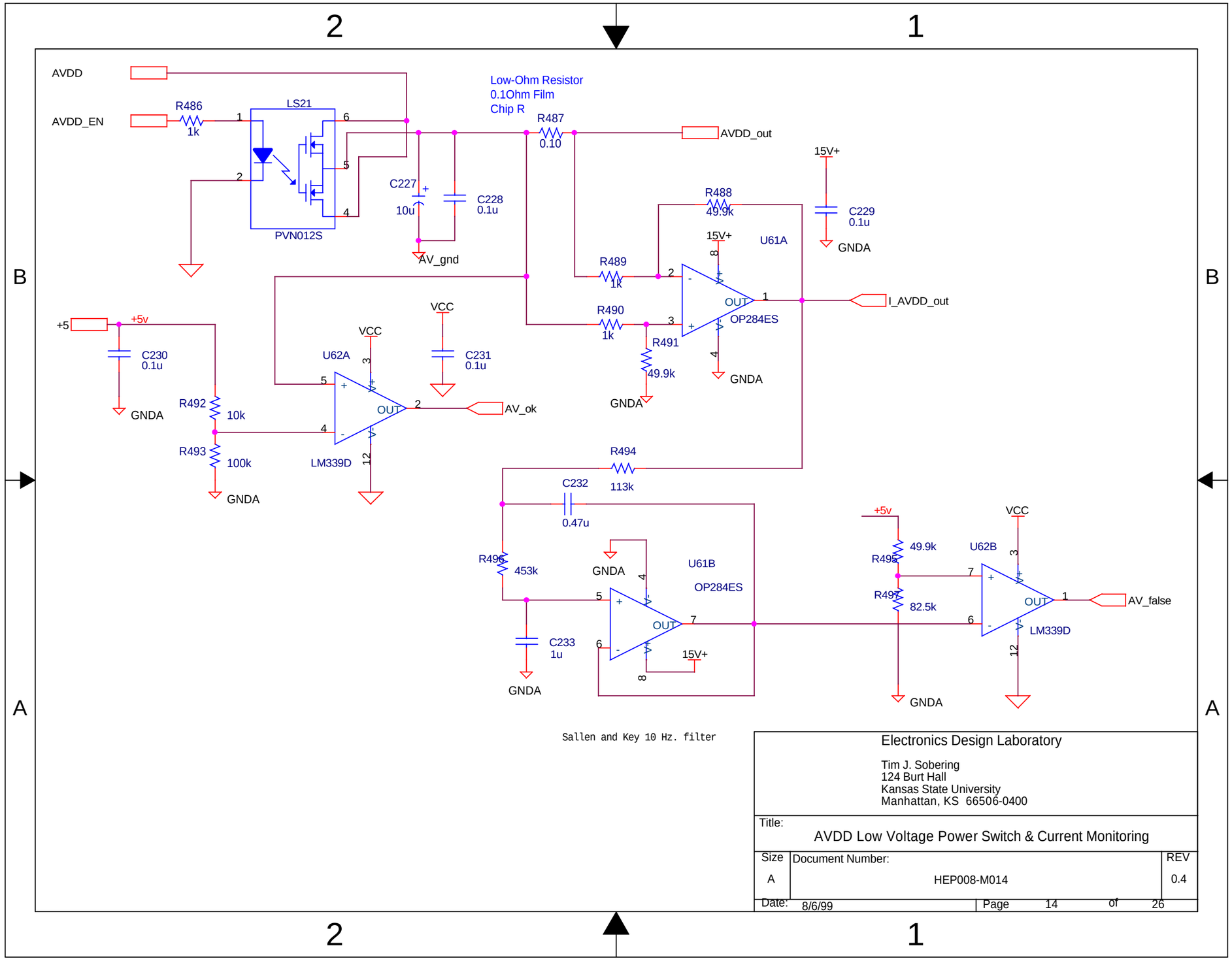

Sallen and Key 10 Hz. filter

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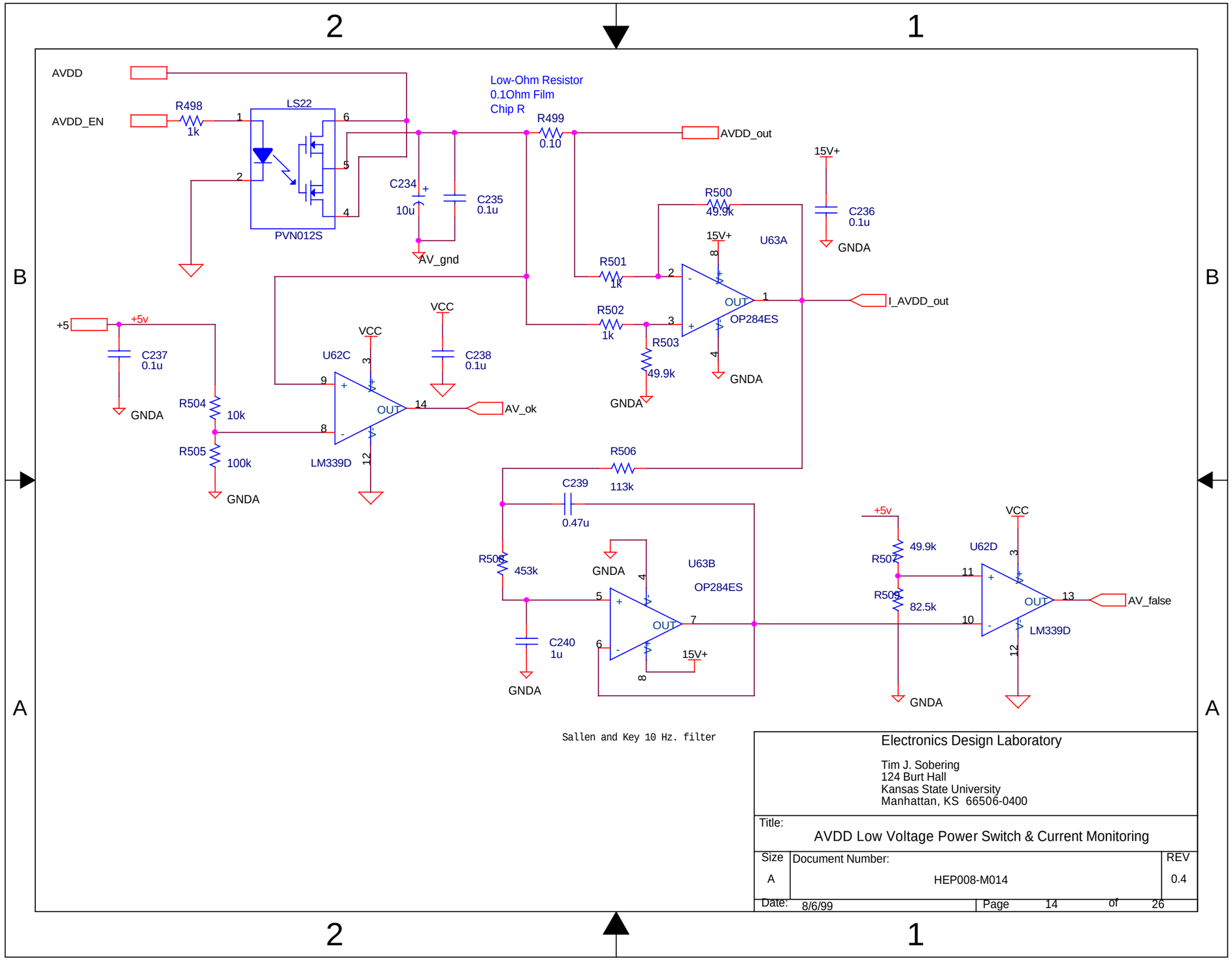
Date: 8/6/99 | Page 14 of 26



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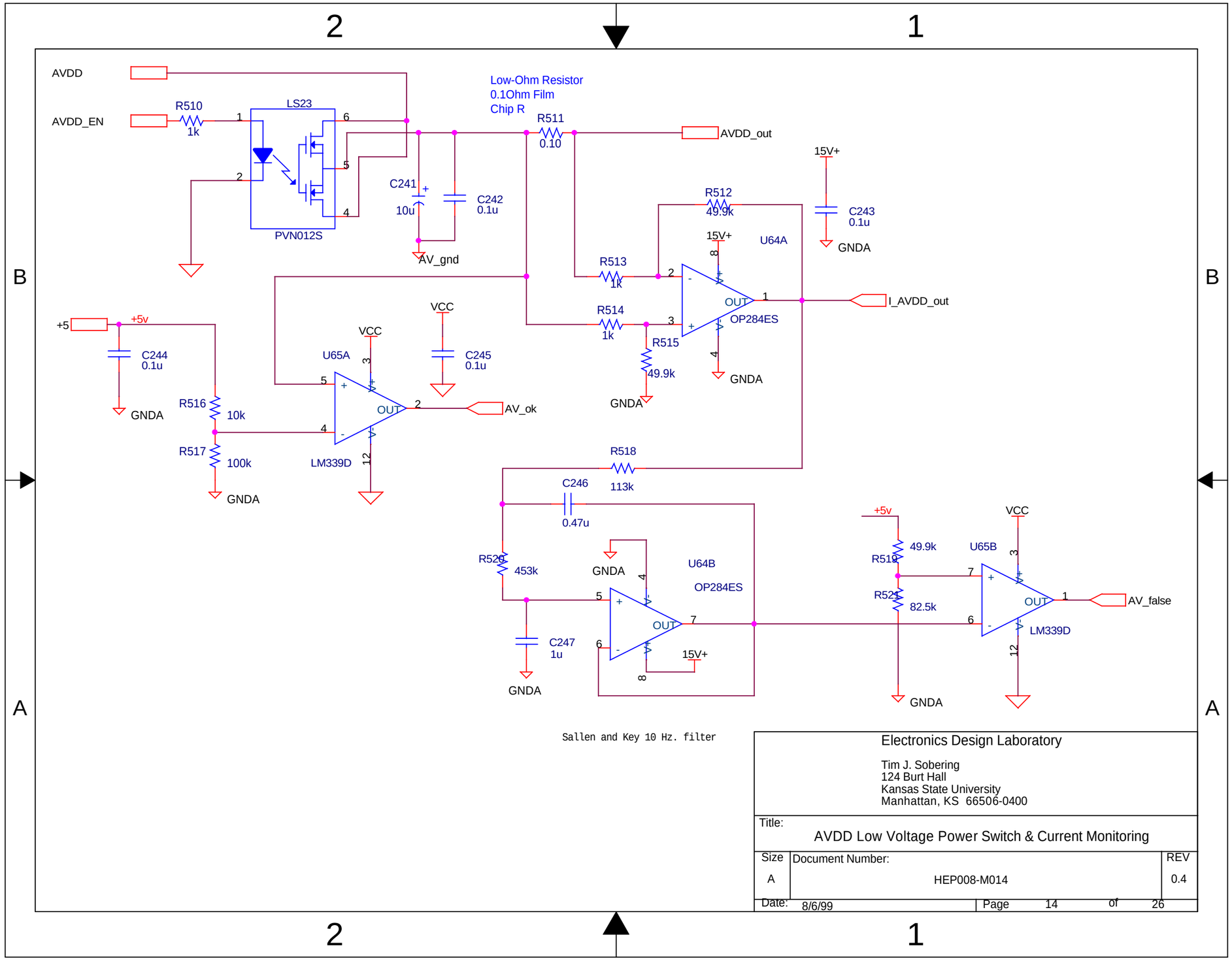

Sallen and Key 10 Hz. filter

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Tim J. Sobering
124 Burt Hall
Kansas State University
Manhattan, KS 66506-0400

Title: AVDD Low Voltage Power Switch & Current Monitoring

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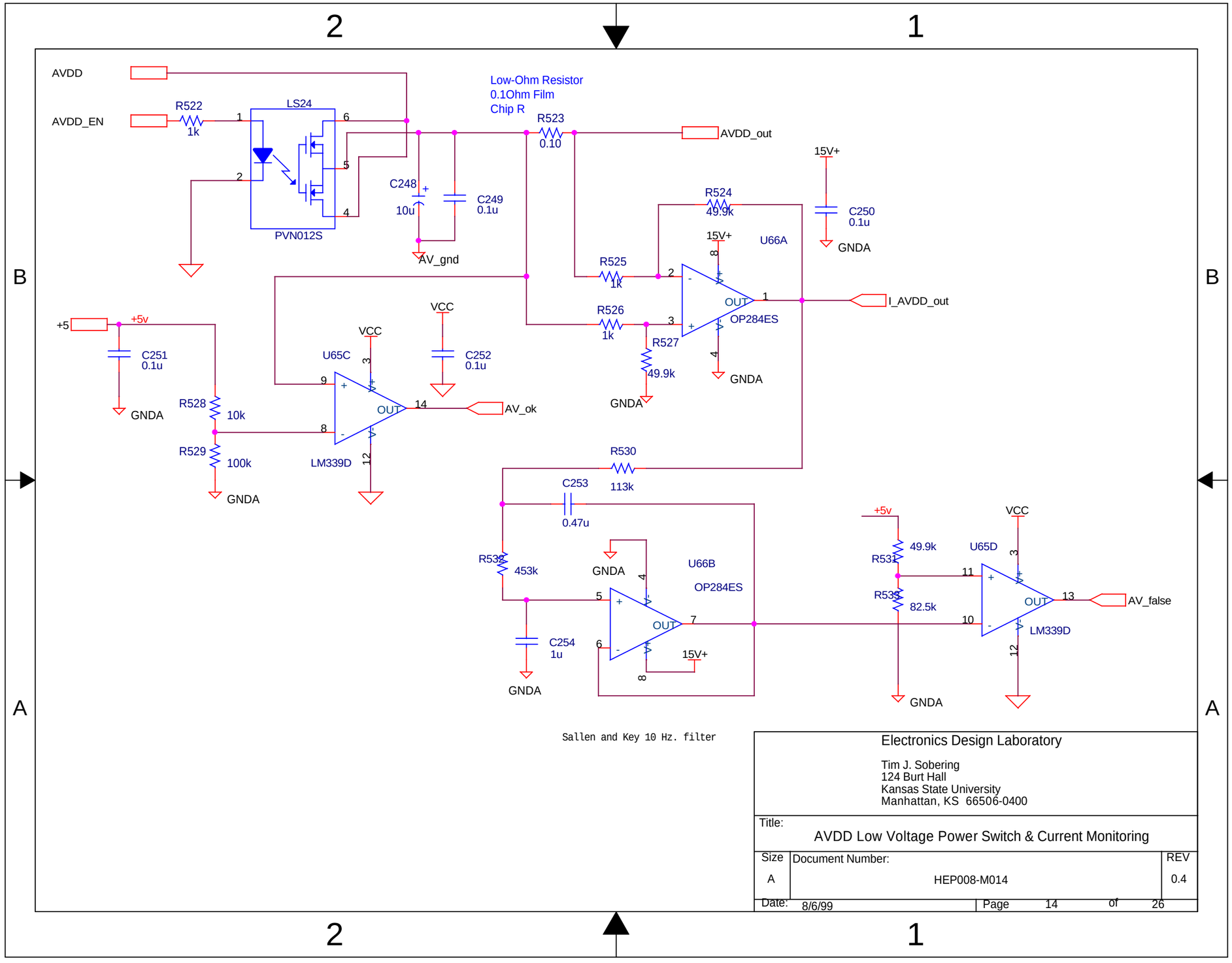
AVDD
AVDD_EN
R522
1k
LS24
PVN012S
Low-Ohm Resistor
0.1Ohm Film
Chip R
R523
0.10
AVDD_out
C248
10u
C249
0.1u
AV_gnd
15V+
C250
0.1u
GNDA
R524
49.9k
U66A
R525
1k
R526
1k
R527
49.9k
OP284ES
I_AVDD_out
+5
+5v
C251
0.1u
R528
10k
R529
100k
VCC
U65C
C252
0.1u
LM339D
AV_ok
R530
113k
C253
0.47u
R532
453k
U66B
OP284ES
C254
1u
R531
49.9k
R533
82.5k
U65D
LM339D
AV_false
Sallen and Key 10 Hz. filter
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Tim J. Sobering
124 Burt Hall
Kansas State University
Manhattan, KS 66506-0400
Title:
AVDD Low Voltage Power Switch & Current Monitoring
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A
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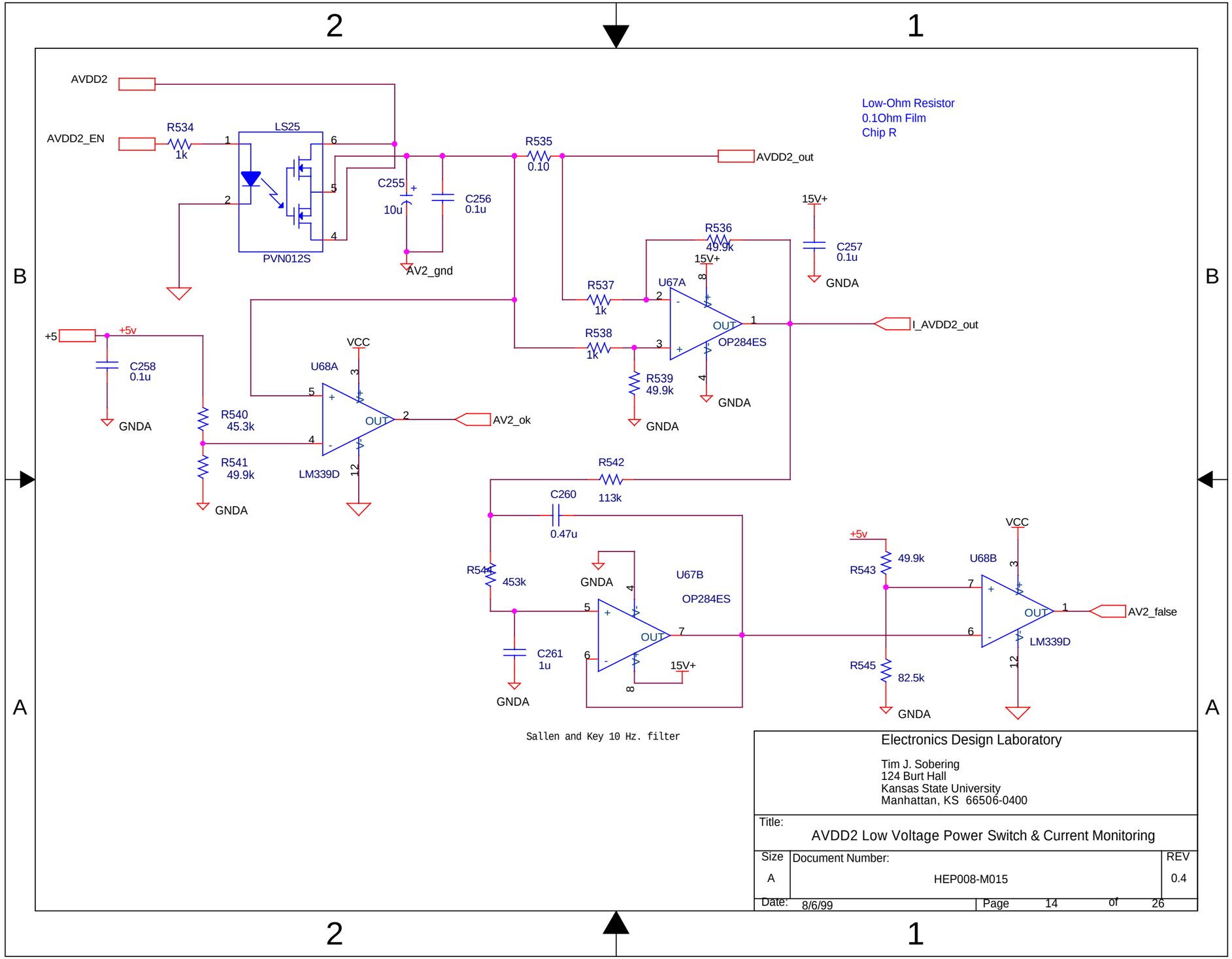

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Tim J. Sobering
124 Burt Hall
Kansas State University
Manhattan, KS 66506-0400

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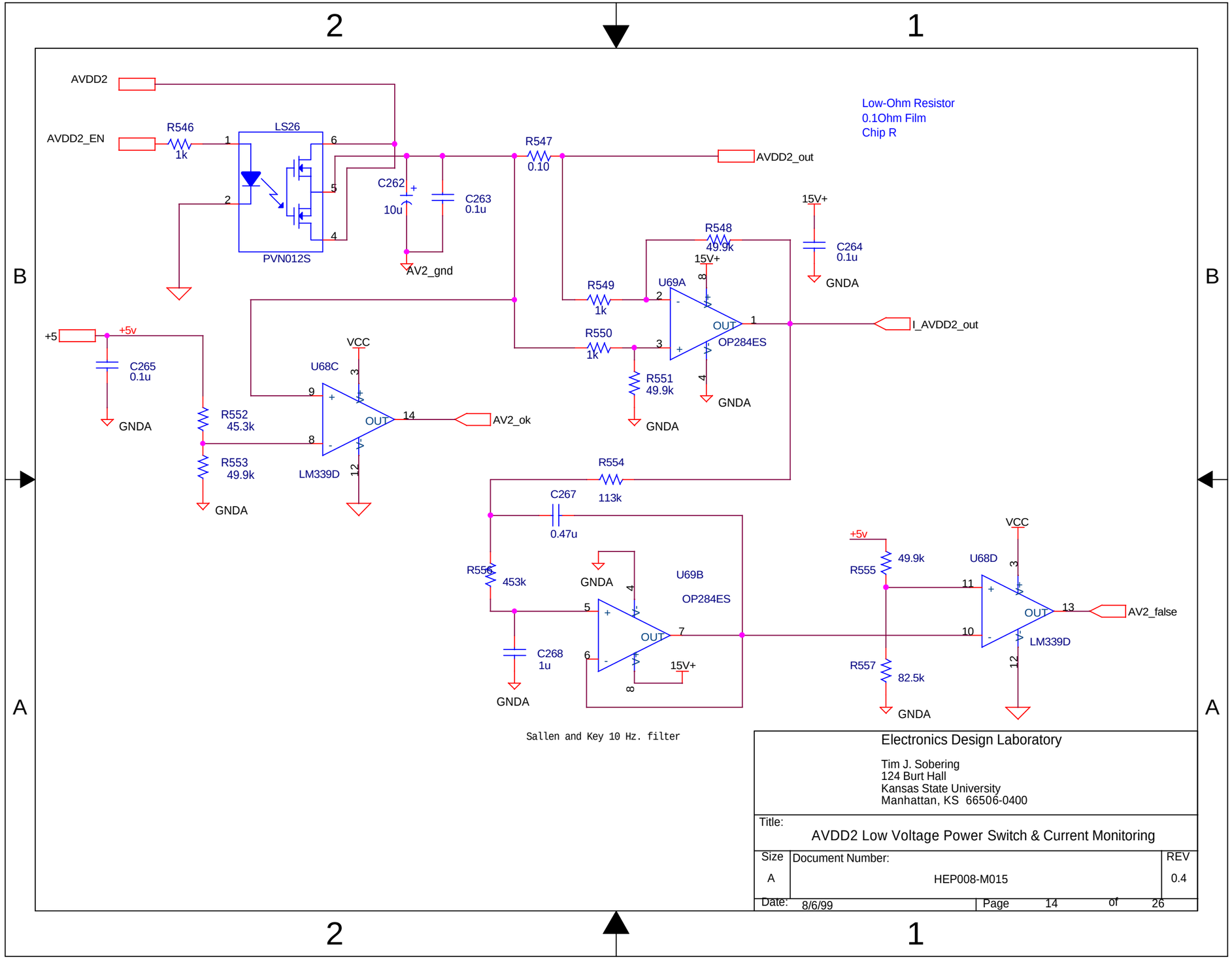
AVDD2
AVDD2_EN
R546
1k
LS26
PVN012S
C262
10u
C263
0.1u
AV2_gnd
R547
0.10
AVDD2_out
Low-Ohm Resistor
0.1Ohm Film
Chip R
15V+
C264
0.1u
GNDA
R548
49.9k
R549
1k
U69A
OP284ES
R550
1k
R551
49.9k
I_AVDD2_out
+5
+5v
C265
0.1u
R552
45.3k
R553
49.9k
U68C
LM339D
VCC
AV2_ok
R554
113k
C267
0.47u
R556
453k
U69B
OP284ES
C268
1u
R555
49.9k
U68D
LM339D
R557
82.5k
AV2_false
Sallen and Key 10 Hz. filter
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124 Burt Hall
Kansas State University
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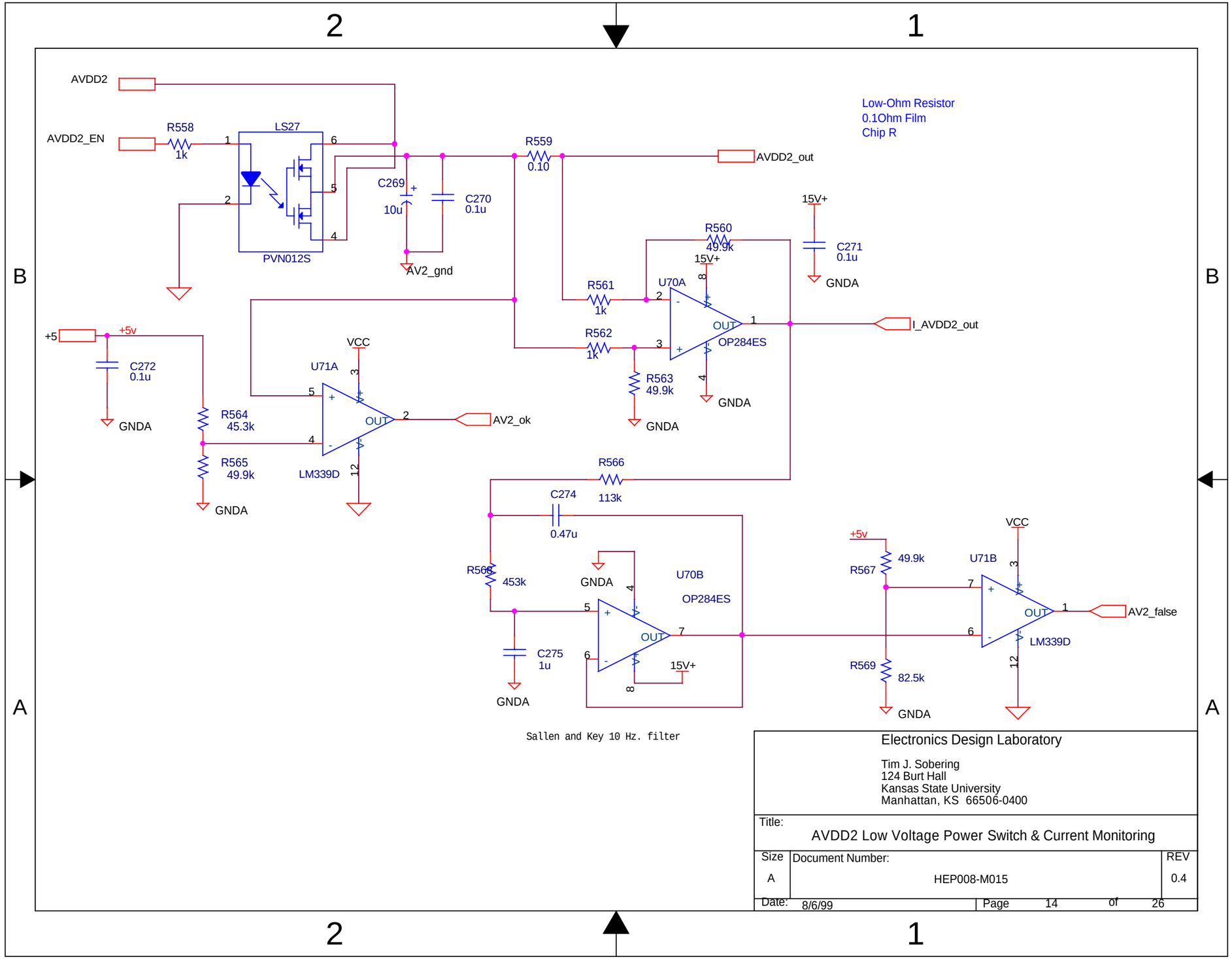

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124 Burt Hall
Kansas State University
Manhattan, KS 66506-0400

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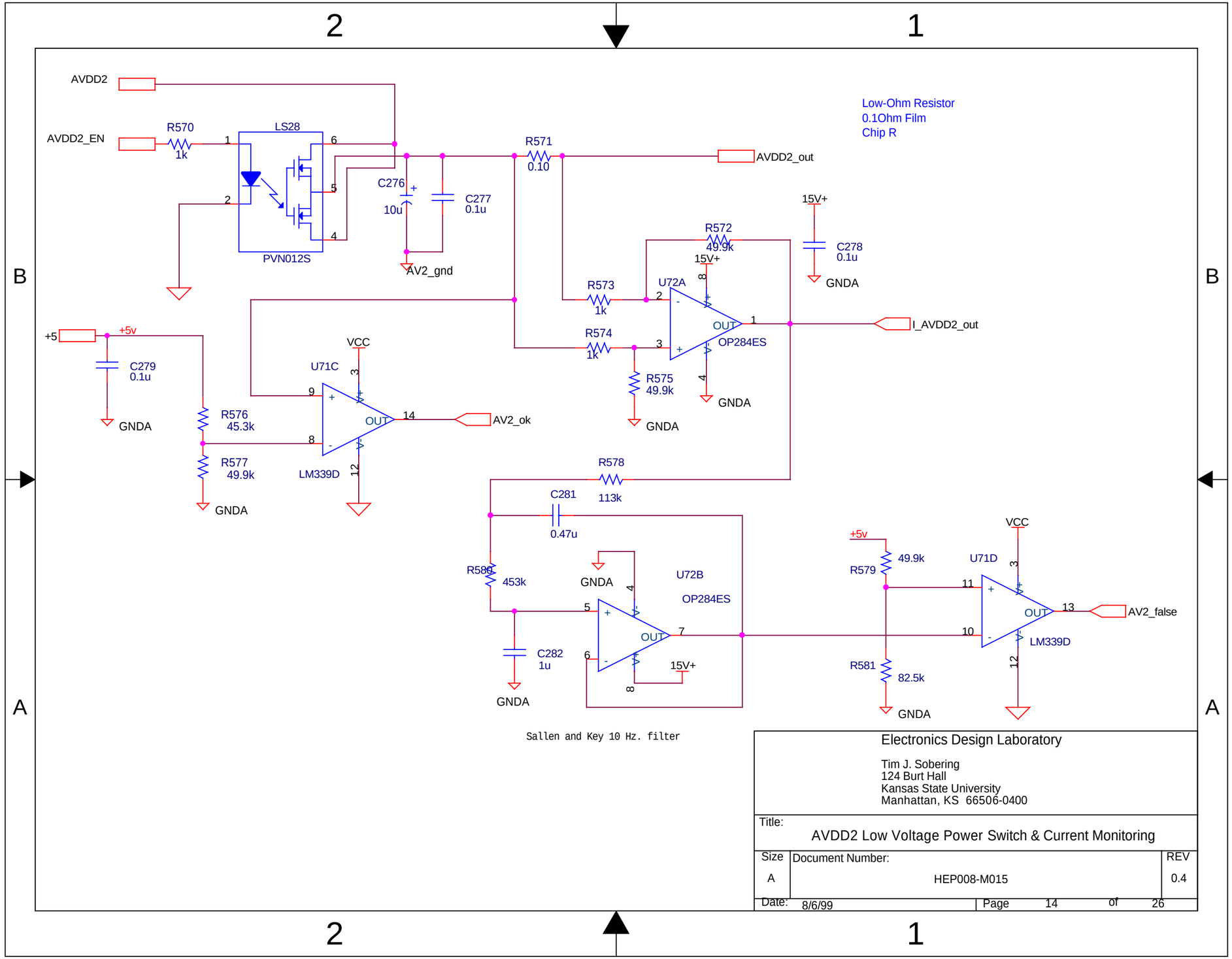

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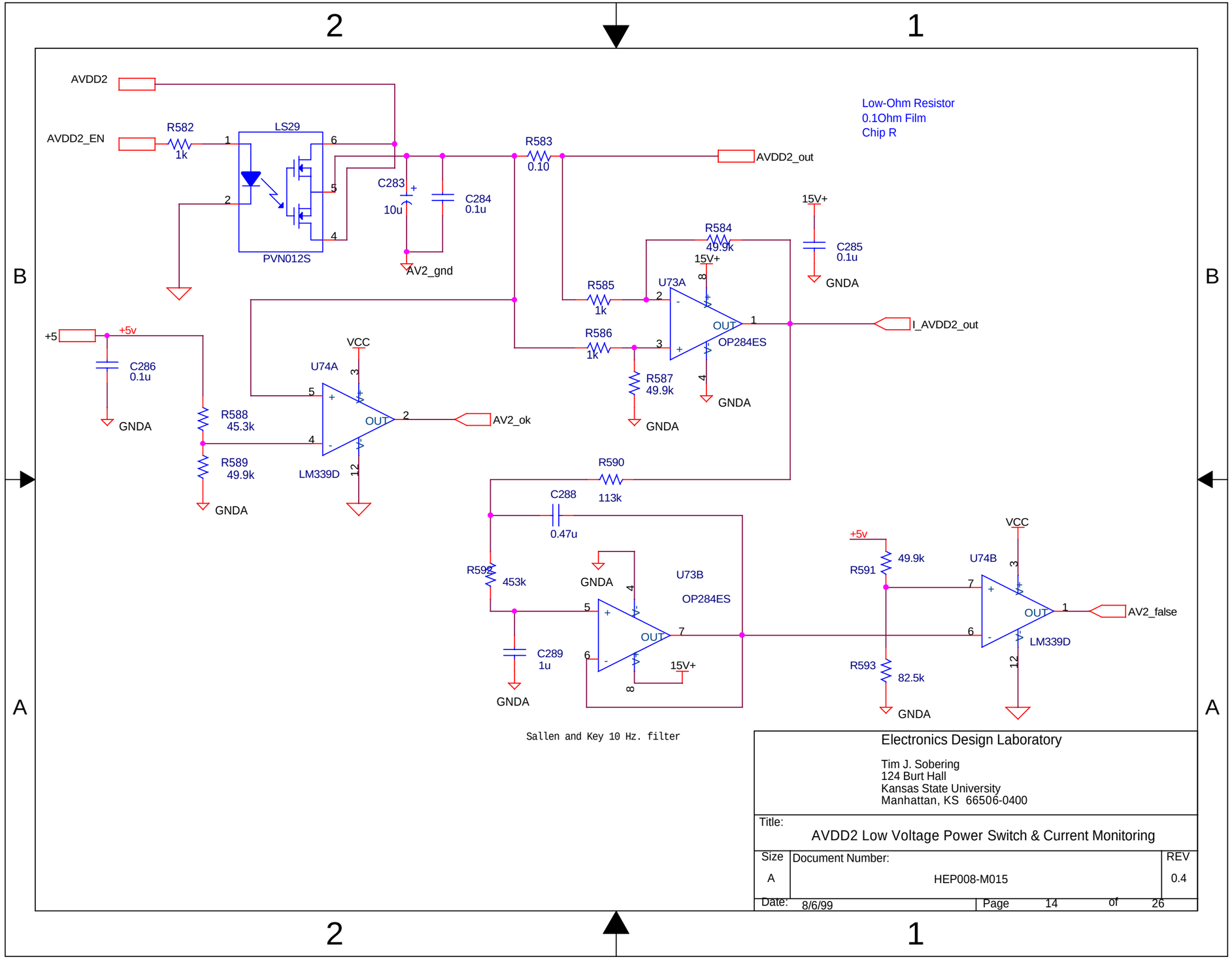

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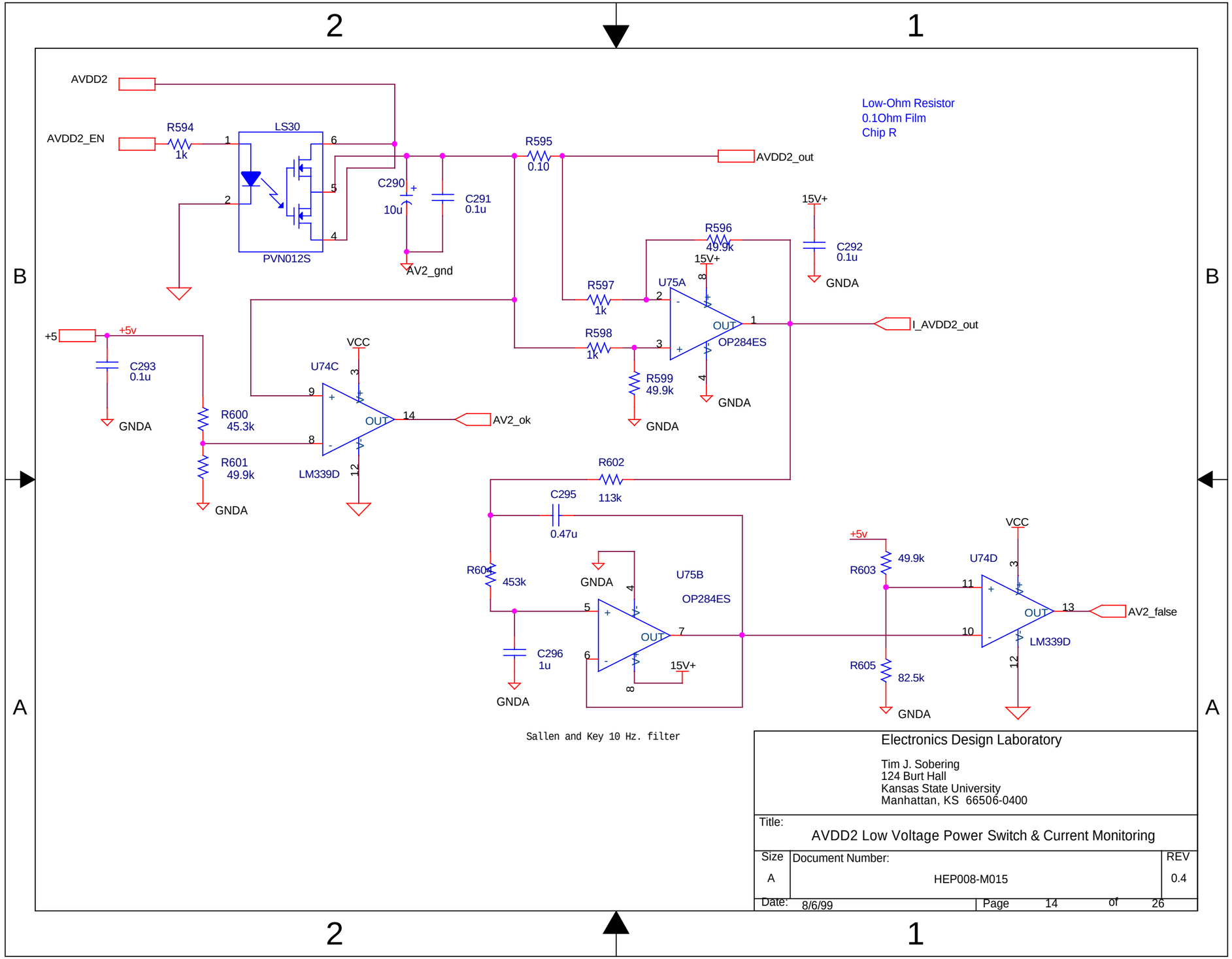

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Manhattan, KS 66506-0400

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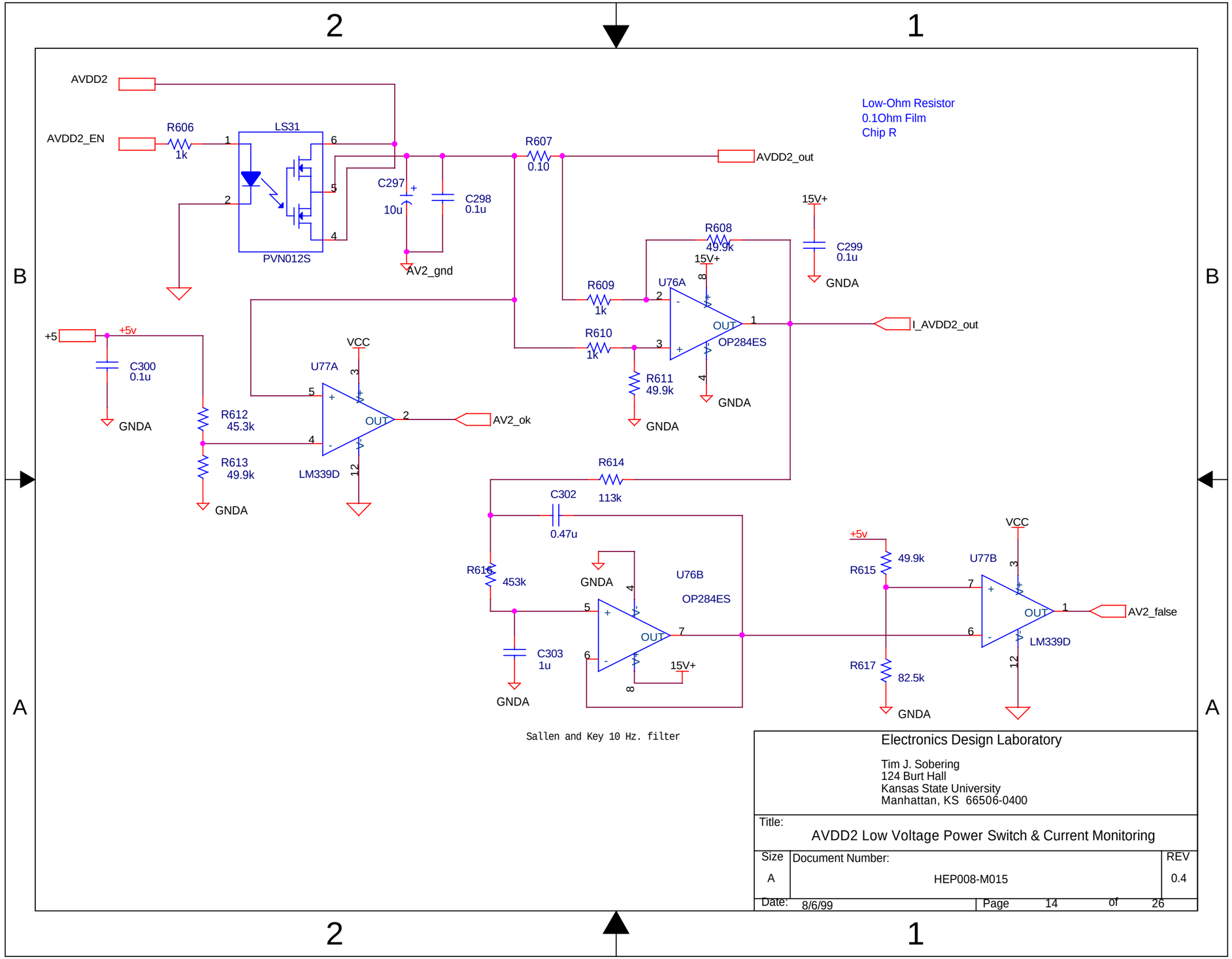

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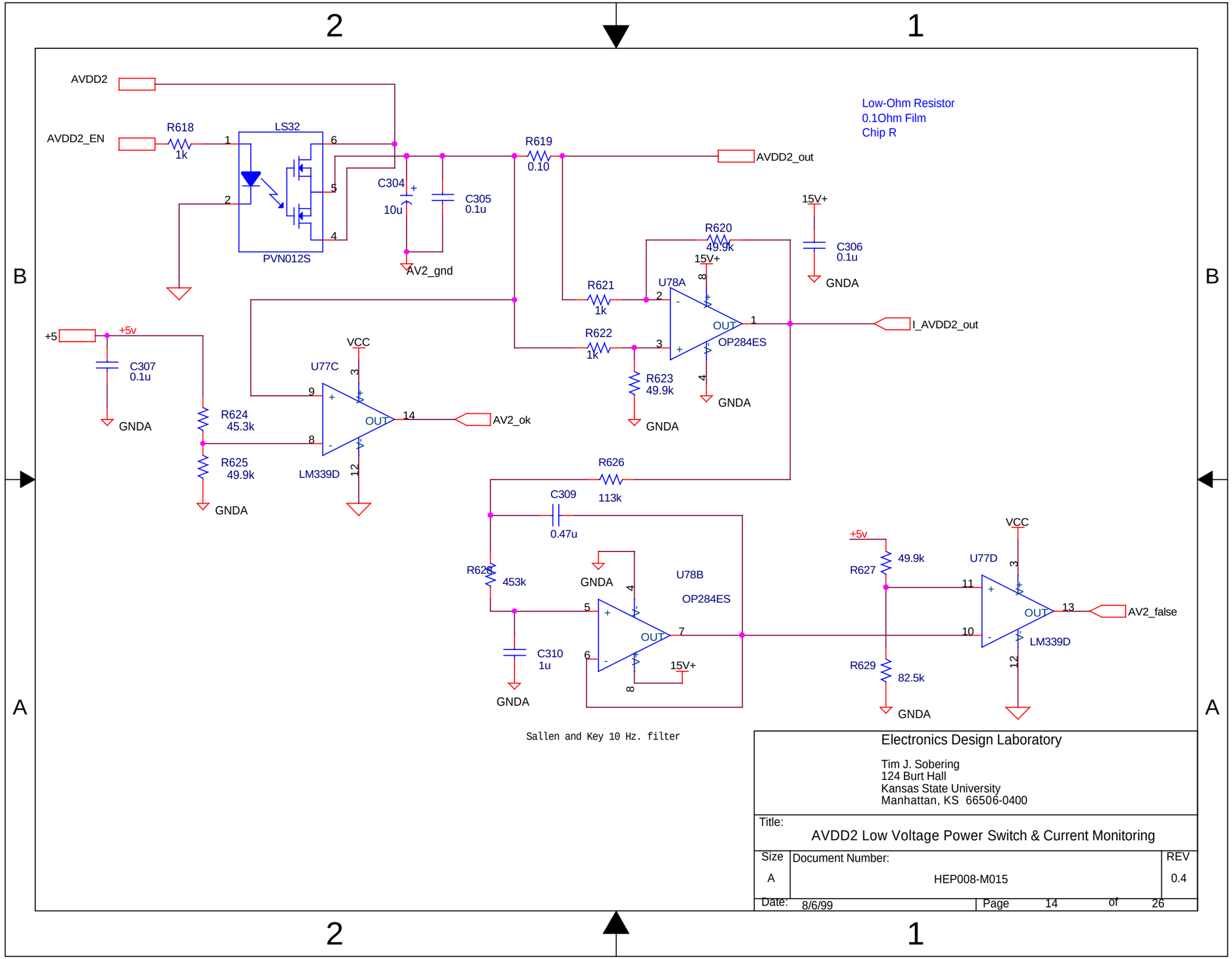

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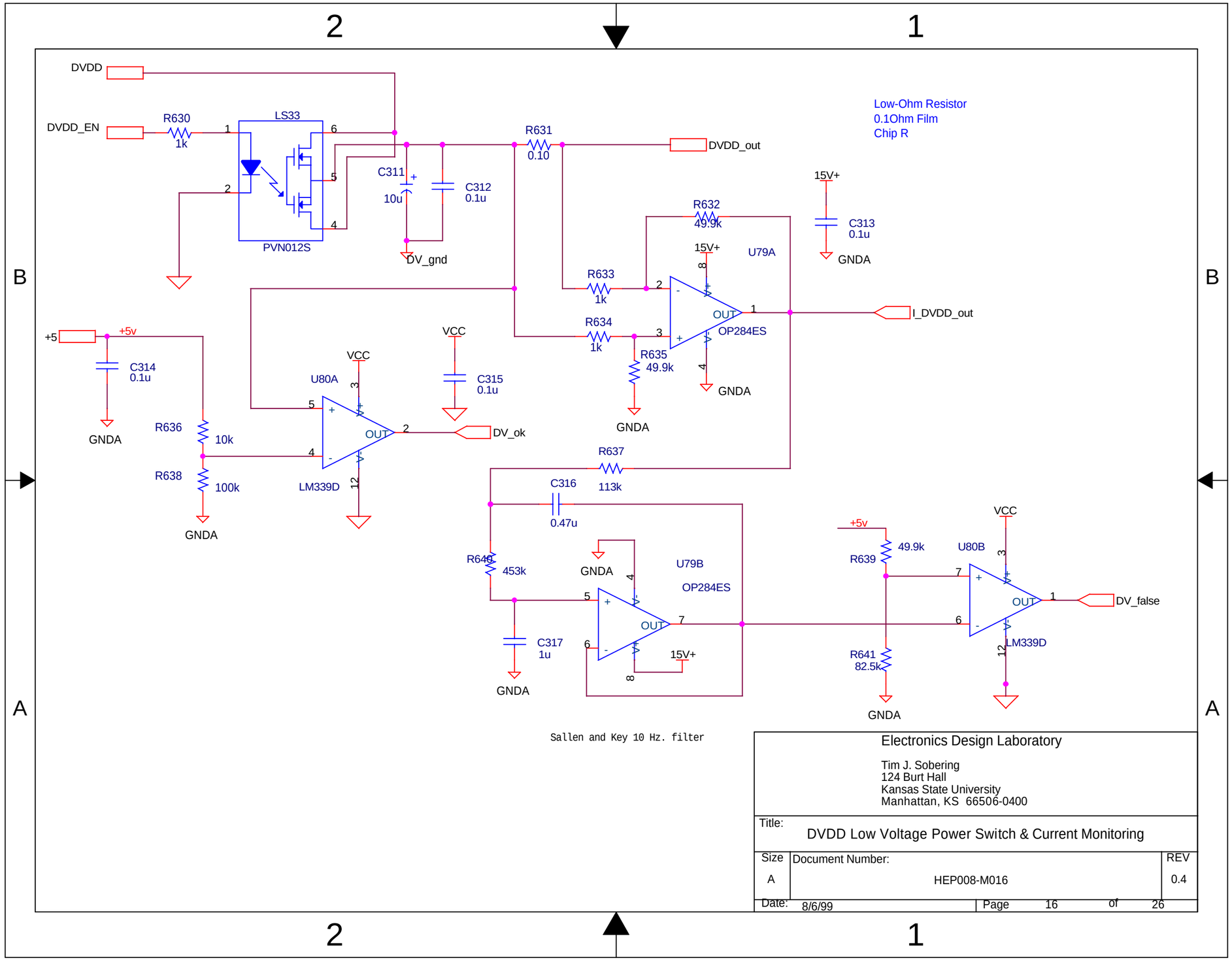

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Tim J. Sobering
124 Burt Hall
Kansas State University
Manhattan, KS 66506-0400

Title: DVDD Low Voltage Power Switch & Current Monitoring

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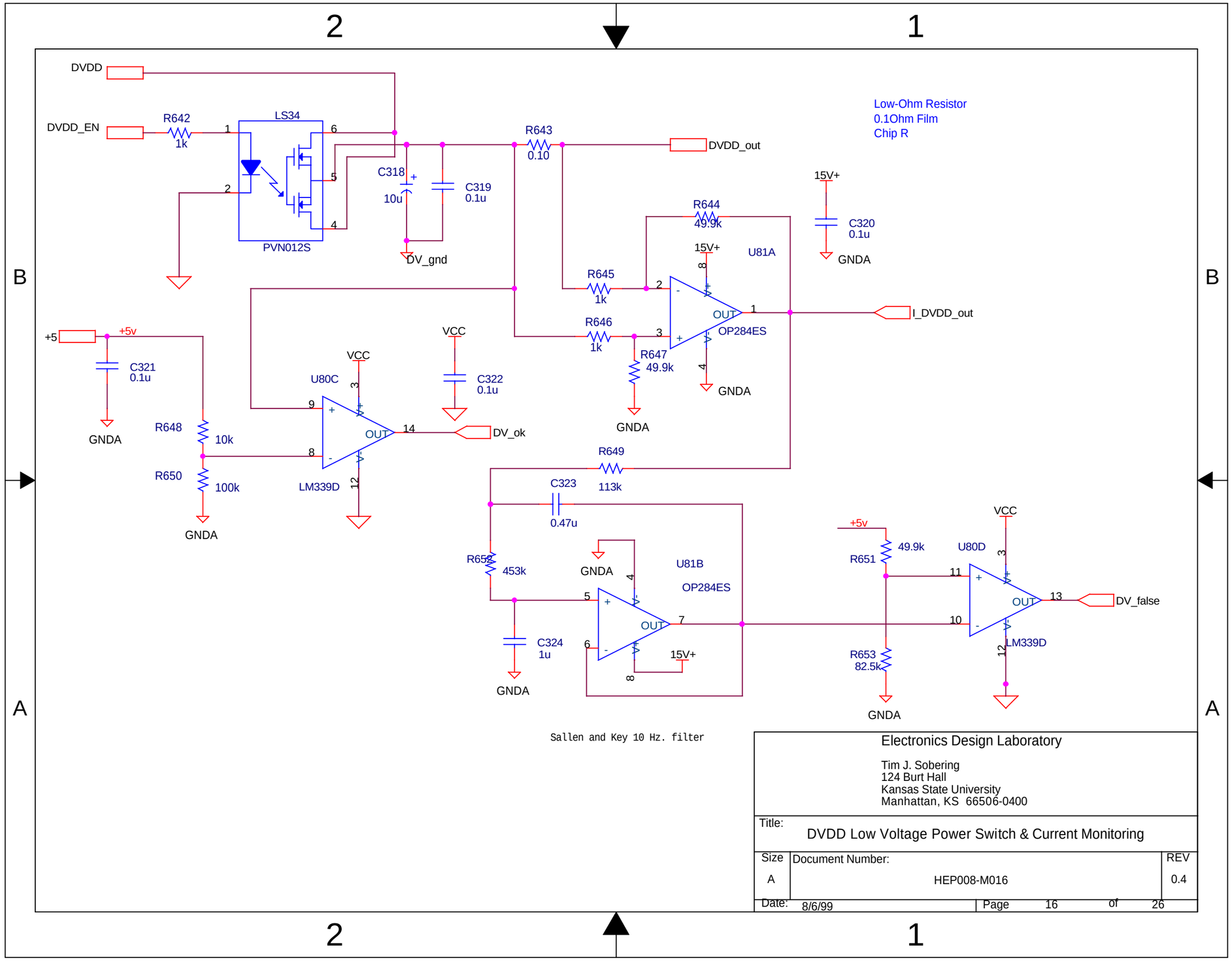

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124 Burt Hall
Kansas State University
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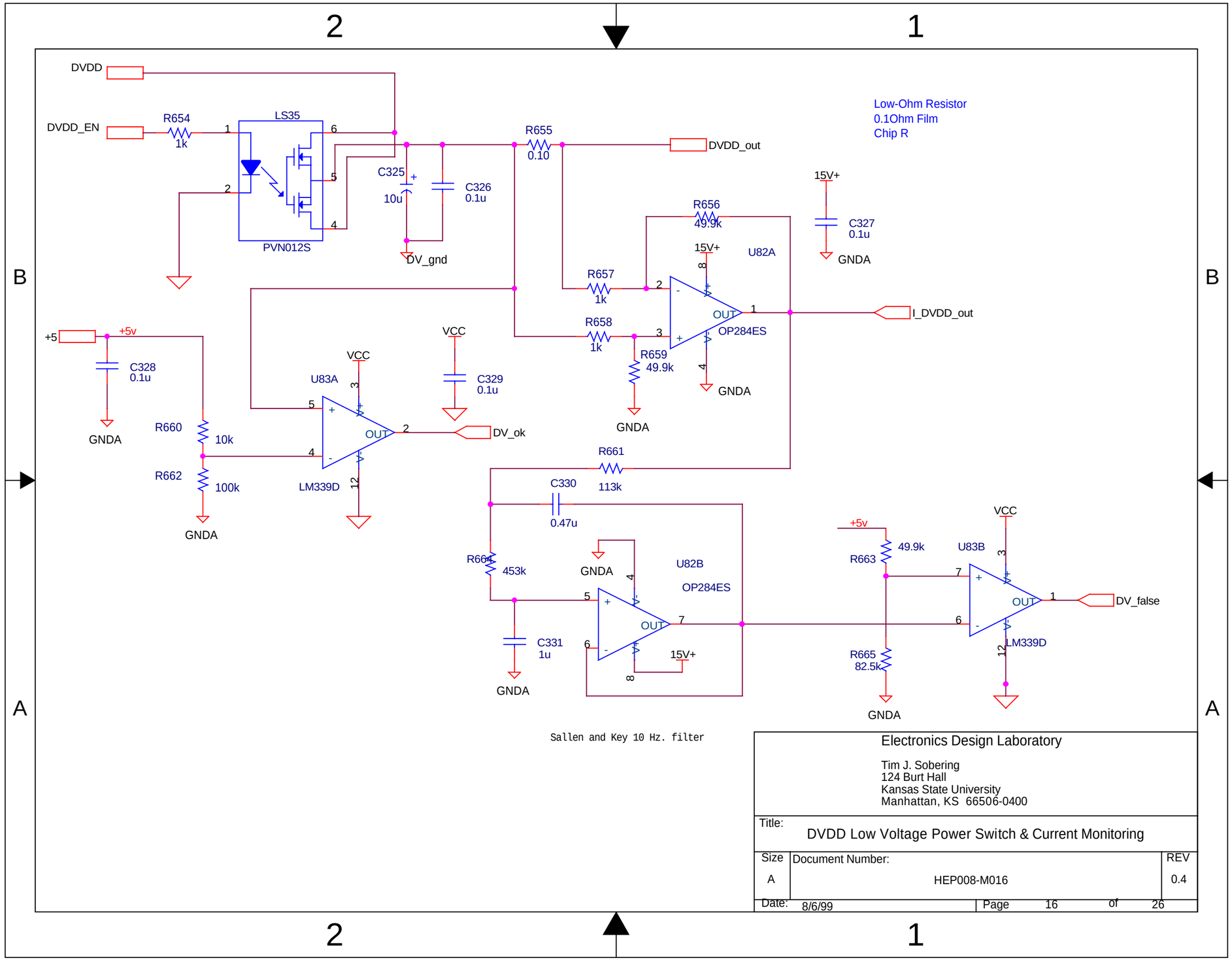

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124 Burt Hall
Kansas State University
Manhattan, KS 66506-0400

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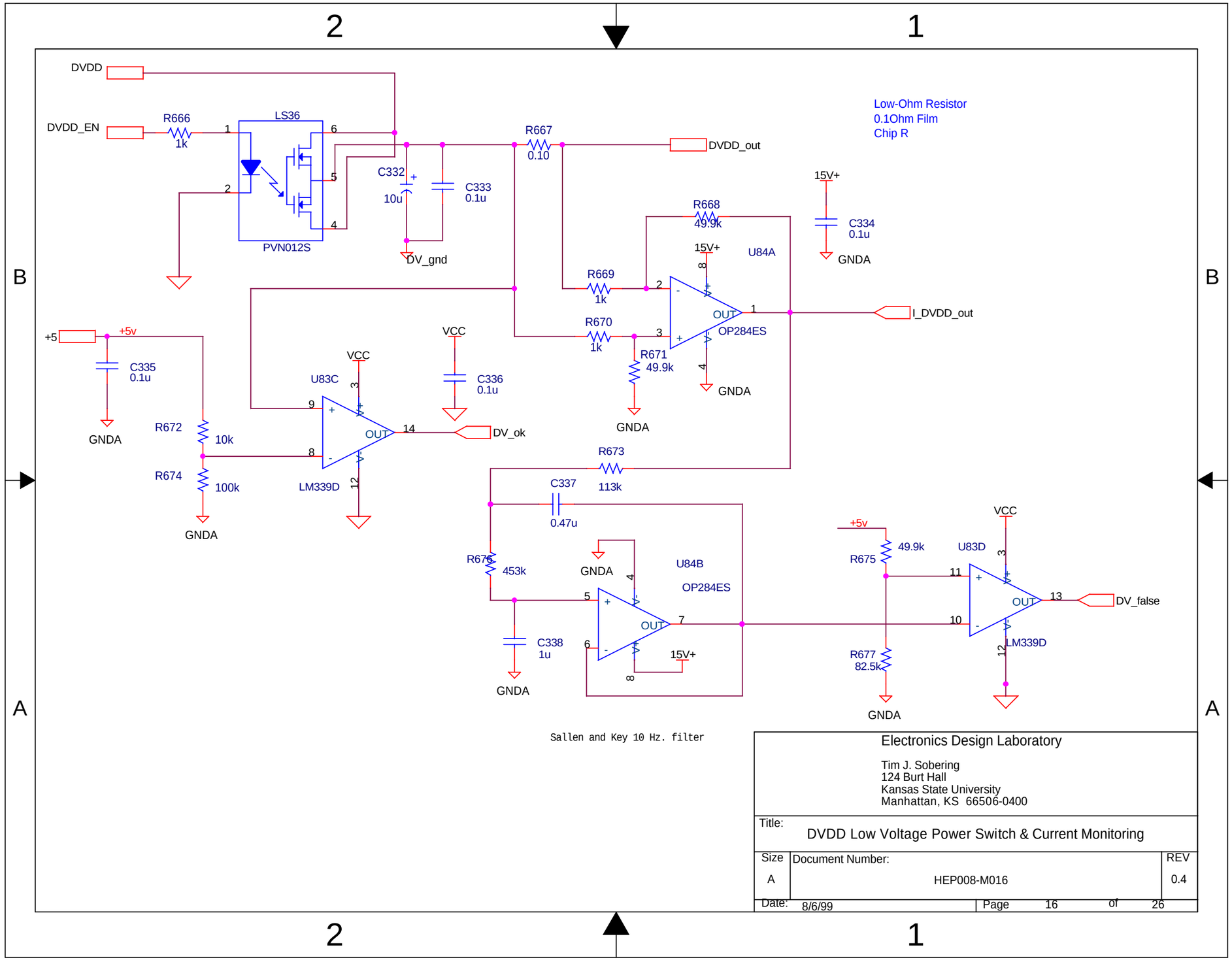
DVDD
DVDD_EN
R666
1k
LS36
PVN012S
C332
10u
C333
0.1u
DV_gnd
R667
0.10
DVDD_out
Low-Ohm Resistor
0.1Ohm Film
Chip R
15V+
C334
0.1u
GNDA
R668
49.9k
U84A
R669
1k
R670
1k
R671
49.9k
OP284ES
I_DVDD_out
+5
+5v
C335
0.1u
VCC
U83C
C336
0.1u
R672
10k
R674
100k
LM339D
DV_ok
R673
113k
C337
0.47u
R676
453k
U84B
OP284ES
C338
1u
15V+
49.9k
R675
U83D
R677
82.5k
LM339D
DV_false
Sallen and Key 10 Hz. filter
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Tim J. Sobering
124 Burt Hall
Kansas State University
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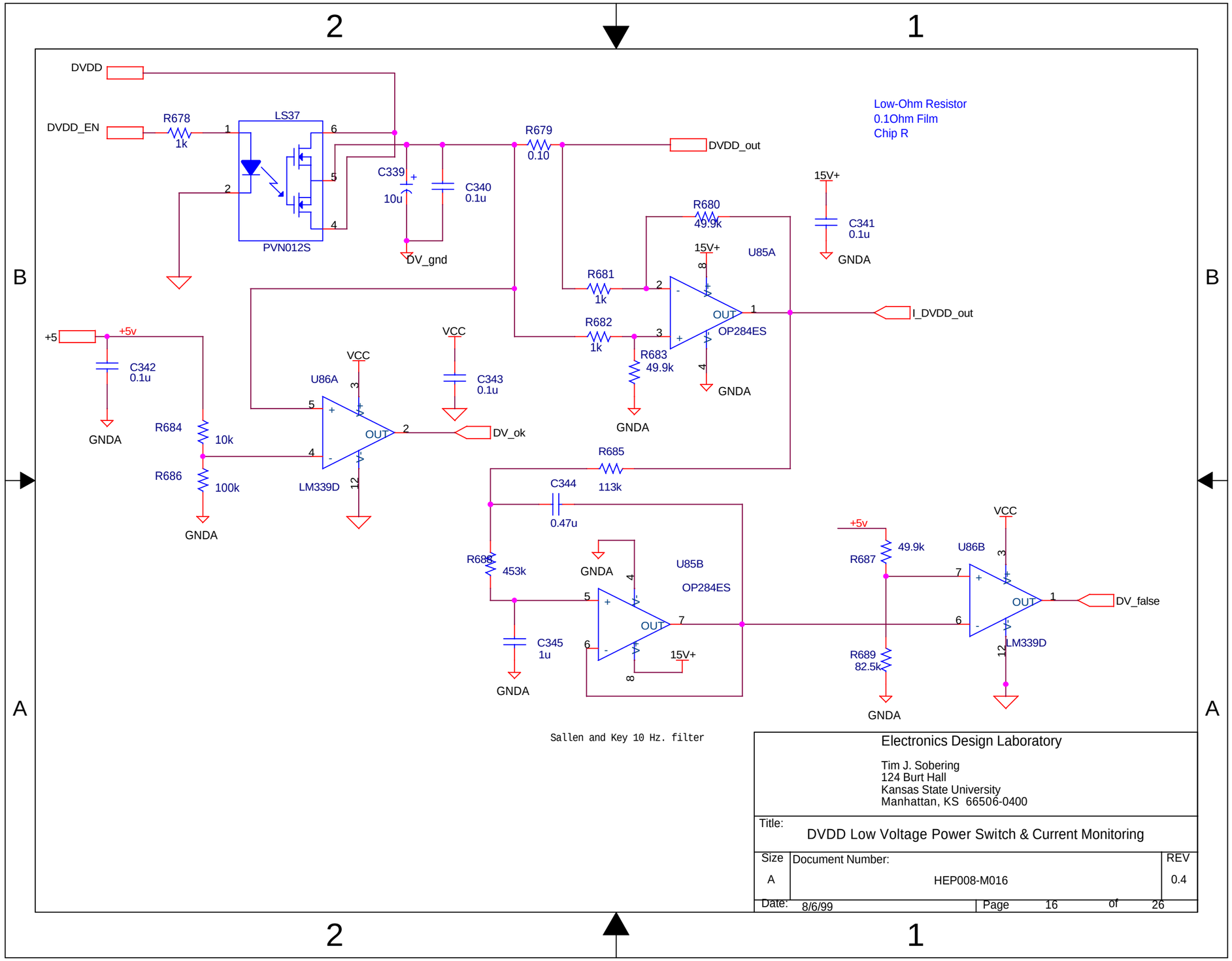
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DVDD_EN
R678
1k
LS37
PVN012S
C339
10u
C340
0.1u
DV_gnd
R679
0.10
DVDD_out
Low-Ohm Resistor
0.1Ohm Film
Chip R
15V+
C341
0.1u
GNDA
R680
49.9k
U85A
R681
1k
R682
1k
R683
49.9k
OP284ES
I_DVDD_out
+5
+5v
C342
0.1u
VCC
C343
0.1u
U86A
LM339D
DV_ok
R684
10k
R686
100k
R685
113k
C344
0.47u
R688
453k
U85B
OP284ES
C345
1u
R687
49.9k
U86B
LM339D
DV_false
R689
82.5k
Sallen and Key 10 Hz. filter
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124 Burt Hall
Kansas State University
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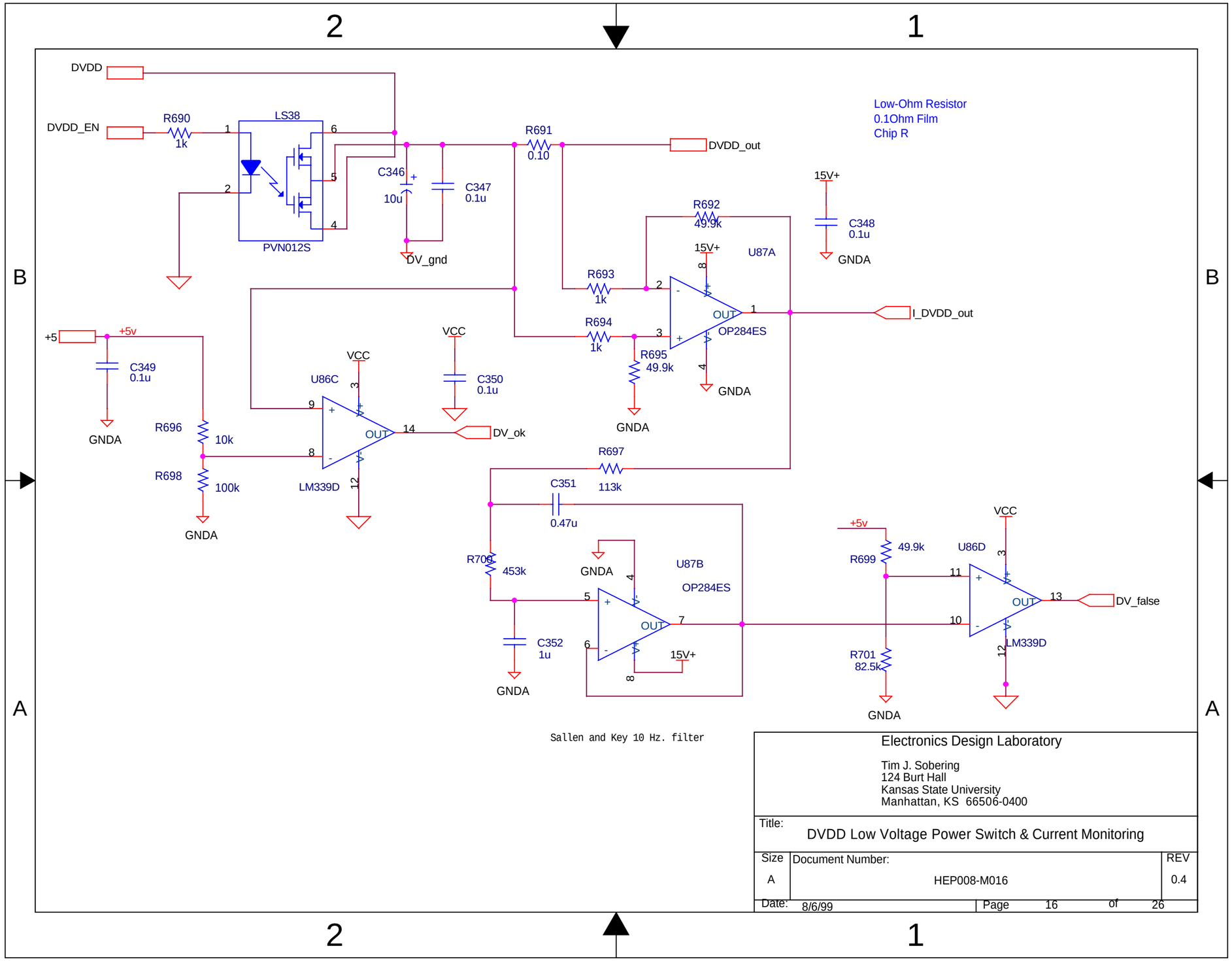
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DVDD_EN
R690
1k
LS38
PVN012S
C346
10u
C347
0.1u
DV_gnd
R691
0.10
DVDD_out
Low-Ohm Resistor
0.1Ohm Film
Chip R
15V+
C348
0.1u
GNDA
R692
49.9k
U87A
R693
1k
R694
1k
R695
49.9k
OP284ES
I_DVDD_out
+5
+5v
C349
0.1u
VCC
C350
0.1u
U86C
LM339D
R696
10k
R698
100k
DV_ok
R697
113k
C351
0.47u
R700
453k
U87B
OP284ES
C352
1u
15V+
R699
49.9k
U86D
LM339D
R701
82.5k
DV_false
Sallen and Key 10 Hz. filter
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Tim J. Sobering
124 Burt Hall
Kansas State University
Manhattan, KS 66506-0400
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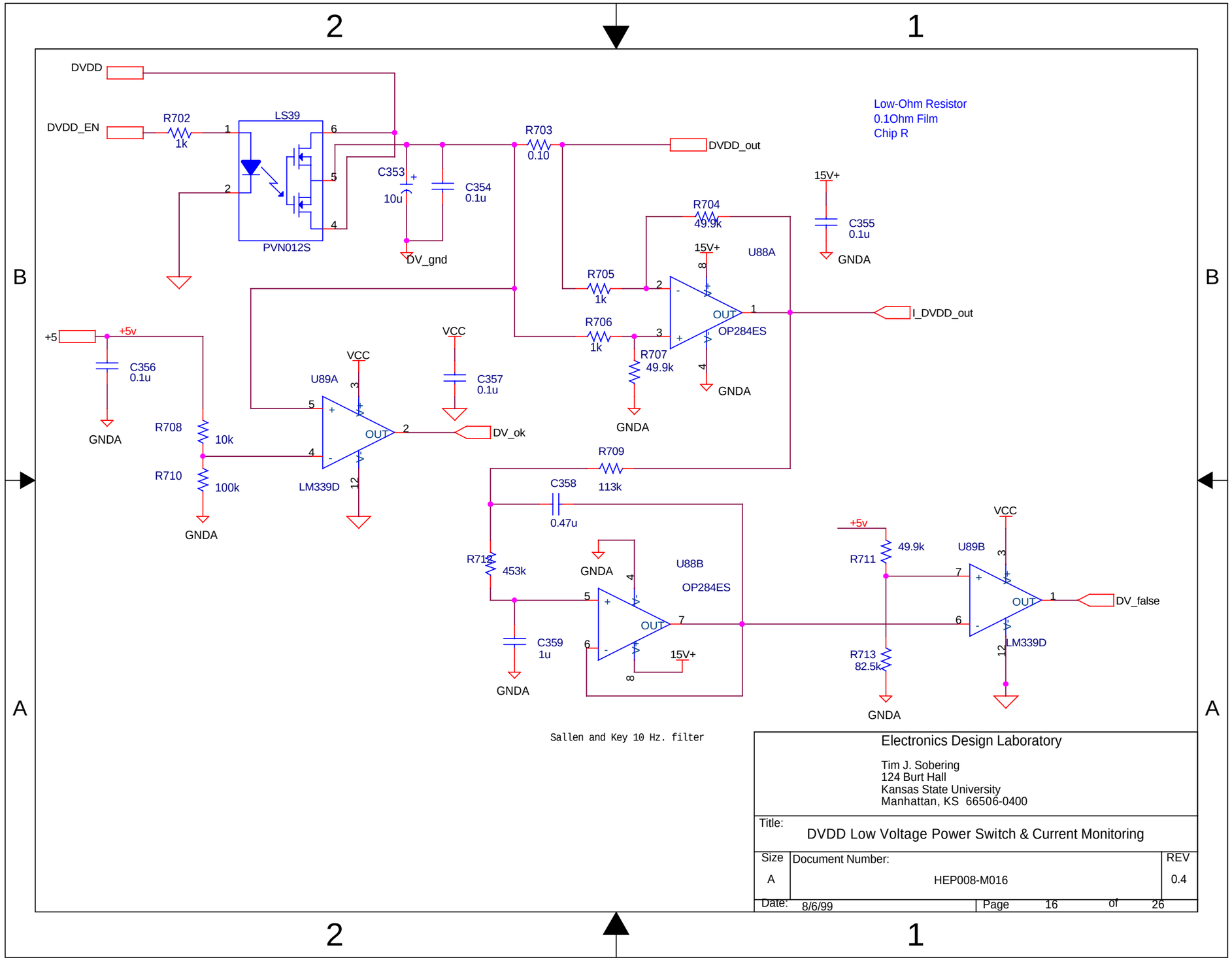

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124 Burt Hall
Kansas State University
Manhattan, KS 66506-0400

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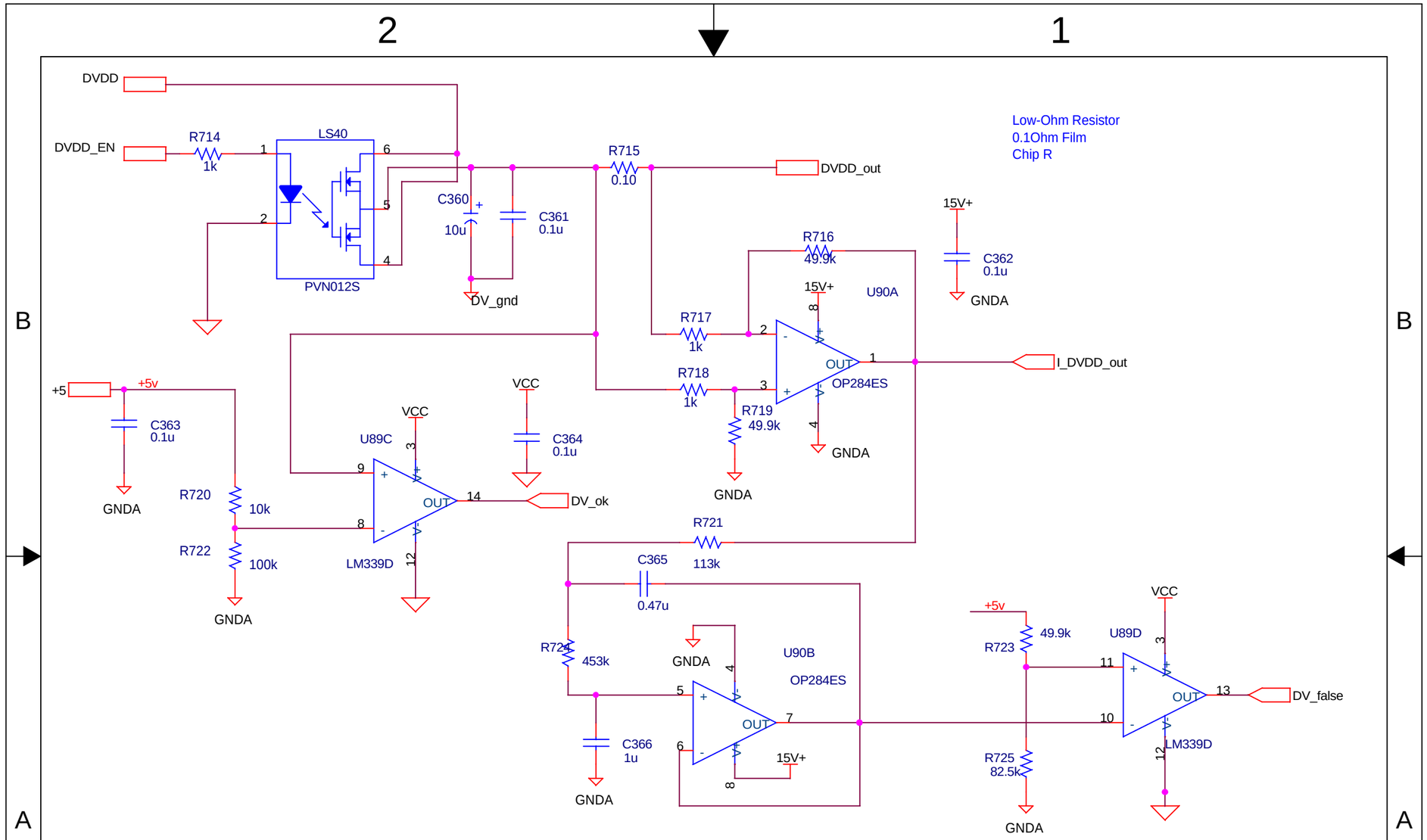

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124 Burt Hall
Kansas State University
Manhattan, KS 66506-0400

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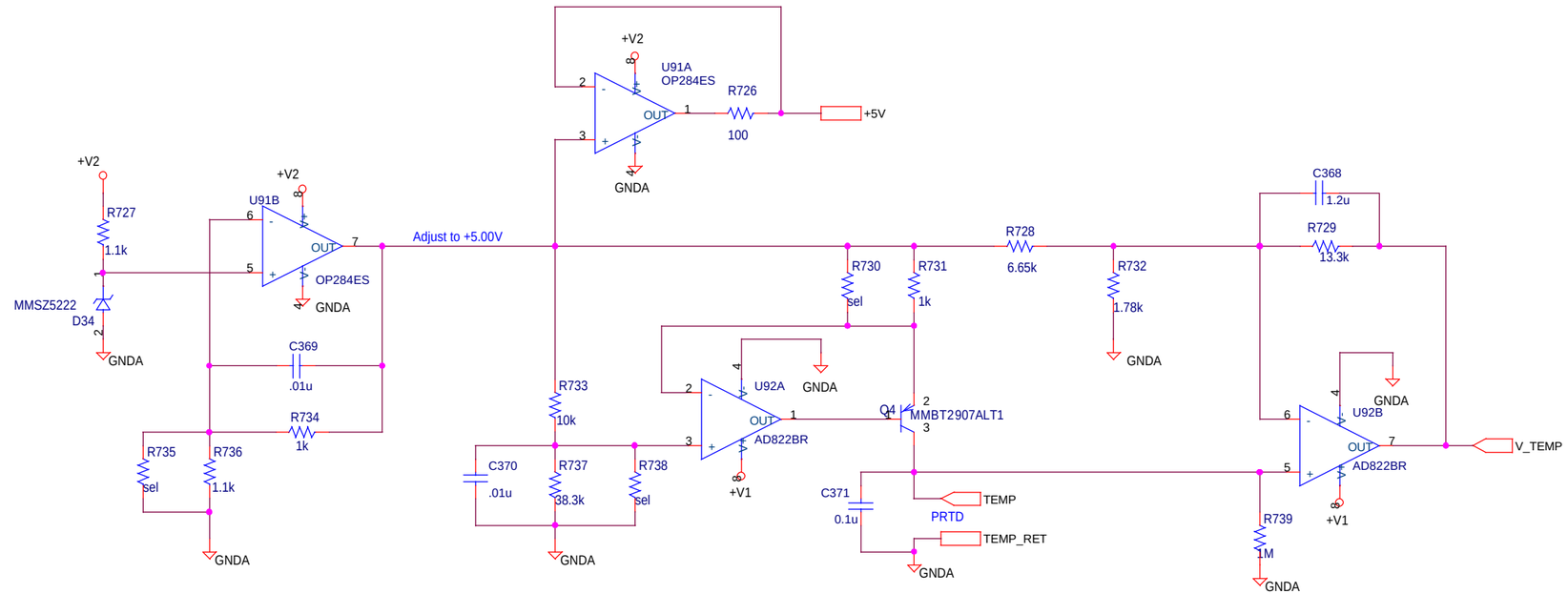

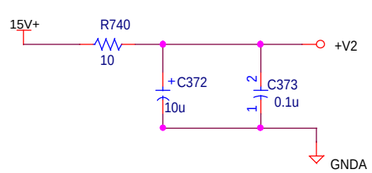

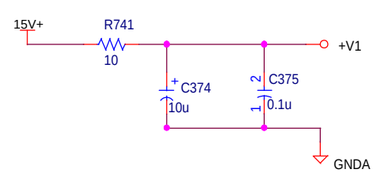

Notes:

1. Pick a FET in place of Q2 for lower error.
2. Ideal value for R31||R32 is 5.234k
3. Ideal value for R33||R34 is 1.192k
4. Check drive on OP-77
5. Size R25
6. Adjust R35 for 1mA max through thermistor

Note:
Temperature sensor is Pt RTD 1kOhm@0deg C.
3.85 deltaOhm / deg C.
Supply should be constant 1mA.

TEMP is one side of the PRTD, the raw temperature voltage
~1v +/-3.85mV/(deg.C).

TEMP_RET is the current-return side.

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Tim J. Sobering
124 Burt Hall
Kansas State University
Manhattan, KS 66506-0400

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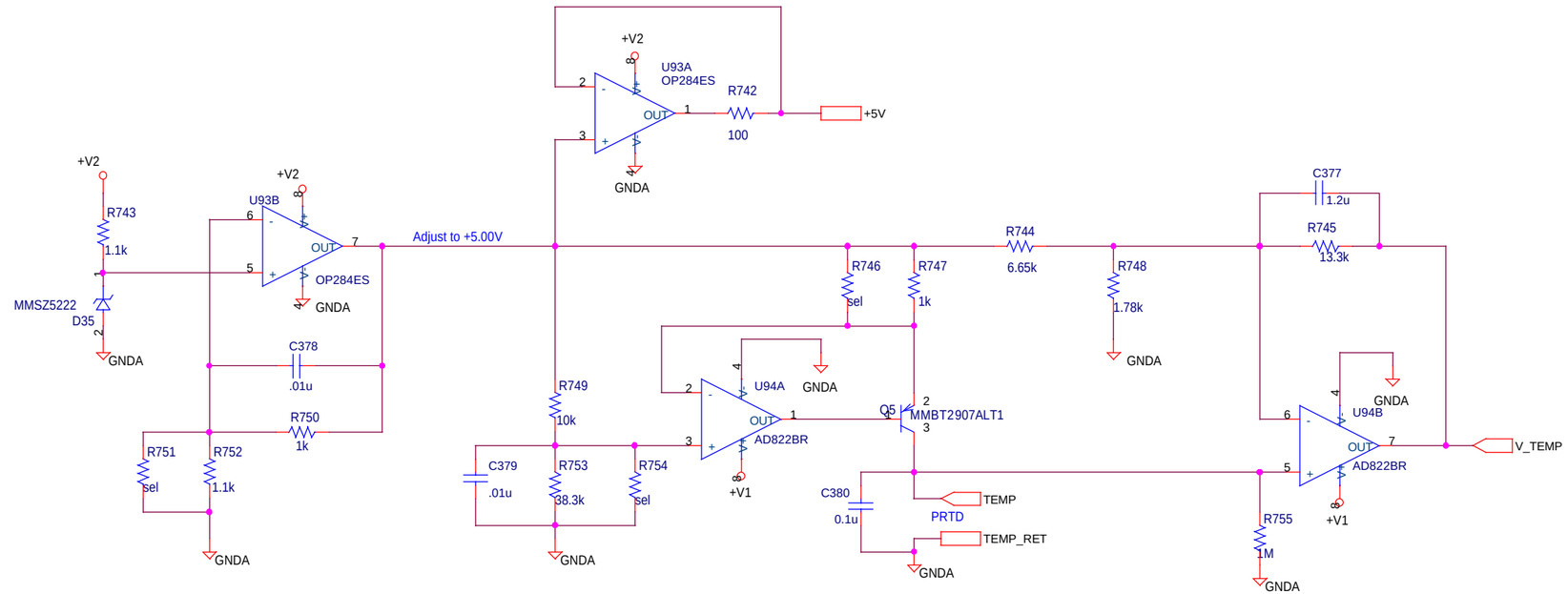

Notes:

1. Pick a FET in place of Q2 for lower error.
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124 Burt Hall
Kansas State University
Manhattan, KS 66506-0400

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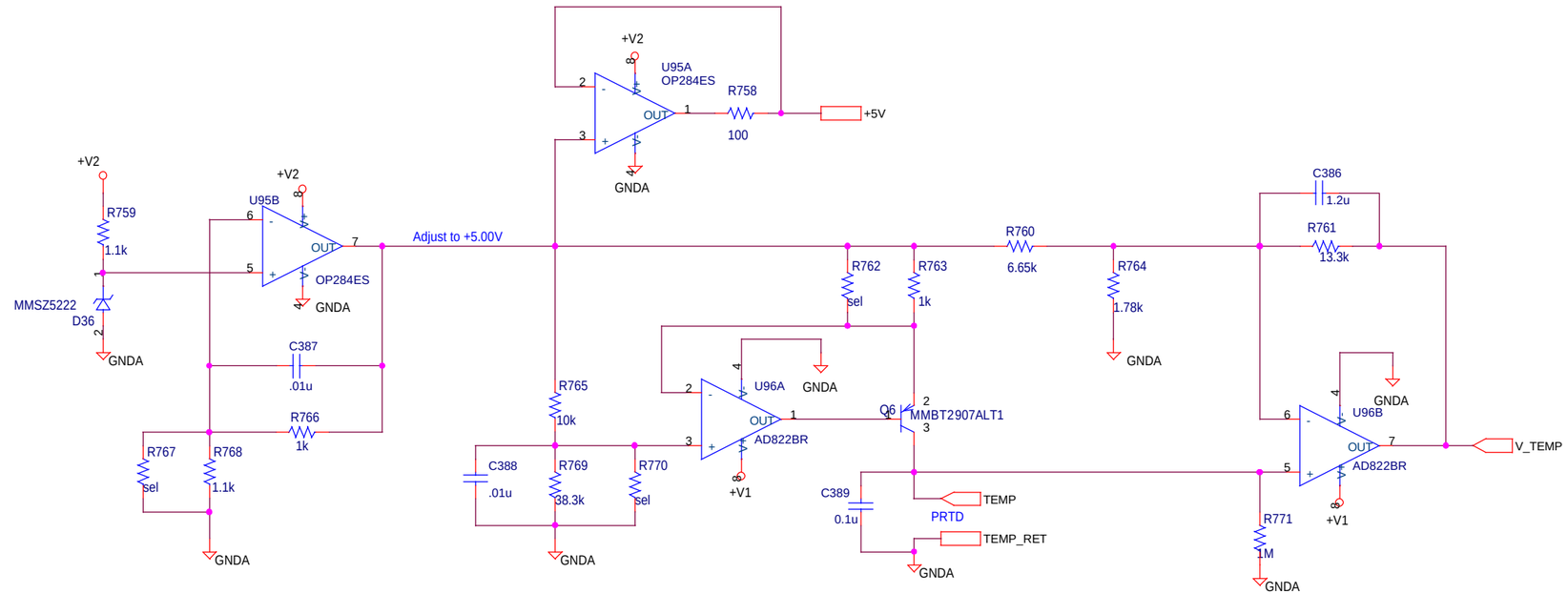

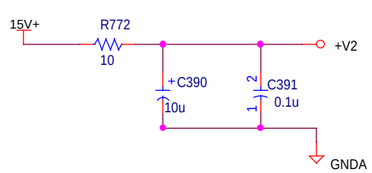

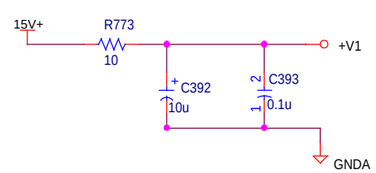

Notes:

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124 Burt Hall
Kansas State University
Manhattan, KS 66506-0400

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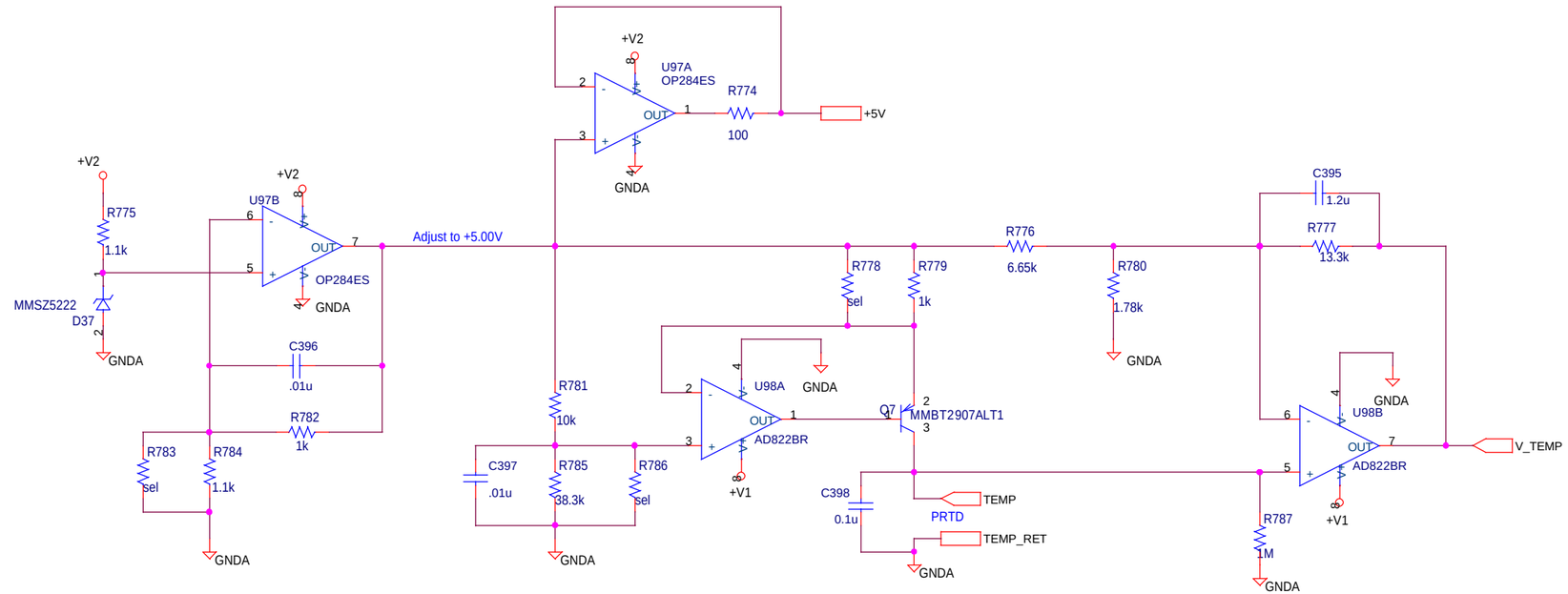

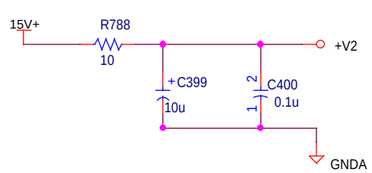

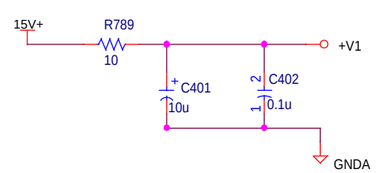

Notes:

1. Pick a FET in place of Q2 for lower error.
2. Ideal value for R31||R32 is 5.234k
3. Ideal value for R33||R34 is 1.192k
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5. Size R25
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124 Burt Hall
Kansas State University
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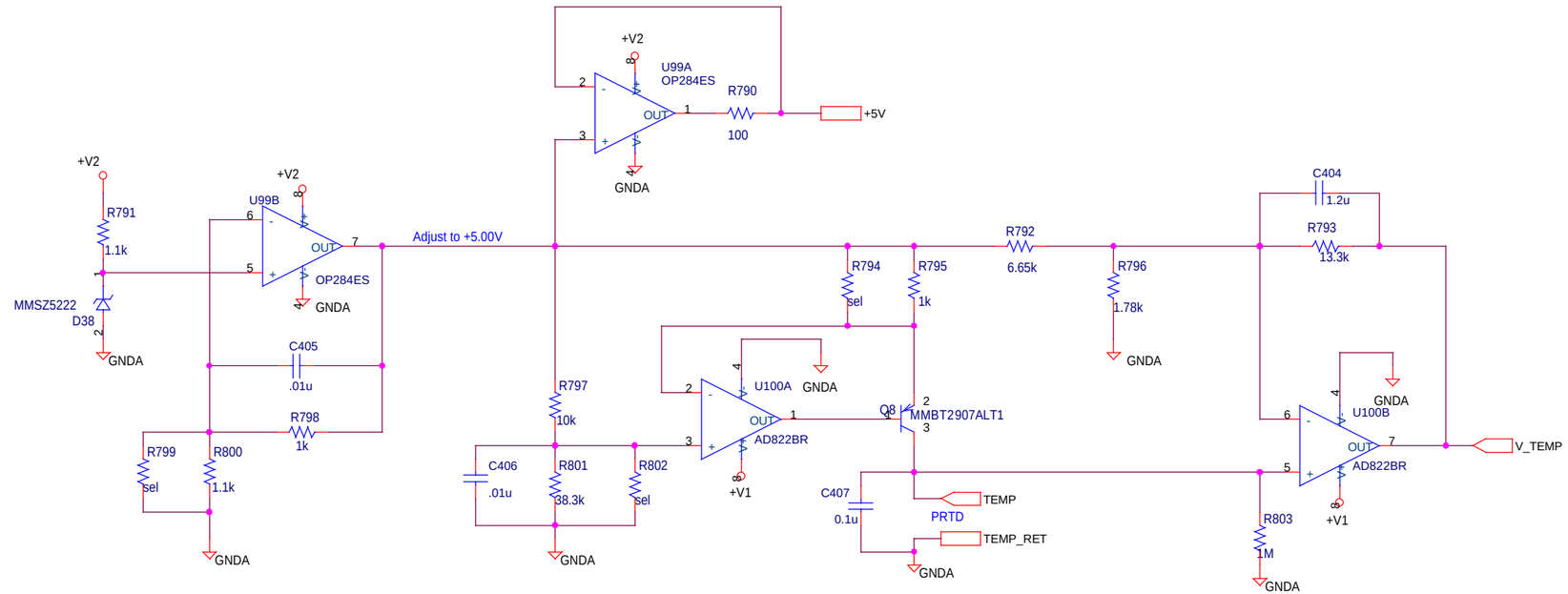

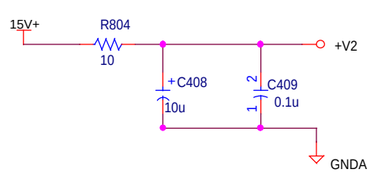

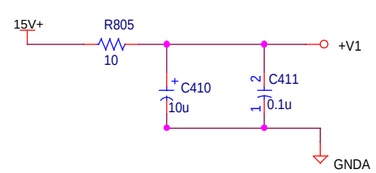

Notes:

1. Pick a FET in place of Q2 for lower error.
2. Ideal value for R31||R32 is 5.234k
3. Ideal value for R33||R34 is 1.192k
4. Check drive on OP-77
5. Size R25
6. Adjust R35 for 1mA max through thermistor

Note:
Temperature sensor is Pt RTD 1kOhm@0deg C.
3.85 deltaOhm / deg C.
Supply should be constant 1mA.

TEMP is one side of the PRTD, the raw temperature voltage
~1v +/-3.85mV/(deg.C).

TEMP_RET is the current-return side.

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Tim J. Sobering
124 Burt Hall
Kansas State University
Manhattan, KS 66506-0400

Title: Temperature Monitoring

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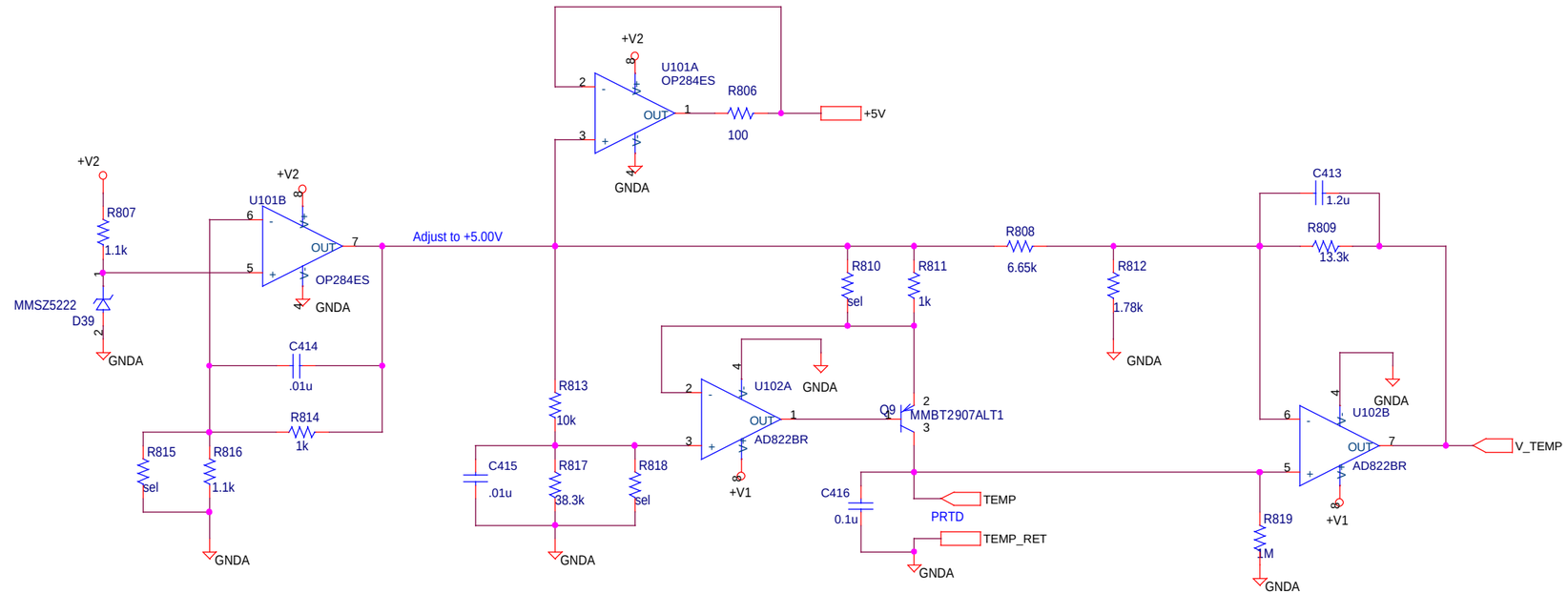

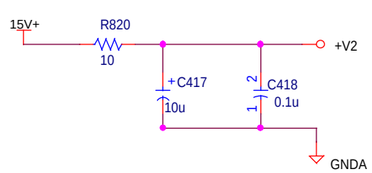

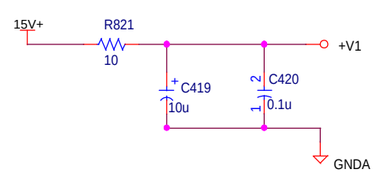

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124 Burt Hall
Kansas State University
Manhattan, KS 66506-0400

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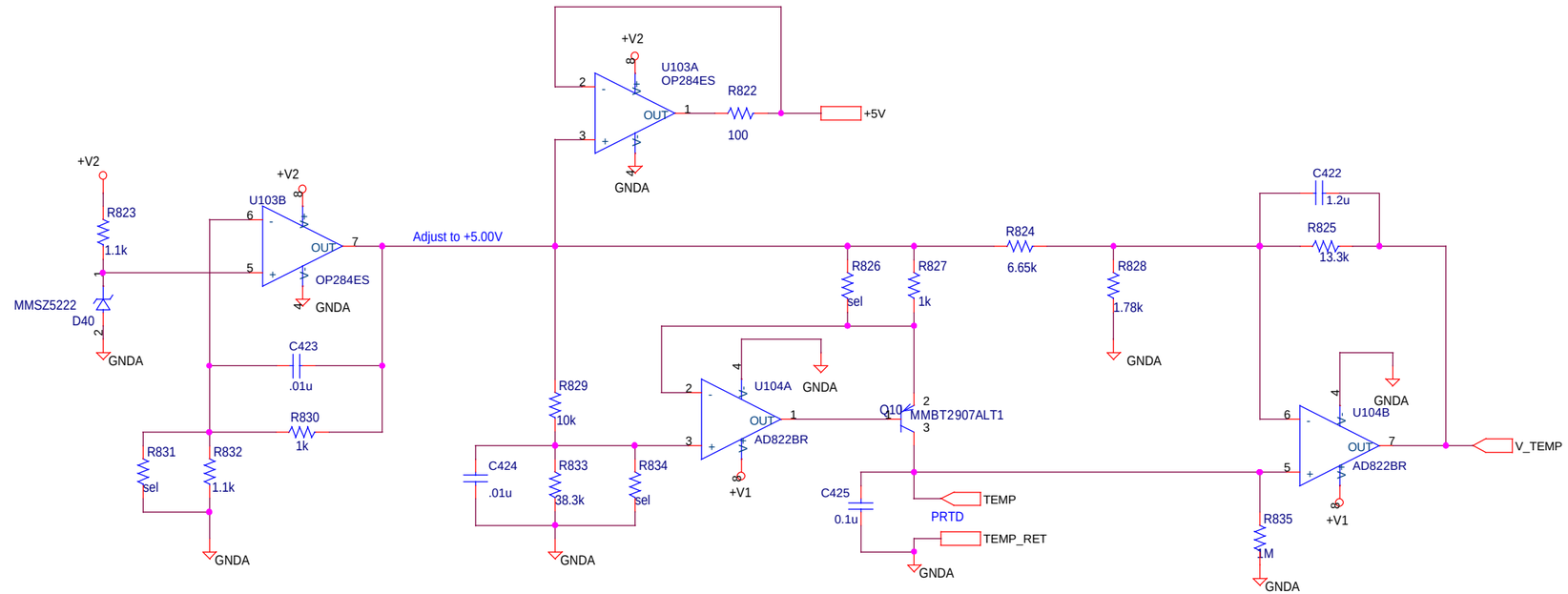

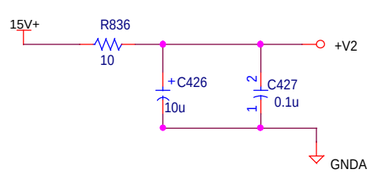

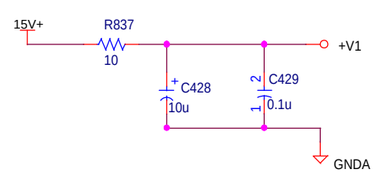

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Tim J. Sobering
124 Burt Hall
Kansas State University
Manhattan, KS 66506-0400

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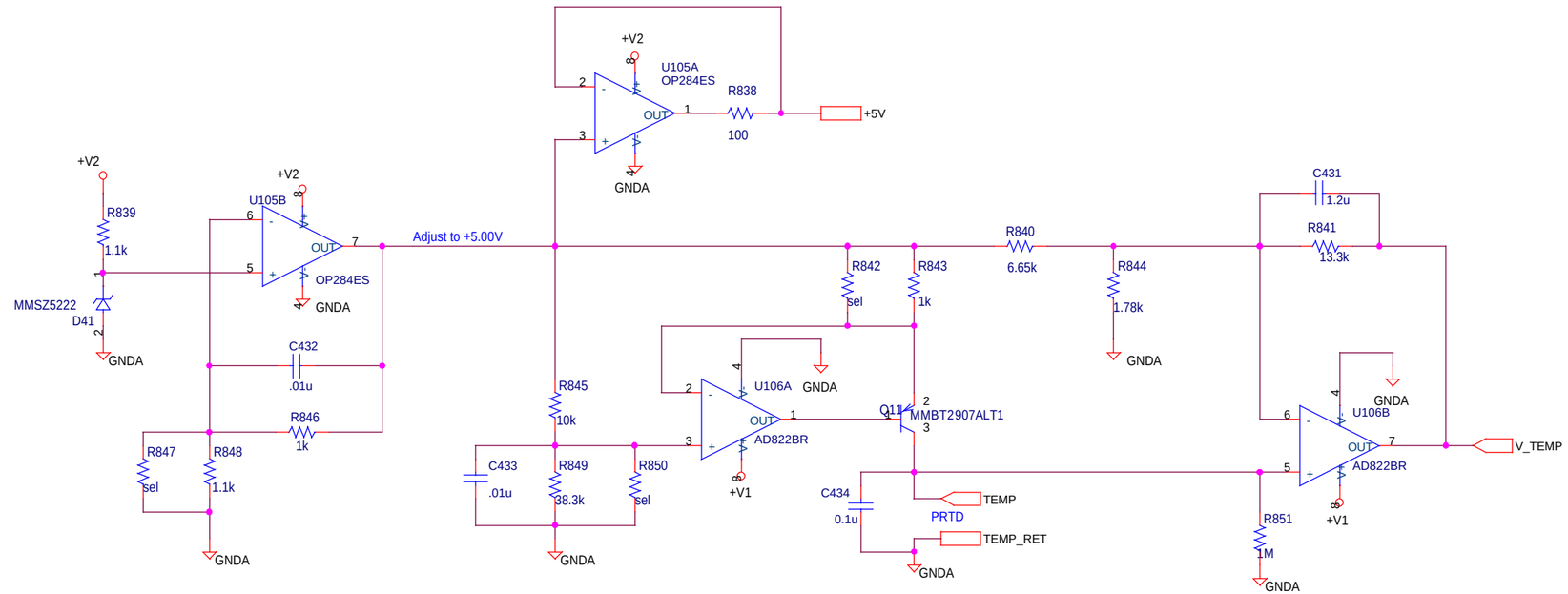

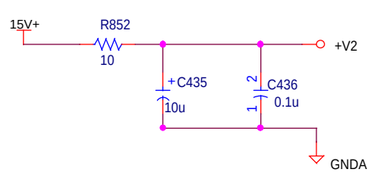

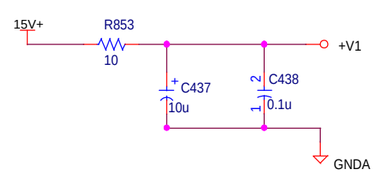

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3. Ideal value for R33||R34 is 1.192k
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Tim J. Sobering
124 Burt Hall
Kansas State University
Manhattan, KS 66506-0400

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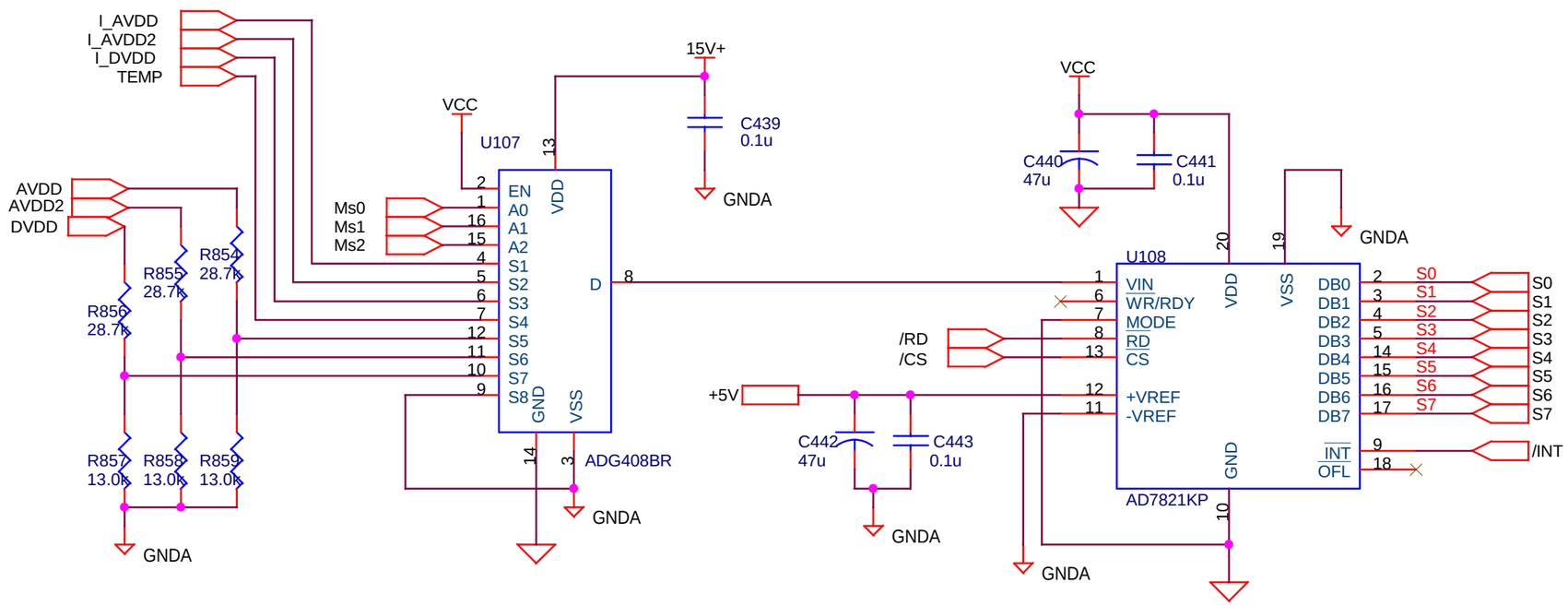

Title	Signal Mux & ADC	
Size A	Document Number <Doc>	Rev 3
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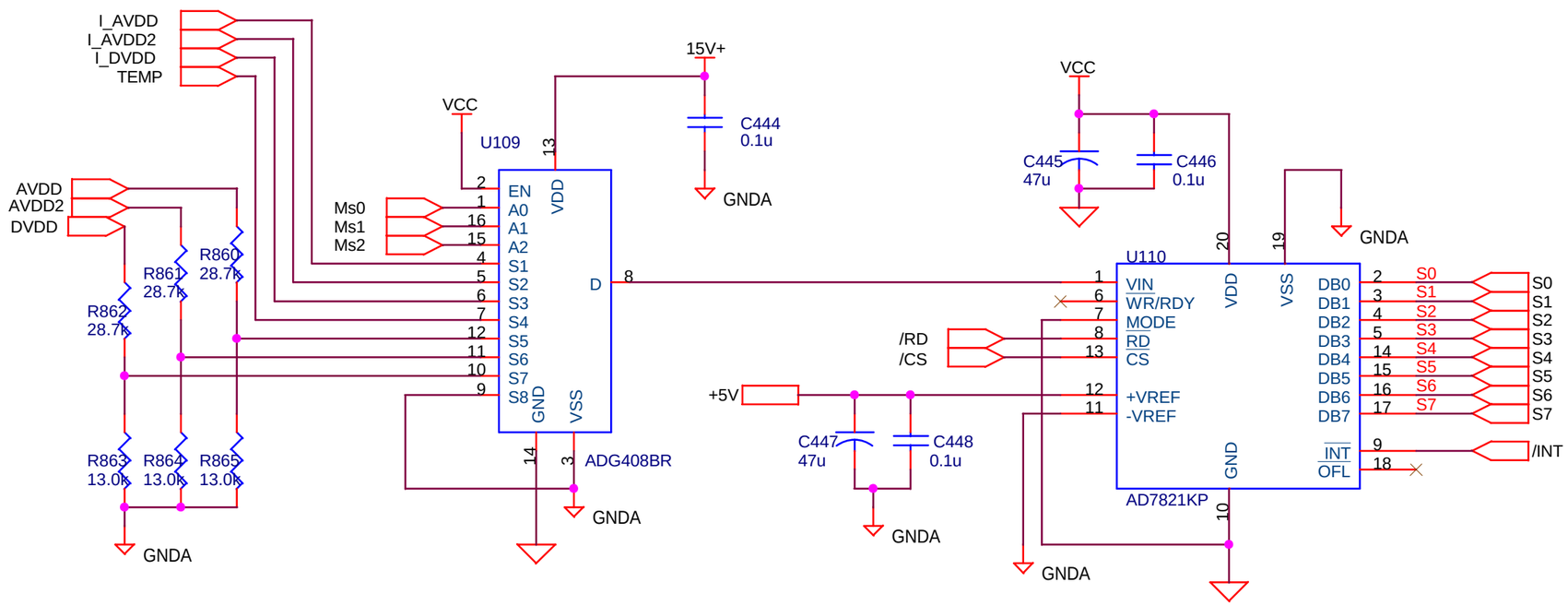

Title
Signal Mux & ADC

Size	Document Number	Rev
A	<Doc>	3

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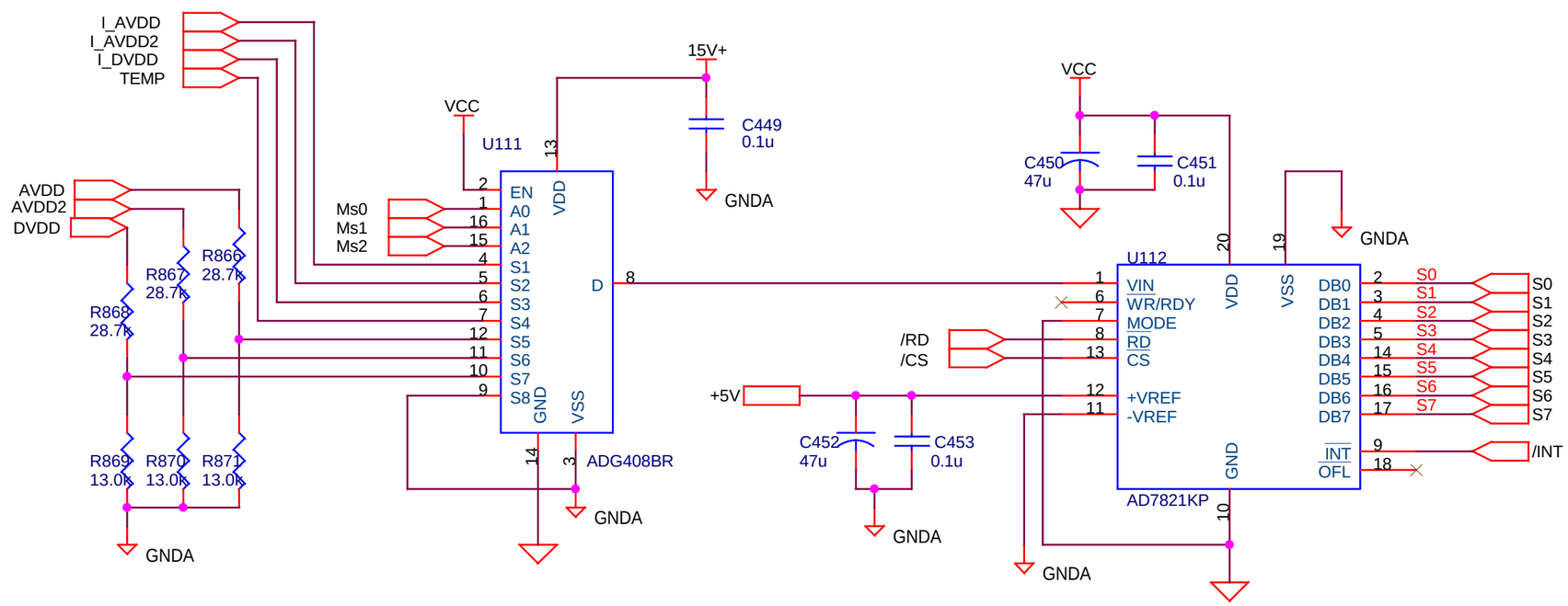
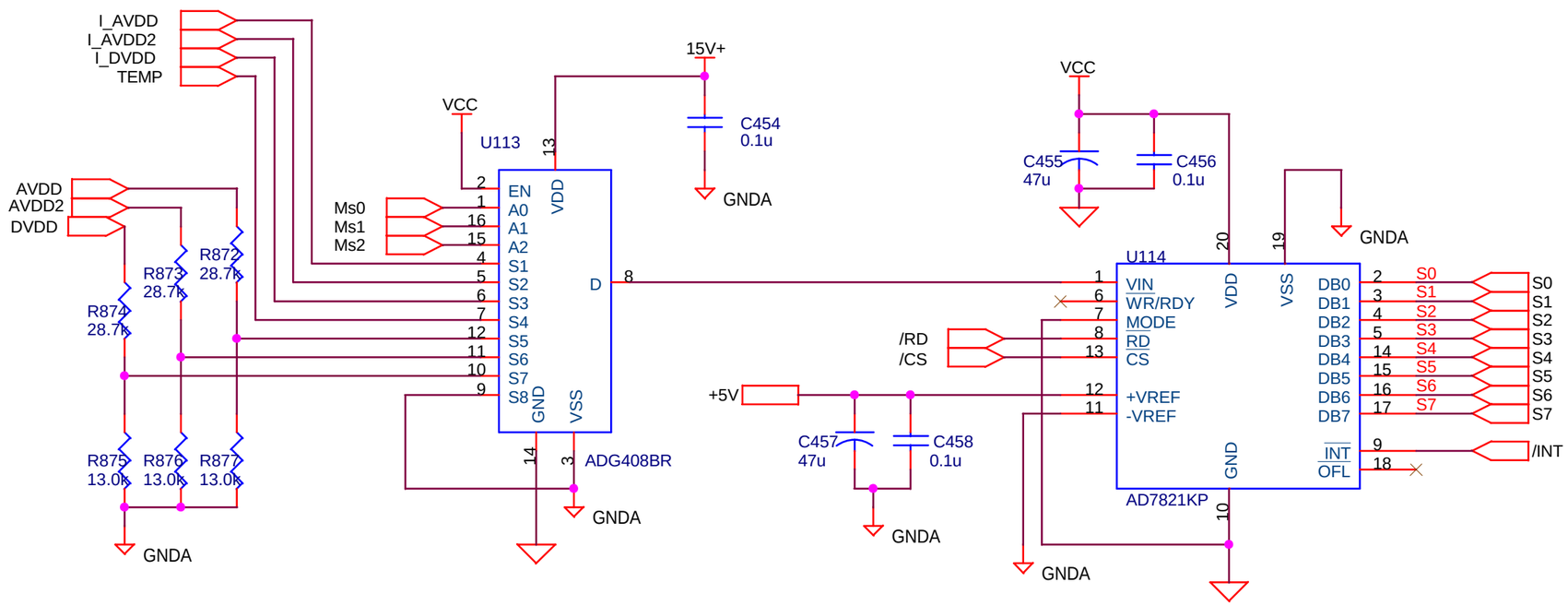
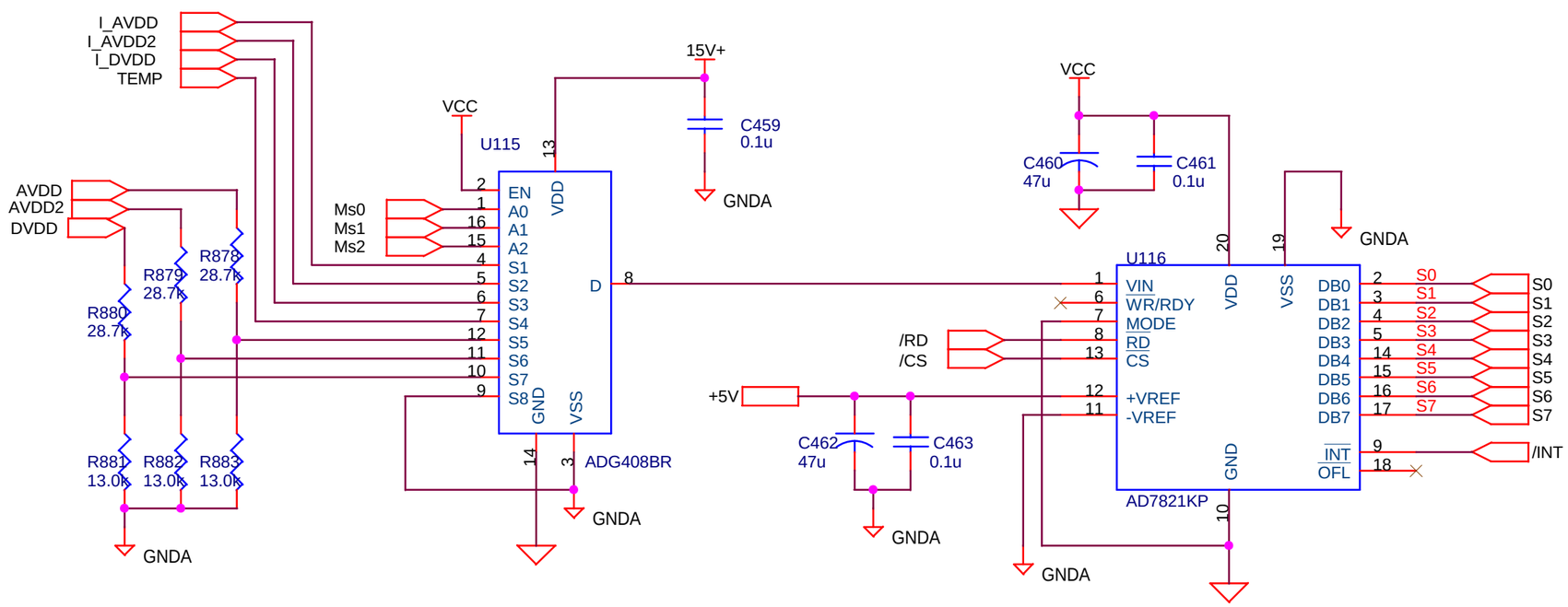


Title	Signal Mux & ADC	
Size A	Document Number <Doc>	Rev 3
Date: Wednesday, August 11, 1999	Sheet 84 of 95	



Title	Signal Mux & ADC	
Size A	Document Number <Doc>	Rev 3
Date: Wednesday, August 11, 1999	Sheet 85 of 95	



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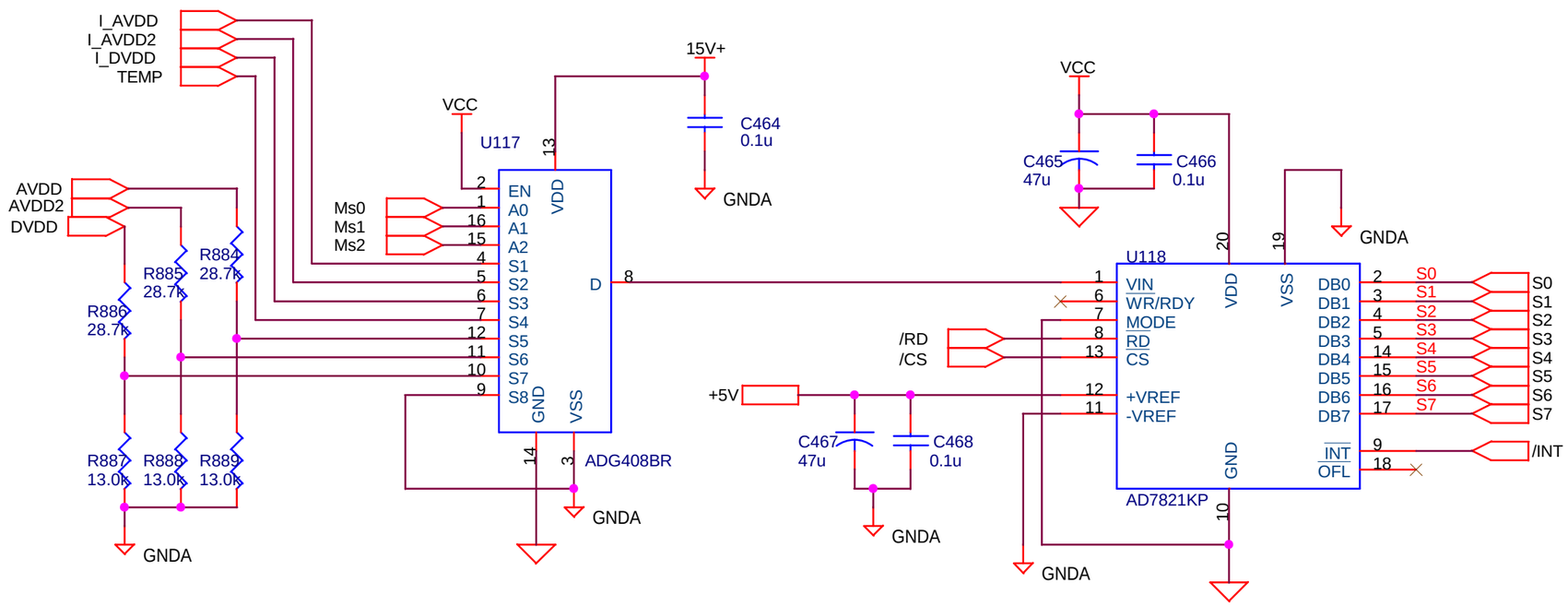
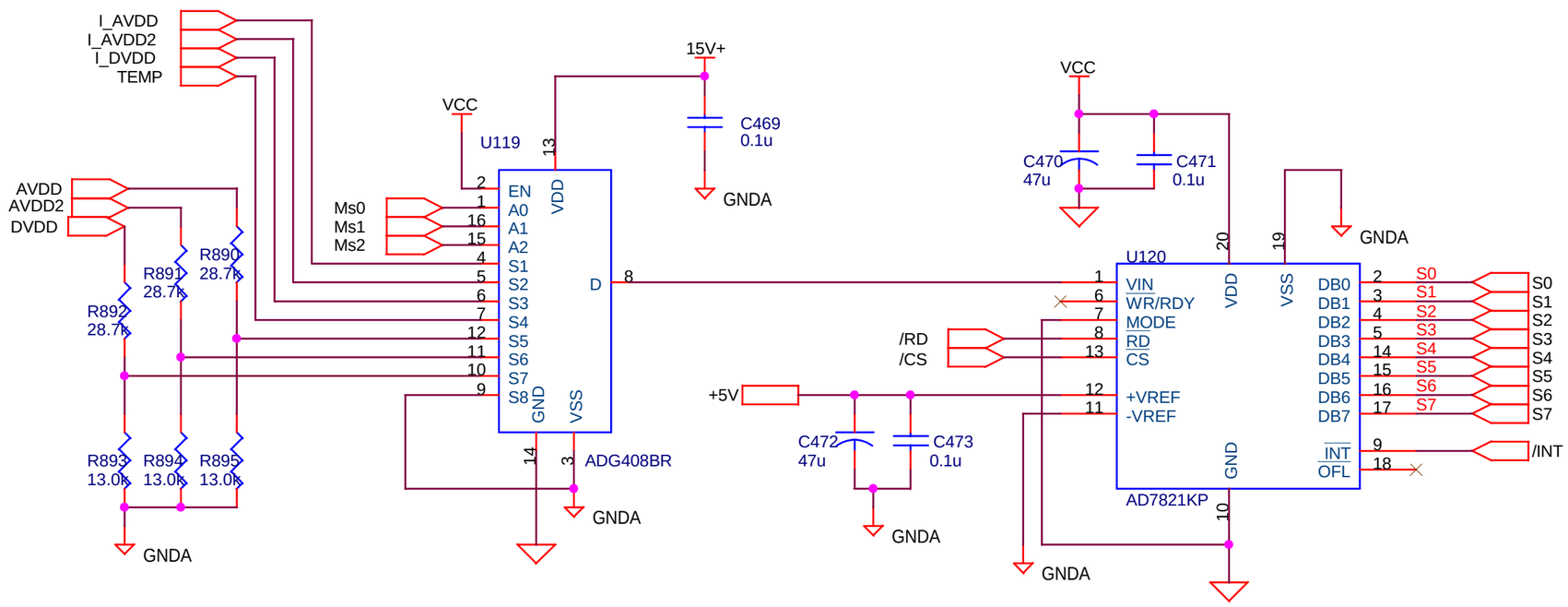
Size A	Document Number <Doc>	Rev 3
Date: Wednesday, August 11, 1999	Sheet 86 of 95	



Title	Signal Mux & ADC	
Size A	Document Number <Doc>	Rev 3
Date: Wednesday, August 11, 1999	Sheet 87 of 95	



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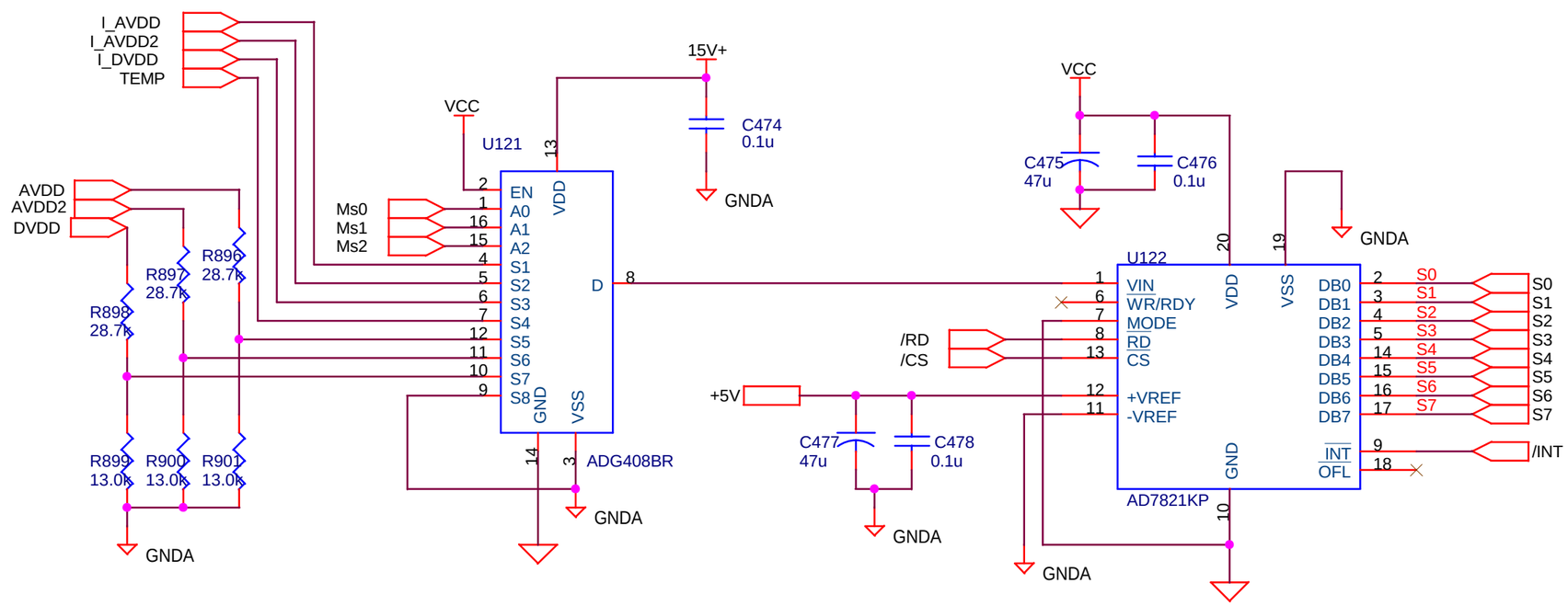
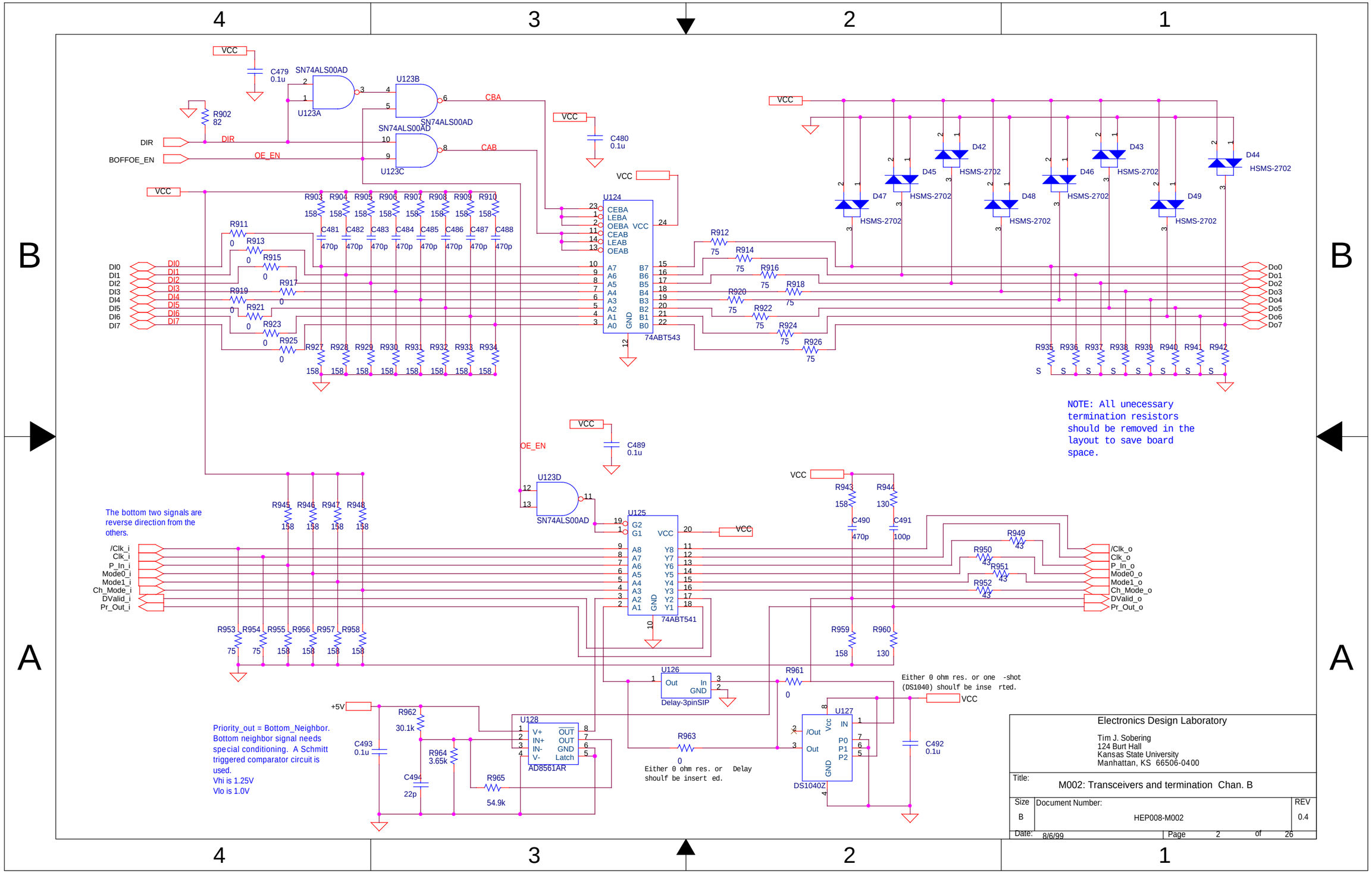
Size A	Document Number <Doc>	Rev 3
Date: Wednesday, August 11, 1999	Sheet 88 of 95	



Title	Signal Mux & ADC	
Size A	Document Number <Doc>	Rev 3
Date: Wednesday, August 11, 1999	Sheet 89 of 95	



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Tim J. Sobering
124 Burt Hall
Kansas State University
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Title: M002: Transceivers and termination Chan. B

Size	Document Number:	REV
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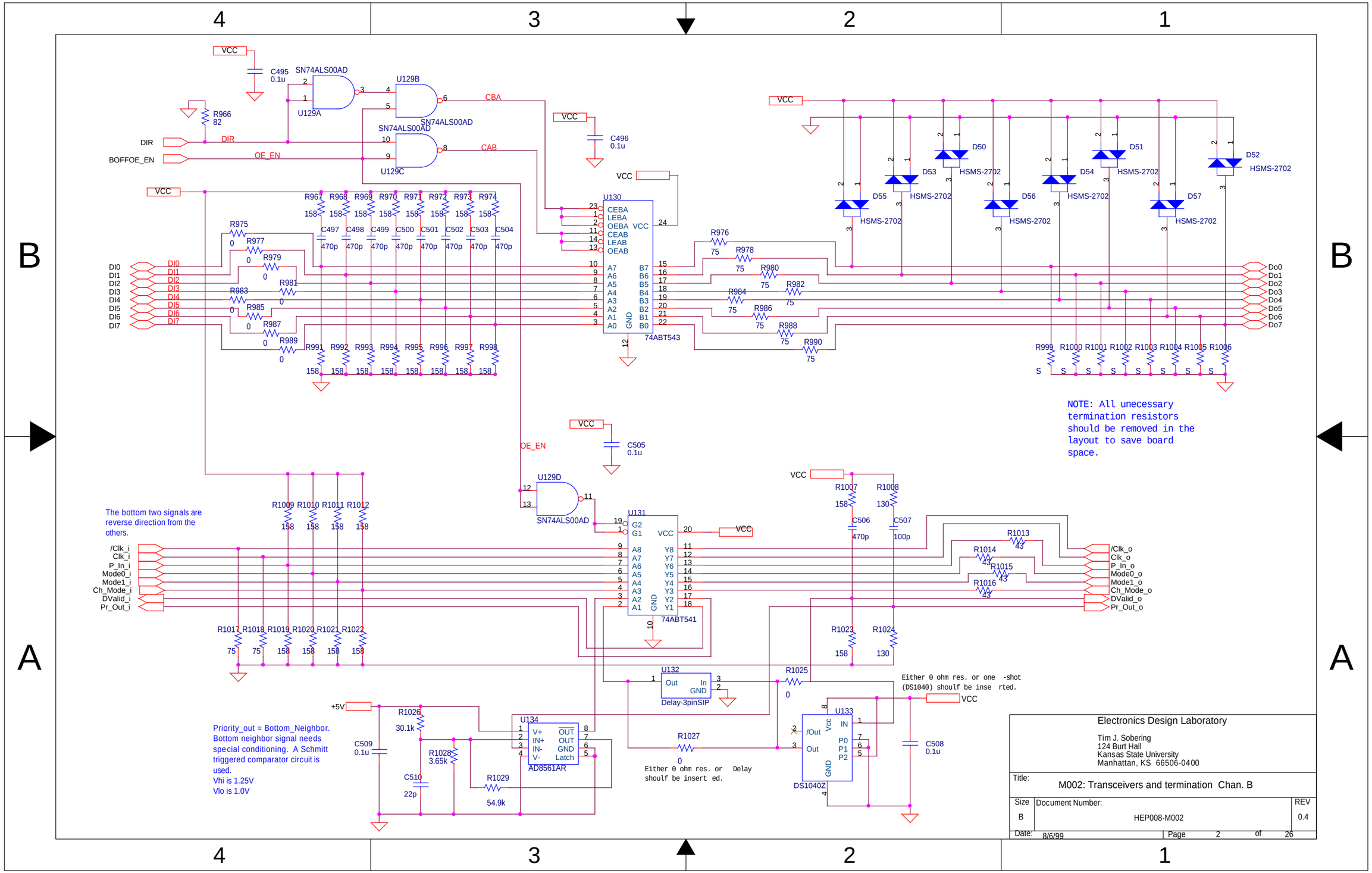

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Tim J. Sobering
124 Burt Hall
Kansas State University
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Title: M002: Transceivers and termination Chan. B

Size	Document Number:	REV
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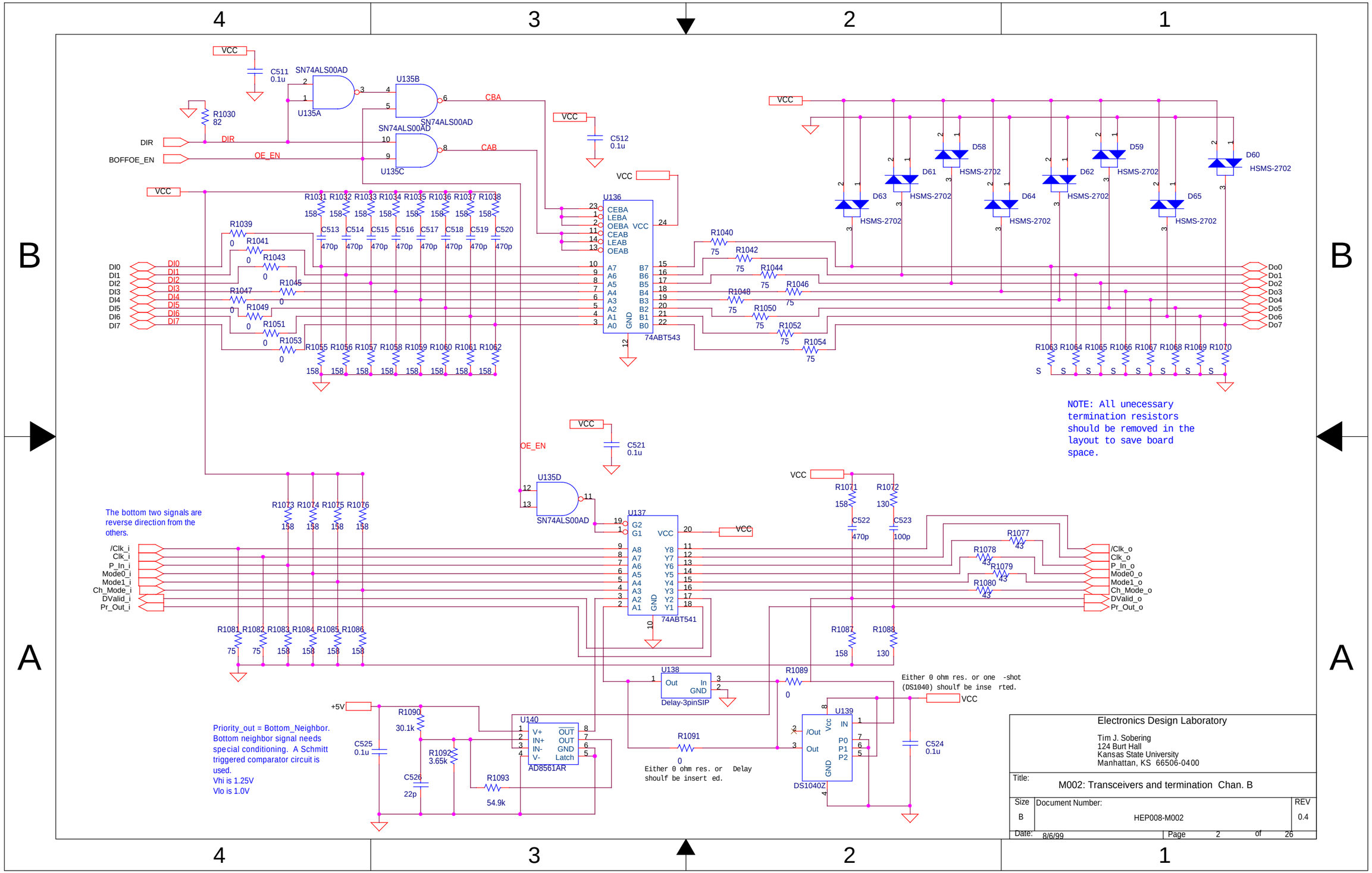
VCC
C511 0.1u
SN74ALS00AD
U135A
U135B
SN74ALS00AD
U135C
R1030 82
DIR
BOFFOE_EN
OE_EN
CBA
CAB
C512 0.1u
U136
74ABT543
CEBA
LEBA
OEBA
CEAB
LEAB
OEAB
GND
R1031 R1032 R1033 R1034 R1035 R1036 R1037 R1038
C513 C514 C515 C516 C517 C518 C519 C520
R1039 R1041 R1043 R1045 R1047 R1049 R1051 R1053
R1055 R1056 R1057 R1058 R1059 R1060 R1061 R1062
DI0 DI1 DI2 DI3 DI4 DI5 DI6 DI7
R1040 R1042 R1044 R1046 R1048 R1050 R1052 R1054
D58 D59 D60 D61 D62 D63 D64 D65
HSMS-2702
R1063 R1064 R1065 R1066 R1067 R1068 R1069 R1070
Do0 Do1 Do2 Do3 Do4 Do5 Do6 Do7
NOTE: All unecessary termination resistors should be removed in the layout to save board space.
C521 0.1u
U135D
SN74ALS00AD
U137
74ABT541
G2
G1
R1073 R1074 R1075 R1076
The bottom two signals are reverse direction from the others.
/Clk_i
Clk_i
P_In_i
Mode0_i
Mode1_i
Ch_Mode_i
DValid_i
Pr_Out_i
R1081 R1082 R1083 R1084 R1085 R1086
R1071 R1072
C522 470p
C523 100p
R1077 R1078 R1079 R1080
/Clk_o
Clk_o
P_In_o
Mode0_o
Mode1_o
Ch_Mode_o
DValid_o
Pr_Out_o
R1087 R1088
U138
Delay-3pinSIP
Out
In
GND
R1089
Either 0 ohm res. or one -shot (DS1040) shoulf be inse rted.
+5V
R1090 30.1k
C525 0.1u
R1092 3.65k
C526 22p
R1093 54.9k
U140
AD8561AR
V+
IN+
IN-
V-
OUT
GND
Latch
Priority_out = Bottom_Neighbor. Bottom neighbor signal needs special conditioning. A Schmitt triggered comparator circuit is used.
Vhi is 1.25V
Vlo is 1.0V
R1091
Either 0 ohm res. or Delay shoulf be insert ed.
U139
DS1040Z
/Out
Out
IN
P0
P1
P2
C524 0.1u
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Tim J. Sobering
124 Burt Hall
Kansas State University
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M002: Transceivers and termination Chan. B
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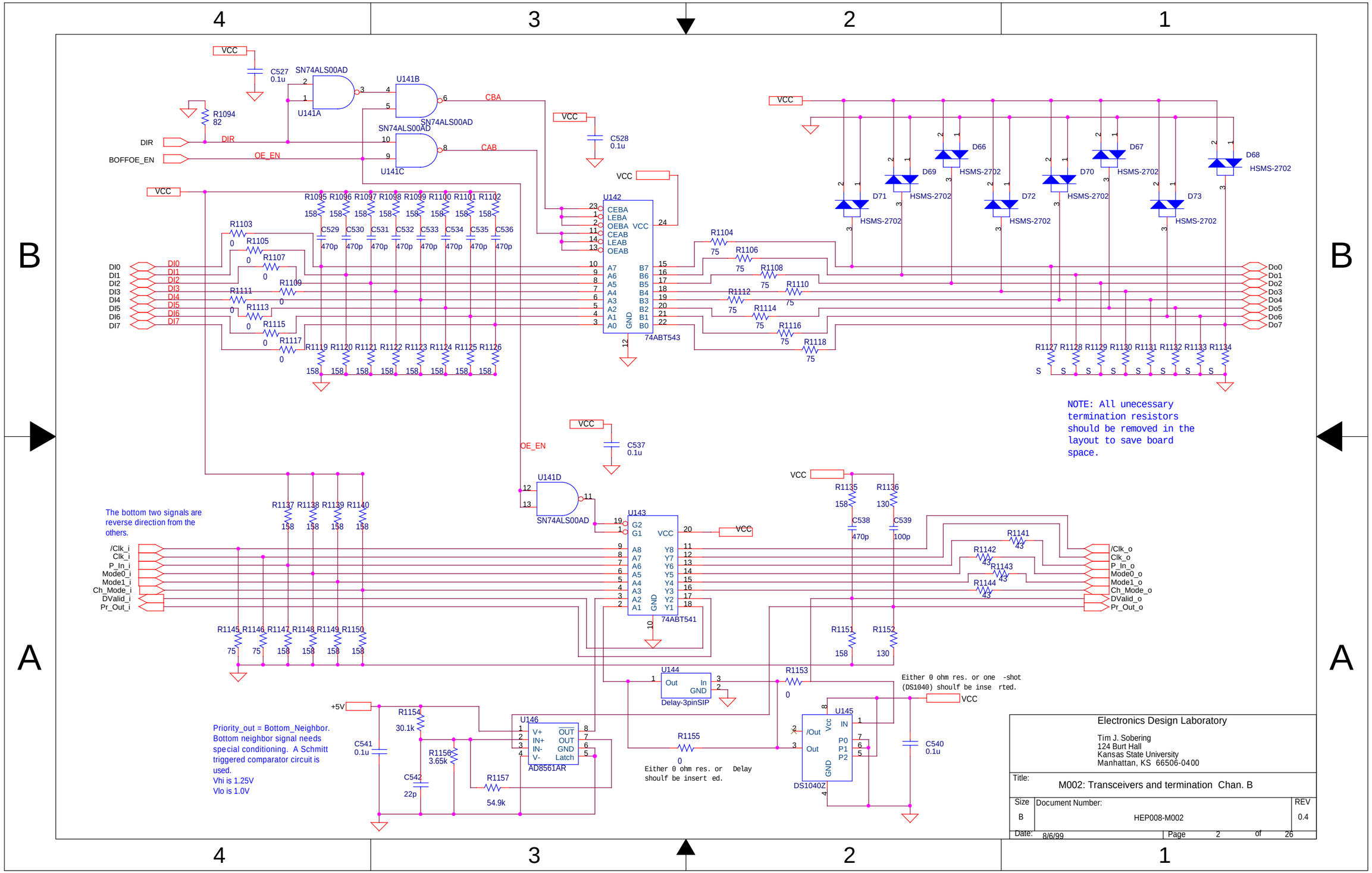
VCC
C527 0.1u
SN74ALS00AD
U141A
U141B
SN74ALS00AD
U141C
R1094 82
DIR
BOFFOE_EN
OE_EN
CBA
CAB
C528 0.1u
U142
74ABT543
CEBA
LEBA
OEBA
CEAB
LEAB
OEAB
GND
DI0
DI1
DI2
DI3
DI4
DI5
DI6
DI7
Do0
Do1
Do2
Do3
Do4
Do5
Do6
Do7
HSMS-2702
NOTE: All unecessary termination resistors should be removed in the layout to save board space.
C537 0.1u
U141D
SN74ALS00AD
U143
74ABT541
The bottom two signals are reverse direction from the others.
/Clk_i
Clk_i
P_In_i
Mode0_i
Mode1_i
Ch_Mode_i
DValid_i
Pr_Out_i
/Clk_o
Clk_o
P_In_o
Mode0_o
Mode1_o
Ch_Mode_o
DValid_o
Pr_Out_o
C538 470p
C539 100p
U144
Delay-3pinSIP
Either 0 ohm res. or one -shot (DS1040) shoulf be inse rted.
Either 0 ohm res. or Delay shoulf be insert ed.
U145
DS1040Z
+5V
U146
AD8561AR
Priority_out = Bottom_Neighbor. Bottom neighbor signal needs special conditioning. A Schmitt triggered comparator circuit is used.
Vhi is 1.25V
Vlo is 1.0V
C541 0.1u
C542 22p
C540 0.1u
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Tim J. Sobering
124 Burt Hall
Kansas State University
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Title:
M002: Transceivers and termination Chan. B
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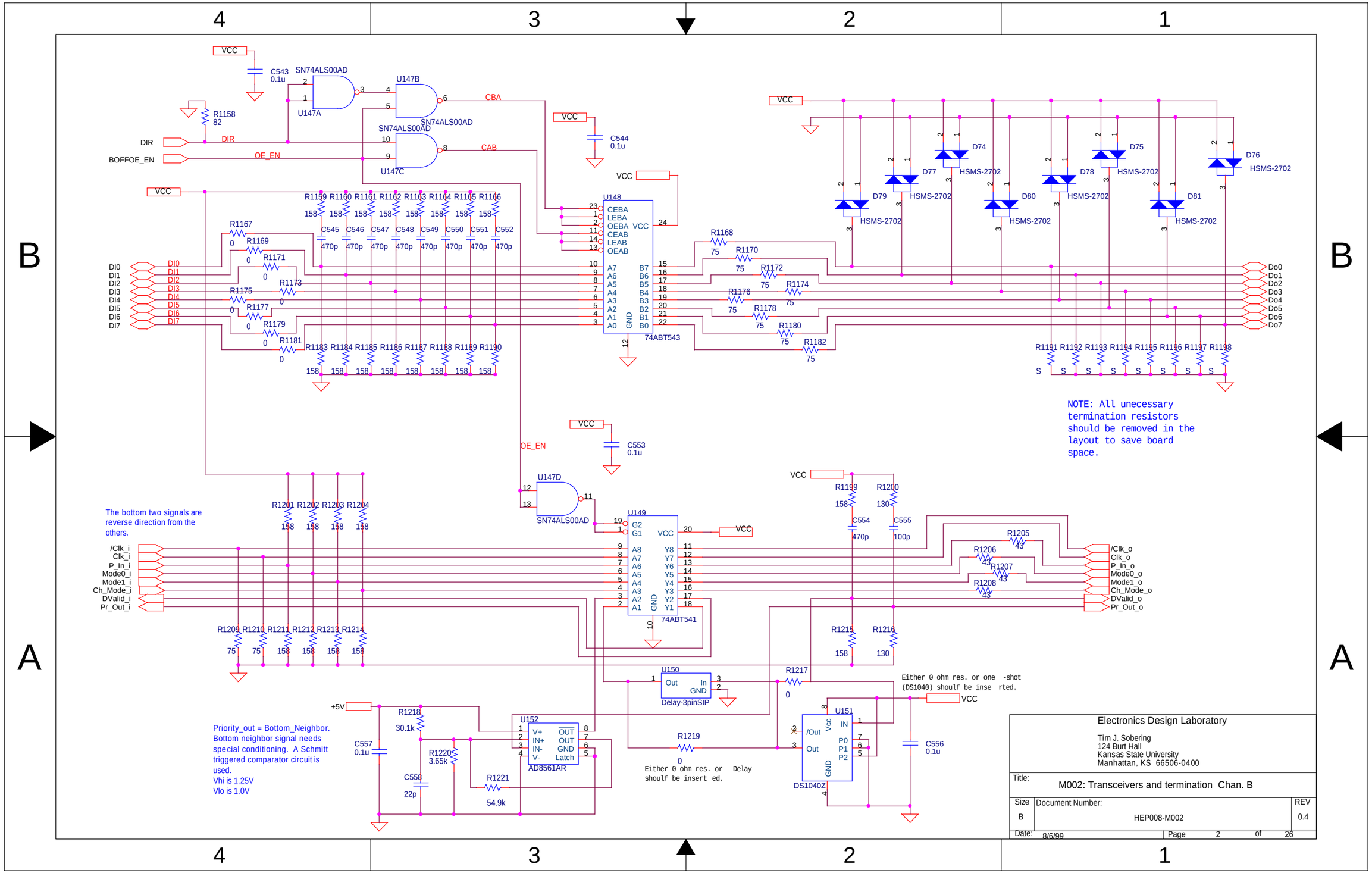
VCC
C543 0.1u
SN74ALS00AD
U147A
U147B
U147C
U147D
R1158 82
DIR
BOFFOE_EN
OE_EN
CBA
CAB
C544 0.1u
C553 0.1u
U148
74ABT543
CEBA
LEBA
OEBA
CEAB
LEAB
OEAB
A7 A6 A5 A4 A3 A2 A1 A0
B7 B6 B5 B4 B3 B2 B1 B0
GND
R1159 R1160 R1161 R1162 R1163 R1164 R1165 R1166
C545 C546 C547 C548 C549 C550 C551 C552
470p
R1167 R1169 R1171 R1173 R1175 R1177 R1179 R1181
R1183 R1184 R1185 R1186 R1187 R1188 R1189 R1190
DI0 DI1 DI2 DI3 DI4 DI5 DI6 DI7
R1168 R1170 R1172 R1174 R1176 R1178 R1180 R1182
75
D74 D75 D76 D77 D78 D79 D80 D81
HSMS-2702
R1191 R1192 R1193 R1194 R1195 R1196 R1197 R1198
Do0 Do1 Do2 Do3 Do4 Do5 Do6 Do7
NOTE: All unecessary termination resistors should be removed in the layout to save board space.
The bottom two signals are reverse direction from the others.
R1201 R1202 R1203 R1204
158
/Clk_i
Clk_i
P_In_i
Mode0_i
Mode1_i
Ch_Mode_i
DValid_i
Pr_Out_i
R1209 R1210 R1211 R1212 R1213 R1214
75
U149
74ABT541
G2
G1
A8 A7 A6 A5 A4 A3 A2 A1
Y8 Y7 Y6 Y5 Y4 Y3 Y2 Y1
R1199 R1200
130
C554 470p
C555 100p
R1205 R1206 R1207 R1208
43
/Clk_o
Clk_o
P_In_o
Mode0_o
Mode1_o
Ch_Mode_o
DValid_o
Pr_Out_o
R1215 R1216
U150
Delay-3pinSIP
Out
In
GND
R1217
0
Either 0 ohm res. or one -shot (DS1040) shoulf be inse rted.
+5V
R1218 30.1k
C557 0.1u
C558 22p
R1220 3.65k
R1221 54.9k
U152
AD8561AR
V+
IN+
IN-
V-
OUT
GND
Latch
Priority_out = Bottom_Neighbor. Bottom neighbor signal needs special conditioning. A Schmitt triggered comparator circuit is used.
Vhi is 1.25V
Vlo is 1.0V
R1219
Either 0 ohm res. or Delay shoulf be insert ed.
U151
DS1040Z
/Out
Out
IN
P0
P1
P2
C556 0.1u
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Tim J. Sobering
124 Burt Hall
Kansas State University
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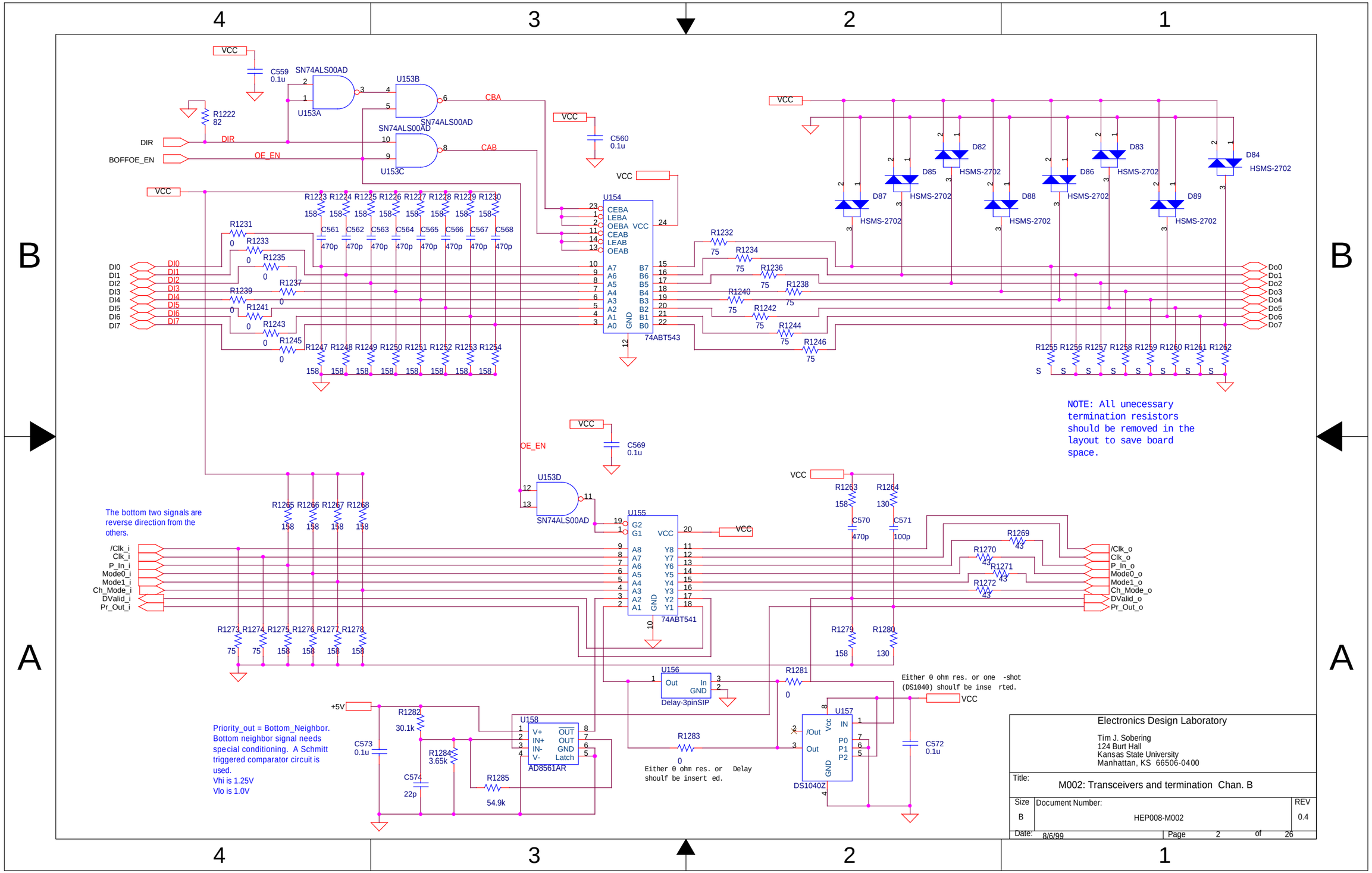
VCC
C559 0.1u
SN74ALS00AD
U153A
U153B
U153C
U153D
R1222 82
DIR
BOFFOE_EN
OE_EN
CBA
CAB
C560 0.1u
C569 0.1u
U154
74ABT543
CEBA
LEBA
OEBA
CEAB
LEAB
OEAB
A7 A6 A5 A4 A3 A2 A1 A0
B7 B6 B5 B4 B3 B2 B1 B0
GND
DI0 DI1 DI2 DI3 DI4 DI5 DI6 DI7
Do0 Do1 Do2 Do3 Do4 Do5 Do6 Do7
HSMS-2702
D82 D83 D84 D85 D86 D87 D88 D89
NOTE: All unecessary termination resistors should be removed in the layout to save board space.
The bottom two signals are reverse direction from the others.
/Clk_i
Clk_i
P_In_i
Mode0_i
Mode1_i
Ch_Mode_i
DValid_i
Pr_Out_i
/Clk_o
Clk_o
P_In_o
Mode0_o
Mode1_o
Ch_Mode_o
DValid_o
Pr_Out_o
U155
74ABT541
G2 G1
A8 A7 A6 A5 A4 A3 A2 A1
Y8 Y7 Y6 Y5 Y4 Y3 Y2 Y1
C570 470p
C571 100p
U156
Delay-3pinSIP
Out In GND
Either 0 ohm res. or one -shot (DS1040) shoulf be inse rted.
Priority_out = Bottom_Neighbor. Bottom neighbor signal needs special conditioning. A Schmitt triggered comparator circuit is used.
Vhi is 1.25V
Vlo is 1.0V
+5V
U158
AD8561AR
V+ IN+ IN- V-
OUT OUT GND Latch
C573 0.1u
C574 22p
R1282 30.1k
R1284 3.65k
R1285 54.9k
R1283 0
Either 0 ohm res. or Delay shoulf be insert ed.
U157
DS1040Z
/Out Out Vcc GND IN P0 P1 P2
C572 0.1u
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124 Burt Hall
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