1553 to SRC/SFE Interface Memory Map

Updated: June 25, 2001:

SubAddress	Register/Function	R/W	#words	
0x00/0	MODE Command	R	Mode Code	
0x01/1	SRC VME CSR1	R	1 word	12 words
	SRC Readout Controller CSR1		1 word	
	SFE0 VME CSR1		10 words	
	…			
	SFE9 VME CSR1			
0x02/2	Crate Analog Data: A_Crate0 (Voltage, temp, etc.)	R	6 words	
	…			
	Crate Analog Data: A_Crate5			
0x03/3	Interrupt Vector: IRQ7	R	3 words	
	Interrupt Vector: IRQ6			
	Interrupt Vector: IRQ5			
0x04/4	SFE Write-only: Reset SFE boards CSR	W	1 word	5 words x 16 1-bit fields
	Clear latched errors CSR		1 word	
	Reset output FIFO read pointer CSR		1 word	
	Reset output FIFO CSR		1 word	
	Reset TMCs CSR		1 word	
0x05/5	DSP Code Page Number	W	1 word	
	DSP Code Version	R		
0x06/6	SRC Board Main CSR0	R/W	3 words	
	System Status Register 1			
	System Status Register 2			
0x07/7	SRC RC SFE Mask Register <15:0>	R/W	4 words	
	SRC RC SFE Timeout Register <7:0> / SRC RC Timeout Error SFE Address <11:8> / SRC RC SFE_TO_ERR <12> / SRC RC FULL_ERR <13>			
	SRC RC Page Full Register <15:0>			
	SRC RC L1 Buffer Page – L1_COUNT <3:0> / SRC RC L1 Buffer Page – PAGE_COUNT <7:4>			
0x08/8	L1 Trigger Latency Preset	R/W	7 words	
	Test Pulse Crossing Preset			
	Test Pulse L1 Accept Crossing Preset			
	Test Pulse Coarse Delay <2:0> / L1 Disable <4> / INIT Hold <5>			
	Beam Delay			
	Test Pulse Repeat Prescale			
	Local L1 Accept Delay			
0x09/9	SRC HOTLINK CSRs: L2 & L3	R/W	2 words	
0x0A/10	SFE0 Master Controller CSR0	R/W	10 words	
	…			
	SFE9 Master Controller CSR0			
0x0B/11	SFE0: Group A TMC Read Pointer	R/W	6 words	
	SFE0: Group A TMC Write Pointer			
	SFE0: Group B TMC Read Pointer			
	SFE0: Group B TMC Write Pointer			
	SFE0: Group C TMC Read Pointer			
	SFE0: Group C TMC Write Pointer			
0x0C/12	SFE1: Group A TMC Read Pointer	R/W	6 words	
	SFE1: Group A TMC Write Pointer			

	SFE1: Group B TMC Read Pointer		
	SFE1: Group B TMC Write Pointer		
	SFE1: Group C TMC Read Pointer		
	SFE1: Group C TMC Write Pointer		
0x0D/13	SFE2: Group A TMC Read Pointer	R/W	6 words
	SFE2: Group A TMC Write Pointer		
	SFE2: Group B TMC Read Pointer		
	SFE2: Group B TMC Write Pointer		
	SFE2: Group C TMC Read Pointer		
	SFE2: Group C TMC Write Pointer		
0x0E/14	SFE3: Group A TMC Read Pointer	R/W	6 words
	SFE3: Group A TMC Write Pointer		
	SFE3: Group B TMC Read Pointer		
	SFE3: Group B TMC Write Pointer		
	SFE3: Group C TMC Read Pointer		
	SFE3: Group C TMC Write Pointer		
0x0F/15	SFE4: Group A TMC Read Pointer	R/W	6 words
	SFE4: Group A TMC Write Pointer		
	SFE4: Group B TMC Read Pointer		
	SFE4: Group B TMC Write Pointer		
	SFE4: Group C TMC Read Pointer		
	SFE4: Group C TMC Write Pointer		
0x10/16	SFE5: Group A TMC Read Pointer	R/W	6 words
	SFE5: Group A TMC Write Pointer		
	SFE5: Group B TMC Read Pointer		
	SFE5: Group B TMC Write Pointer		
	SFE5: Group C TMC Read Pointer		
	SFE5: Group C TMC Write Pointer		
0x11/17	SFE6: Group A TMC Read Pointer	R/W	6 words
	SFE6: Group A TMC Write Pointer		
	SFE6: Group B TMC Read Pointer		
	SFE6: Group B TMC Write Pointer		
	SFE6: Group C TMC Read Pointer		
	SFE6: Group C TMC Write Pointer		
0x12/18	SFE7: Group A TMC Read Pointer	R/W	6 words
	SFE7: Group A TMC Write Pointer		
	SFE7: Group B TMC Read Pointer		
	SFE7: Group B TMC Write Pointer		
	SFE7: Group C TMC Read Pointer		
	SFE7: Group C TMC Write Pointer		
0x13/19	SFE8: Group A TMC Read Pointer	R/W	6 words
	SFE8: Group A TMC Write Pointer		
	SFE8: Group B TMC Read Pointer		
	SFE8: Group B TMC Write Pointer		
	SFE8: Group C TMC Read Pointer		
	SFE8: Group C TMC Write Pointer		
0x14/20	SFE9: Group A TMC Read Pointer	R/W	6 words
	SFE9: Group A TMC Write Pointer		
	SFE9: Group B TMC Read Pointer		
	SFE9: Group B TMC Write Pointer		
	SFE9: Group C TMC Read Pointer		
	SFE9: Group C TMC Write Pointer		
0x15/21	SFE0 Timing Data L1 Trigger Latency (LAT_PRE)	R/W	20 words
	SFE0 ADC Data L1 Trigger Latency (ADC_DEL)		
	…		
	SFE9 LAT_PRE		

	SFE9 ADC_DEL		
0x16/22	SFE0 Trigger Data L1 Trigger Latency (L1_DEL)	R/W	20 words
	SFE0 L1 Self Test Trigger Latency (L1STRG_LAT)		
	…		
	SFE9 L1_DEL		
	SFE9 L1STRG_LAT		
0x17/23	SFE0 Test Pulse Amplitude	R/W	10 words
	…		
	SFE9 Test Pulse Amplitude		
0x18/24	SLP Delay0	R/W	24 words
	SLP Amplitude0		
	…		
	SLP Delay11		
	SLP Amplitude11		
0x19/25	Multi-block Data Transfer Destination Address	R/W	2 words
	Multi-block Data Transfer Byte Count		2 words
	Multi-block Data Transfer Checksum		1 word
	Multi-block Data Transfer Control		1 word
	Multi-block Data Transfer Status		1 word
0x1A/26	Multi-block WRITE	W	Up to 8 Kwords
0x1B/27	Multi-block READ	R	Up to 8 Kwords
0x1C/28	*NOT USED*	-	-
0x1D/29	*NOT USED*	-	-
0x1E/30	*NOT USED*	-	-
0x1F/31	MODE command	R	Mode Code

MODE COMMAND CODES:

MC		R/W	
0x09/9	Reset multi-block mode	(T/R = 1)	None
0x0A/10	Reset SRC	(T/R = 1)	None
0x0B/11	DSP Service Request	(T/R = 1)	None
0x0C/12	L2 & L3 FIFO Reset	(T/R = 1)	None
0x0D/13	SRC CLR_ERRS	(T/R = 1)	None
0x0E/14	SYSRESET	(T/R = 1)	None
0x0F/15	-	-	-

SubAddress	Register/Function	R/W	#words
0x00/0	*NOT USED*	-	-
0x01/1	SFE0 Group A Chan Enable Mask	R/W	6 words
	SFE0 Group A Analog Chan selection		
	SFE0 Group B Chan Enable Mask		
	SFE0 Group B Analog Chan selection		
	SFE0 Group C Chan Enable Mask		
	SFE0 Group C Analog Chan selection		
0x02/2	SFE1 Group A Chan Enable Mask	R/W	6 words
	SFE1 Group A Analog Chan selection		
	SFE1 Group B Chan Enable Mask		
	SFE1 Group B Analog Chan selection		
	SFE1 Group C Chan Enable Mask		
	SFE1 Group C Analog Chan selection		
0x03/3	SFE2 Group A Chan Enable Mask	R/W	6 words
	SFE2 Group A Analog Chan selection		
	SFE2 Group B Chan Enable Mask		
	SFE2 Group B Analog Chan selection		
	SFE2 Group C Chan Enable Mask		
	SFE2 Group C Analog Chan selection		
0x04/4	SFE3 Group A Chan Enable Mask	R/W	6 words
	SFE3 Group A Analog Chan selection		
	SFE3 Group B Chan Enable Mask		
	SFE3 Group B Analog Chan selection		
	SFE3 Group C Chan Enable Mask		
	SFE3 Group C Analog Chan selection		
0x05/5	SFE4 Group A Chan Enable Mask	R/W	6 words
	SFE4 Group A Analog Chan selection		
	SFE4 Group B Chan Enable Mask		
	SFE4 Group B Analog Chan selection		
	SFE4 Group C Chan Enable Mask		
	SFE4 Group C Analog Chan selection		
0x06/6	SFE5 Group A Chan Enable Mask	R/W	6 words
	SFE5 Group A Analog Chan selection		
	SFE5 Group B Chan Enable Mask		
	SFE5 Group B Analog Chan selection		
	SFE5 Group C Chan Enable Mask		
	SFE5 Group C Analog Chan selection		
0x07/7	SFE6 Group A Chan Enable Mask	R/W	6 words
	SFE6 Group A Analog Chan selection		
	SFE6 Group B Chan Enable Mask		
	SFE6 Group B Analog Chan selection		
	SFE6 Group C Chan Enable Mask		
	SFE6 Group C Analog Chan selection		
0x08/8	SFE7 Group A Chan Enable Mask	R/W	6 words
	SFE7 Group A Analog Chan selection		
	SFE7 Group B Chan Enable Mask		
	SFE7 Group B Analog Chan selection		
	SFE7 Group C Chan Enable Mask		
	SFE7 Group C Analog Chan selection		
0x09/9	SFE8 Group A Chan Enable Mask	R/W	6 words
	SFE8 Group A Analog Chan selection		
	SFE8 Group B Chan Enable Mask		
	SFE8 Group B Analog Chan selection		
	SFE8 Group C Chan Enable Mask		
	SFE8 Group C Analog Chan selection		
0x0A/10	SFE9 Group A Chan Enable Mask	R/W	6 words
	SFE9 Group A Analog Chan selection		
	SFE9 Group B Chan Enable Mask		
	SFE9 Group B Analog Chan selection		
	SFE9 Group C Chan Enable Mask		

	SFE9 Group C Analog Chan selection			
0x0B/11	SFE0: Threshold 0	Threshold 1	R/W	24 words
	…	…		
	Threshold 46	Threshold 47		
0x0C/12	SFE1: Threshold 0	Threshold 1	R/W	24 words
	…	…		
	Threshold 46	Threshold 47		
0x0D/13	SFE2: Threshold 0	Threshold 1	R/W	24 words
	…	…		
	Threshold 46	Threshold 47		
0x0E/14	SFE3: Threshold 0	Threshold 1	R/W	24 words
	…	…		
	Threshold 46	Threshold 47		
0x0F/15	SFE4: Threshold 0	Threshold 1	R/W	24 words
	…	…		
	Threshold 46	Threshold 47		
0x10/16	SFE5: Threshold 0	Threshold 1	R/W	24 words
	…	…		
	Threshold 46	Threshold 47		
0x11/17	SFE6: Threshold 0	Threshold 1	R/W	24 words
	…	…		
	Threshold 46	Threshold 47		
0x12/18	SFE7: Threshold 0	Threshold 1	R/W	24 words
	…	…		
	Threshold 46	Threshold 47		
0x13/19	SFE8: Threshold 0	Threshold 1	R/W	24 words
	…	…		
	Threshold 46	Threshold 47		
0x14/20	SFE9: Threshold 0	Threshold 1	R/W	24 words
	…	…		
	Threshold 46	Threshold 47		
0x15/21	SFE0 Group A Timing Gate		R/W	6 words
	SFE0 Group A Analog Gate			
	SFE0 Group B Timing Gate			
	SFE0 Group B Analog Gate			
	SFE0 Group C Timing Gate			
	SFE0 Group C Analog Gate			
0x16/22	SFE1 Group A Timing Gate		R/W	6 words
	SFE1 Group A Analog Gate			
	SFE1 Group B Timing Gate			
	SFE1 Group B Analog Gate			
	SFE1 Group C Timing Gate			
	SFE1 Group C Analog Gate			
0x17/23	SFE2 Group A Timing Gate		R/W	6 words
	SFE2 Group A Analog Gate			
	SFE2 Group B Timing Gate			
	SFE2 Group B Analog Gate			
	SFE2 Group C Timing Gate			
	SFE2 Group C Analog Gate			
0x18/24	SFE3 Group A Timing Gate		R/W	6 words
	SFE3 Group A Analog Gate			
	SFE3 Group B Timing Gate			
	SFE3 Group B Analog Gate			
	SFE3 Group C Timing Gate			
	SFE3 Group C Analog Gate			
0x19/25	SFE4 Group A Timing Gate		R/W	6 words
	SFE4 Group A Analog Gate			
	SFE4 Group B Timing Gate			
	SFE4 Group B Analog Gate			
	SFE4 Group C Timing Gate			
	SFE4 Group C Analog Gate			

0x1A/26	SFE5 Group A Timing Gate	R/W	6 words
	SFE5 Group A Analog Gate		
	SFE5 Group B Timing Gate		
	SFE5 Group B Analog Gate		
	SFE5 Group C Timing Gate		
	SFE5 Group C Analog Gate		
0x1B/27	SFE6 Group A Timing Gate	R/W	6 words
	SFE6 Group A Analog Gate		
	SFE6 Group B Timing Gate		
	SFE6 Group B Analog Gate		
	SFE6 Group C Timing Gate		
	SFE6 Group C Analog Gate		
0x1C/28	SFE7 Group A Timing Gate	R/W	6 words
	SFE7 Group A Analog Gate		
	SFE7 Group B Timing Gate		
	SFE7 Group B Analog Gate		
	SFE7 Group C Timing Gate		
	SFE7 Group C Analog Gate		
0x1D/29	SFE8 Group A Timing Gate	R/W	6 words
	SFE8 Group A Analog Gate		
	SFE8 Group B Timing Gate		
	SFE8 Group B Analog Gate		
	SFE8 Group C Timing Gate		
	SFE8 Group C Analog Gate		
0x1E/30	SFE9 Group A Timing Gate	R/W	6 words
	SFE9 Group A Analog Gate		
	SFE9 Group B Timing Gate		
	SFE9 Group B Analog Gate		
	SFE9 Group C Timing Gate		
	SFE9 Group C Analog Gate		
0x1F/31	*NOT USED*	-	-

	New/changed subaddresses

Scintillator Counters MIL-1553 Control/Status Records:

Crate names:

`CEB, CES, CET` - Central East
`CWB, CWB, CWT` - Central West
`NABET, NABWT, NABWB, NABEB, NCE, NCW` - Forward North
`SABET, SABWT, SABWB, SABEB, SCE, SCW` - Forward South

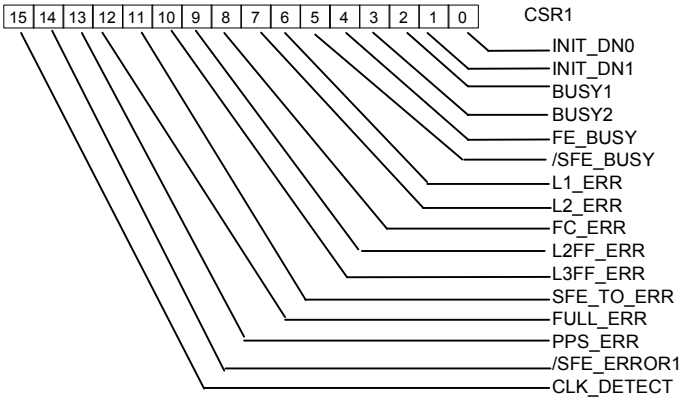
Record mil1553 "MUO_SRC_{crate_name}/AMON:R"
Crate Analog Data

Word #	Parameter	Equation
0	Crate temperature	ADC*0.32 C
1	SRC temperature	ADC*0.32 C
2	+5V monitor	ADC*0.039 V
3	-5V monitor	ADC*0.041 V
4	+12V monitor	ADC*0.096 V
5	-12V monitor	ADC*0.097 V

Record mil1553 "MUO_SRC_{crate_name}/CSR1:R"
SRC/SFEs Control Status Registers

From 6 to 11 words, depends on the crate, the first two words always present:

Word 0 is SRC CSR1 and contains various SRC status and error conditions.

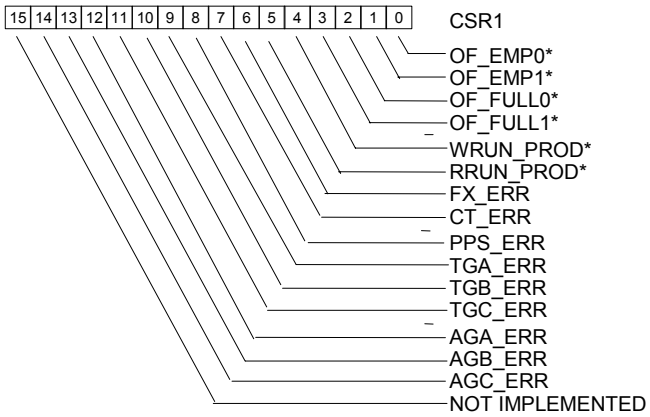


Bits	Signal Name	Message if ON	Message if OFF	Description
B2	BUSY1	L1 busy	No L1 busy	The DSP has determined that all SFE L1 Buffers are full
B3	BUSY2	L2 busy	No L2 busy	The DSP has determined that all L2 Buffers are full
B4	FE_BUSY	FE busy	No FE busy	SRC Readout Controller has detected that all SFE L1 Buffers are in use
B5	/SFE_BUSY	No SFE busy	SFE busy	One or more SFEs has detected that all its L1 Buffers are in use
B6	L1_ERR	L1 error	No L1 error	The DSP has detected an L1 data overflow
B7	L2_ERR	L2 error	No L2 error	The DSP has detected an L2 data overflow
B8	FC_ERR	FC error	No FC error	First crossing error found on SRC
B9	L2FF_ERR	L2 FIFO full	L2 FIFO OK	L2 Hotlink FIFO is full
B10	L3FF_ERR	L3 FIFO full	L2 FIFO OK	L3 Hotlink FIFO is full
B11	SFE_TO_ERR	SFE timeout	No SFE timeout	SRC Readout Controller detected an SFE timeout Error
B12	FULL_ERR	SFE buffers full	SFE buffers OK	SRC Readout Controller detected that the SFE L1 Buffer has been overwritten
B13	PPS_ERR	FPGA dnload Error	FPGA dnload OK	FLEX FPGA Download Error
B14	/SFE_ERROR1	No SFE error	SFE error	One or more SFEs has detected an Error
B15	CLK_DETECT	Encoded clock OK	No encoded clock	Encoded clock is present at the SRC

Word 1 is readout controller CSR1 contains error messages and runtime parameters for the SRC and its associated systems.

This word is not used for monitoring.

The next group of words (from 4 to 9) corresponds to the SFEs located in the crate, one word per SFE:



Bits	Signal Name	Message if ON	Message if OFF	Description
B6	FX_ERR	FC error	No FC error	An error was detected in the Master Controller's crossing counter (CROSSING) when compared to the actual FIRSTX
B7	CT_ERR	Coarse time error	Coarse time OK	An error was detected in the Master Controller's coarse time counter (CT_CNT)
B8	PPS_ERR	Flex cfg error	Flex cfg OK	An error was detected during the Flex 10K device configuration
B9	TGA_ERR	Trigger gate A error	Trigger gate A OK	A crossing overlap error was detected in the Group A Trigger Gate
B10	TGB_ERR	Trigger gate B error	Trigger gate B OK	A crossing overlap error was detected in the Group B Trigger Gate
B11	TGC_ERR	Trigger gate C error	Trigger gate C OK	A crossing overlap error was detected in the Group C Trigger Gate
B12	AGA_ERR	Analog gate A error	Analog gate A OK	A crossing overlap error was detected in the Group A Analog Gate
B13	AGB_ERR	Analog gate B error	Analog gate B OK	A crossing overlap error was detected in the Group B Analog Gate
B14	AGC_ERR	Analog gate C error	Analog gate C OK	A crossing overlap error was detected in the Group C Analog Gate

To clear errors two different records have to be used:

Record mil1553 "MUO_SRC_{crate_name}/RST:W" *SFEs Reset Registers*

Word #	Parameter	Value
0	Reset SFE boards	0
1	Clear latched errors	0000XXXXXXXXXX
2	Reset output FIFO read pointer	0
3	Reset output FIFO	0
4	Reset TMCs	0

Word 1 is a bit mask for the SFEs have to be cleared

Record mil1553 "MUO_SRC_{crate_name}/MODE:W" *Mode Command Register*

Count field equal to 13 - Clear SRC latched errors.

To reset the front-end crate:

Record mil1553 "MUO_SRC_{crate_name}/MODE:W" *Mode Command Register*

Count field equal to 14 - VME SYSRESET.