

D0 Muon Scintillator Electronics LED Pulser Module (SLP) Specification

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Revised:

1. Introduction

Figure 1-1 is a block diagram of the overall Muon Scintillator Front End System consisting of 6500 channels of Photomultiplier Tube (PMT) signals input to approximately 137 Scintillator Front End (SFE) modules, each having 48 channels. The SFE modules are housed in sixteen (16) 9U x 280 mm VME crates located on the D0 Platform and various places on the detector. Each crate contains a 680xx processor, a Scintillator Readout Controller (SRC) module, a Scintillator LED Pulser (SLP) module and approximately 10 SFE modules. The SFE modules accept and process event data from all crossings and, provides an event data buffer for Level 1 accepted events. The SRC collects and further processes Level 1 accepted event data from all SFEs in the crate. The SLP is a test module used to stimulate the scintillator counters producing PMT signals to the SFEs for testing purposes. A summary of SLP specifications is presented in Section 5.

Level 1 (L1) trigger data corresponding to HIT channels is sent directly from each SFE to the Muon Trigger system for each 132 ns crossing interval via a high speed serial link. Event data is processed and temporally stored for each crossing for as long as 4.7 μ s while the L1 trigger decision is made. The Muon Trigger system processes the scintillator trigger data along with that of other Muon subsystems and sends its decision to the Trigger Framework (TFW) which processes trigger data from the entire detector. The SRC module receives timing and trigger information about the L1 accepted events from the Trigger Framework via the Serial Command Link (SCL) and passes it on to the SFE modules. Identification of accepted events temporarily being stored in the SFE is determined by the arrival time of an L1 accept signal to within one crossing interval. Upon receipt of the L1 Accept, data from the accepted event is transferred to one of 16 buffer pages of a dual port memory comprising the SFE L1 Buffer. The SLP module accepts a programmable test trigger pulse from the SRC and drives LEDs whose outputs are distributed to various scintillator counters that produce input signals to the SFEs.

Transfer of event data from the SFEs to the SRC is initiated by the SRC immediately following an L1 Accept. The SRC addresses each SFE module in the crate which then outputs its data to one of 16 pages of a dual port memory on the SRC which serves as an L1 Buffer for the entire crate. After all modules have been read out, the Digital Signal Processor (DSP) on the SRC is notified that the

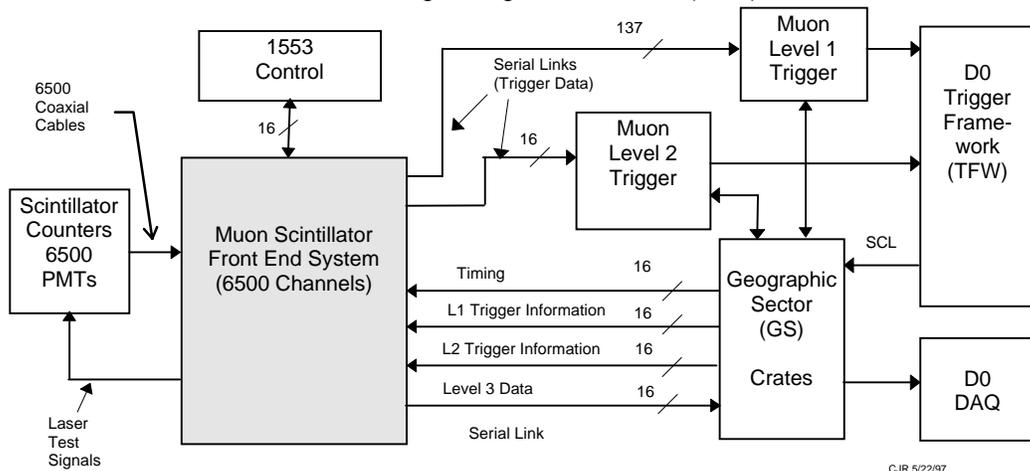


Figure 1-1 Muon Scintillator Counter System

event is ready for readout. The DSP reads reformats and transfers selected event data from the SRC L1 Buffer to a Level 2 (L2) trigger data queue for output to the Muon L2 Trigger System. The DSP awaits the L2 trigger decision from the Trigger Framework and reformats and transfers L2 accepted events to the Level 3 data queue for output to the MRC.

2. General Operational Description

The purpose of the LED pulser is to monitor the long term gain of the PMTs and timing stability of the scintillator system. In addition it provides a mechanism to determine the L1 decision time independent of the beam. Figure 2-1 is a block diagram of the SLP module whose functions are:

- 1) Accept an LVDS test pulse trigger from the SRC via the backplane.
- 2) Input Lemo front panel Nim external test pulse trigger
- 3) Use logical OR of external trigger and SRC trigger as input to 12 channels of LED driver with VME programmable amplitude.
- 4) BNC front panel output of each channel's LED driver signal.
- 5) VME controlled channel enable
- 6) Flash front panel display LED when channel is output.

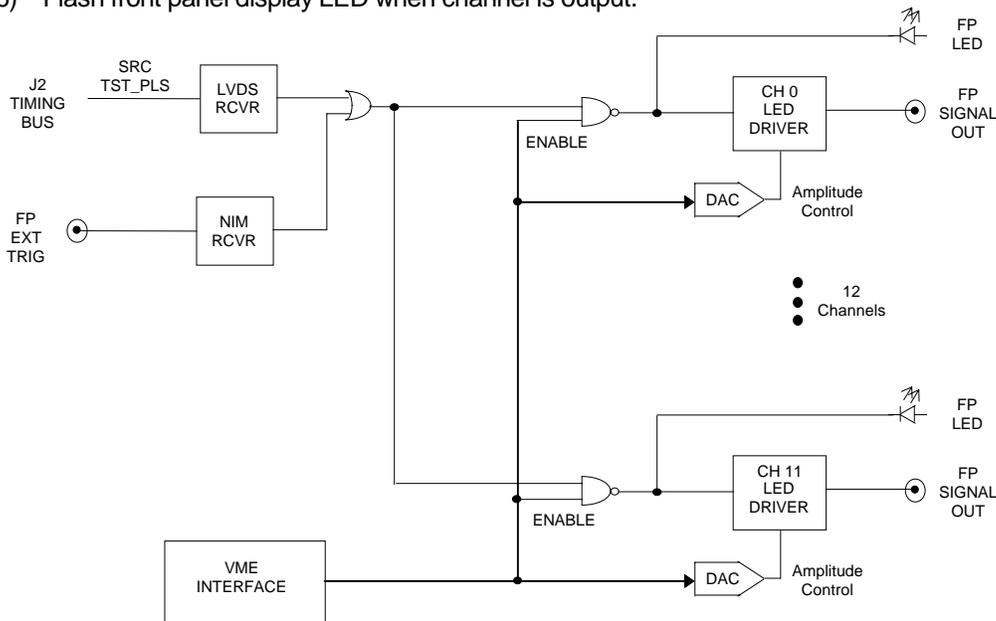


Figure 2-1 Block Diagram of SLP Module

3. LED Driver

The LED driver circuit shown in Figure 3-1 delivers a negative going differentiated pulse. The pulse amplitude is determined by the an 8 bit DAC under VME control and has a maximum value of 10 V. Lead edge rise time is expected to be 3 ns at the source but will be significantly larger at the LED depending on cable length ($\approx 50'$) and cable characteristics. The trailing edge fall time is controllable by values of RC and is selected to have a 25 ns time constant.

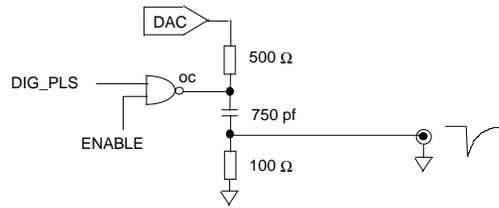


Figure 3-1 LED Pulser Circuit

4. VME Interface

The VME interface includes the following functions:

- 1) Twelve (12) channel amplitude control registers (8 bit R/W)
- 2) Channel Enable Register (12 bits R/W)

5. Specification Summary

Number of Channels	12
Pulse Characteristics	
▪ Amplitude 8 bit DAC	0 to -10v
▪ Leading edge rise time	< 3ns
▪ Trailing edge time constant	25 ns
▪ Polarity	negative
▪ Amplitude stability	<1%
▪ Channel to channel time skew	<1 ns
Mechanical	9U x 280 mm