

Muon Initialization Procedure

There is a difference in how muon front-ends (FE) handle INIT signal as it is described in the GS Specification. This document describes the difference and establishes a requirement for the muon front-ends during initialization.

According to the GS Specification each GS is required to respond to the INIT signal received from the D0 TFW by asserting an INACK signal and holding it active until GS's initialization is complete. Since there is no such signal defined in the muon front-ends this function will be performed by the Muon Fanout Card (MFC). In order to inform the MFC about initialization progress each muon FE is required to raise BUSY1 signal upon receiving INIT signal as soon as possible and hold it active until its initialization is complete. The MFC has access to backplane OR of all FE's BUSY1 signals. This product is used to check status of the FEs and reset INACK signal under software control. Figure 1 illustrates timing relationship between control signals during initialization. Note the difference when FE was busy transferring data at the time INIT is issued. In this case the BUSY1 signal stays active until data transfer and following initialization is complete.

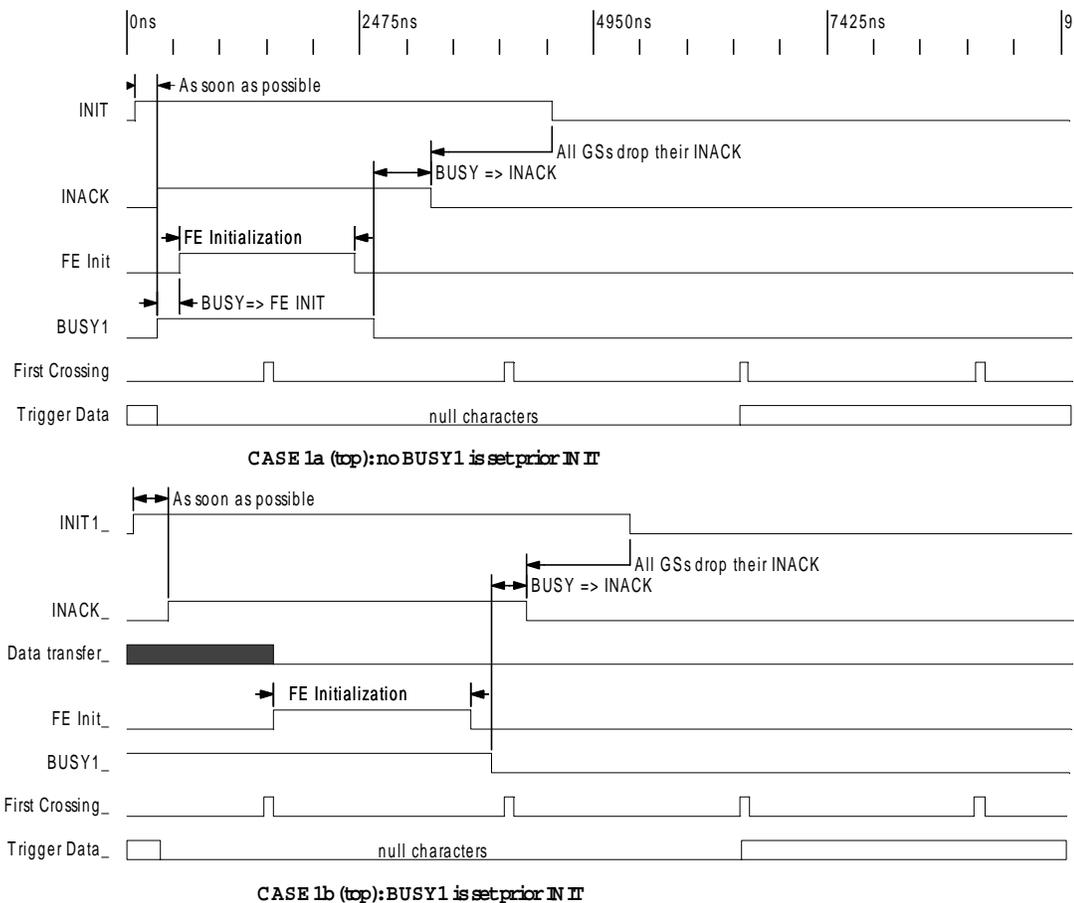


Fig.1. Muon front-end initialization timing.

Another specific procedure is the Cypress HotLink chip synchronization. After power-up and during initialization HotLink receivers have to be re-framed in order to guarantee receiver synch to

the incoming bit stream. This can be achieved by turning off transmitter enable signal (that will cause transmitter to transfer K28.5 pad characters) and enable RF (reframe) pin on HotLink receiver chip. There is hardware logic implemented in HOTLink control CPLD that automatically re-frames receiver and reports status in the MRC status register. The HOTLink re-frame can be triggered by software after the trailing edge of the BUSY1 signal with INIT signal active (Fig.2). In the MFC design, the INACK signal is reset by a bit in the status register allowing additional delay for re-framing.

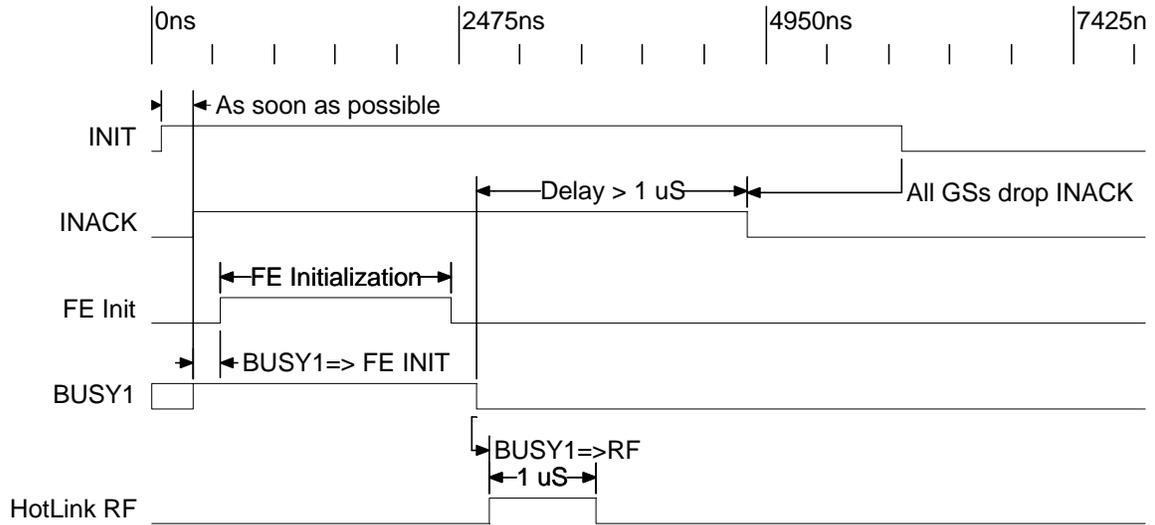


Fig.2. HotLink reframe timing.