

## I. MUON READOUT

The common strategy for the muon detector subsystems readout includes use of common interface modules, unified data formats, and diagnostic and data processing tools. All muon readout units are based on the same DSP processor to perform readout, buffering and formatting of the data and use the same serial link transmitters to transfer L1, L2 and L3 data [8]. A unified approach to provide diagnostic and calibration tools at different levels of implementation has been developed and is discussed later on in this chapter. The Muon Readout Card (MRC) is designed to provide control and data readout for all muon subsystems. The Muon Fanout Card (MFC) provides an interface between muon Geographic Sectors (GS) and D0 Trigger Framework.

### A. DSP Data Processing and Buffer Management

The D0 DAQ specification stipulates that all front ends implement 16 L1 and eight L2 buffers to store events corresponding to the appropriate TFW decision (Fig. I-1). Each GS is required to have a pipeline to store incoming events until a TFW decision is made. The minimum pipeline delay is determined by the Level 1 decision time of  $3.56 \mu\text{s}$  (at the TFW location) and the signal propagation time from the TFW to the GS. Each GS must have the ability to store events accepted by the TFW. Events accepted by L1 and L2 decisions are stored in Level 1 and Level 2 buffers. L2 Reject discards the event from the Level 2 buffer. The muon system buffering scheme follows the D0 specification by implementing flexible DSP based control of the event buffering. A simplified diagram of the muon buffering scheme is shown in Fig. I-2.

A continuously running digitizer generates output information synchronously with the Tevatron RF. A digital pipeline delay, running synchronously with the digitizer is preset to the TFW Level 1 trigger decision time. When the L1 accept arrives at the front end, corresponding event information appears at the delay output and is transferred to the L1

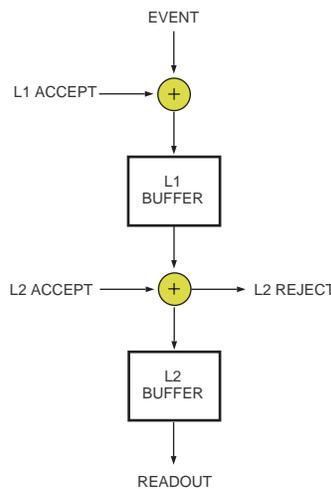


Fig. I-1. D0 buffering scheme.

FIFO. After that, the event information can be asynchronously read out by the readout logic and stored in the intermediate L1 buffer within the DSP memory. From this point on, the DSP takes control of both processing and buffering.

The specified maximum for Run II is about 10 kHz for the L1 trigger rate and 1 kHz for L2. An average interval of 100  $\mu$ s is thus available for transferring an event from the output of the delay to the L1 buffer. In the muon system this process takes about 1.5  $\mu$ s maximum. This deadtime makes no contribution to the DAQ deadtime because, for other reasons, the minimum interval between Level 1 triggers is 2.6  $\mu$ s.

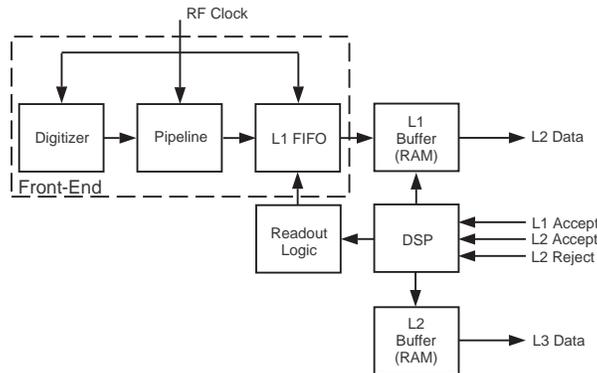


Fig. I-2. Muon system buffering scheme. DSP - digital signal processor.

The Analog Devices simulator for the ADSP-2181 processor operating at 33 MHz has been used to estimate how long it will take to process and format the data before sending it to the MRC. Physics simulations of the Run II scenario show that the expected occupancies for the PDTs, scintillation counters and MDTs are 3%, 1% and 0.5% respectively. We use 10%, 10% and 1%, since accurate occupancy estimates are impossible without real background measurements.

For the PDT front ends, assuming a 10% occupancy, the correction of the time scale, pedestal subtraction and gain correction will take about 12  $\mu$ s. A calculation of pad electrode charge ratios to determine the second coordinate will take about 8  $\mu$ s. The time to readout and transfer an event to the MRC is estimated to be 12  $\mu$ s and 6.2  $\mu$ s respectively for a total of 38.2  $\mu$ s or 3.8% of the average interval between two L2 accepts.

The event size for the scintillation counters is smaller than for the PDTs. The ten SFE cards that will be placed in one VME crate will produce about 30 16-bit words per event assuming 10% occupancy. This will take about 12  $\mu$ s to readout, 15  $\mu$ s to correct  $t_0$  and convert bins to nanoseconds and 4.2  $\mu$ s for the transfer to the MRC. Thus, total front-end data processing takes about 31.2  $\mu$ s.

The MDC drift time data, which is not zero-suppressed, has an event size fixed at 108 64-bit words and is the largest of the three detector subsystems. The readout controller will sparsify and reformat the data into 16 bit form, a process estimated to take 10.2  $\mu$ s. For the MDTs the average occupancy is expected to be in the range of 0.5% to 1%.

Assuming 1% occupancy, the simulation shows that to convert bins to nanoseconds and to correct  $t_0$  will

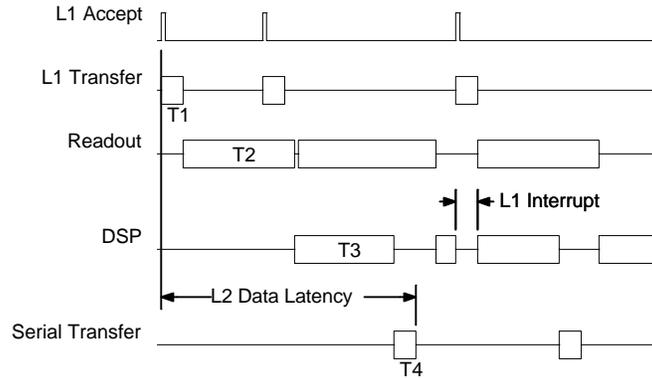


Fig. I-3. L2 data processing timing diagram. T1, T2, T3 and T4 correspond to the data processing times shown for one event.

take about 6.4  $\mu$ s. The transfer time to the MRC is about 2.5  $\mu$ s. The front-end data processing takes about 19.2  $\mu$ s.

The DSP also performs L2 data processing and formatting, which is time critical. Based on queuing simulation of the D0 data acquisition system [9], L2 data latency cannot exceed 30  $\mu$ s without introducing additional dead time. The typical L2 processing times are shown in Fig. I-3. We have estimated that for conservative occupancies of 10%, 10% and 1% described above the following processing times can be achieved (See Table I-1).

Table I-1. L2 data processing times in  $\mu$ s.

| Detector  | T1  | T2   | T3   | T4  | total |
|-----------|-----|------|------|-----|-------|
| PDT @ 10% | 1.5 | 12.0 | 12.0 | 3.0 | 28.5  |
| SC @ 10%  | 0.6 | 12.1 | 7.0  | 5.4 | 25.1  |
| MDT @ 1%  | 0.1 | 10.2 | 6.4  | 2.5 | 19.2  |

For event buffer management, every trigger decision causes a DSP interrupt and is used to store associated information in the synchronization logic (Fig. I-4). If there was an L1 Accept, the DSP checks if the TFW crossing number corresponds to the local crossing number provided by the synchronization logic. In the case of a mismatch an ERROR 1 signal is generated. If there was an L2 Accept or L2 Reject, the DSP checks the corresponding number associated with the event stored in the L1 buffer. In this case, a mismatch generates an ERROR 2. The DSP also checks the status of its buffers and generates BUSY 1 or BUSY 2 signals when appropriate.

An event accepted by L1 is collected from the front-end L1 buffers by subsystem specific readout logic and written into the DSP memory. The DSP then processes and formats the data according to the requirements of the L2 trigger system. After processing, the data is sent to L2. An L2 Accept causes the DSP to process the event according to the L3 system requirements, buffer the event and wait for permission to transfer it to the MRC card for final event building in the muon readout crate. An L2 Reject discards the event, freeing up one L2 buffer. Our estimates show that all the necessary buffer management

including interrupt handling can be done using the ADSP-2181 within 1.5  $\mu$ s. As one can see, the processing times are within the required ranges and we conclude that using the

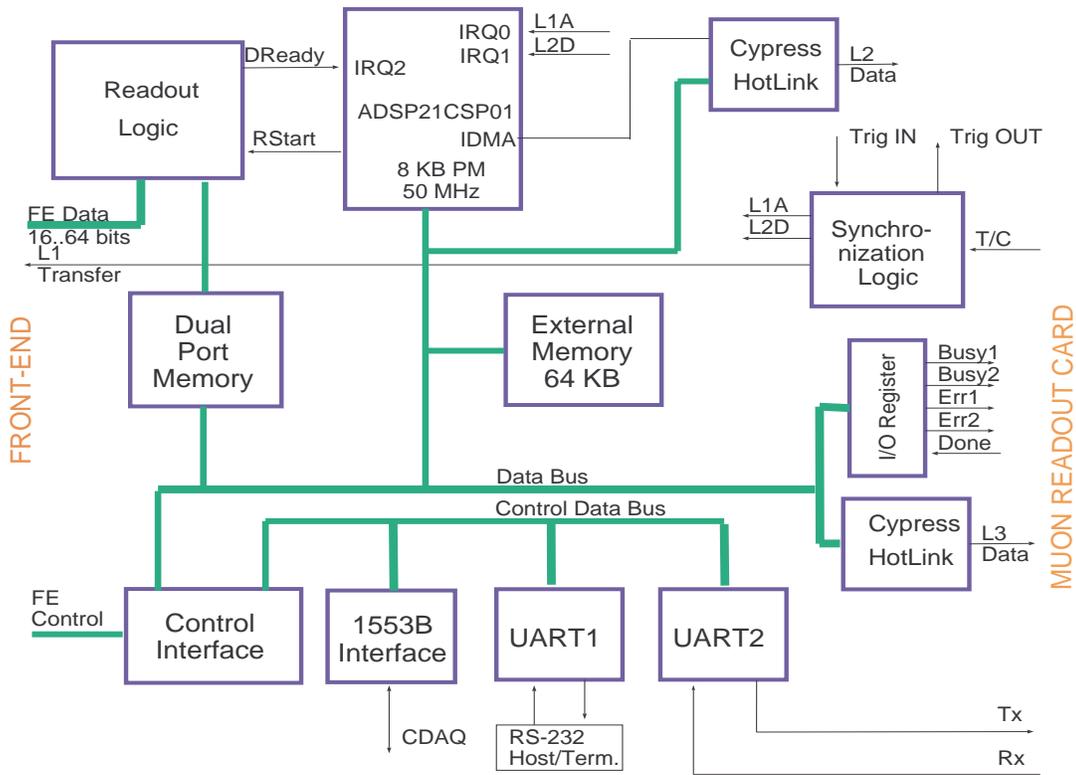


Fig. I-4. Simplified block-diagram of the muon readout controller. L1A - Level 1 Accept, L2D - Level 2 Decision.

DSP to perform these tasks will have a negligible impact on the D0 DAQ system deadtime. The newer version of the Analog Devices DSP processor ADSP21Csp-01 is implemented in the muon readout controller design because of a larger address space and higher performance. This processor has a clock frequency of 50 MHz and external memory up to 64KB for event buffering.

## B. Diagnostic and Calibration Tools

### B1. Diagnostic Modes of Operation.

There are several types of diagnostic operation provided within the muon system which can be described as follows:

#### Pulsing:

All front-end channels (PDT, MDT, and scintillator) are equipped with internal pulsers. The test pulses themselves are generated on the Front-End Units: Front-End Board (FEB) for the PDTs, Scintillator Front-End Cards (SFE) for scintillator, and Mini-Drift Digitizing Cards (MDC) for the MDTs. The enabling, delay and amplitude adjustments of these pulsers are controlled from

the Control Units: the Control Boards (CB) for the PDTs, Scintillator Readout Controllers (SRC) for the scintillators, and the MDT Readout Controllers (MDRC) for the MDTs. For the MDCs, there are actually two sets of pulsers: an analog pulser located on the Amplifier Discriminator Boards (ADBs) and a logical pulser that directly pulses the inputs on the MDC. The SFEs have an external test pulse option similar to the ADB test pulse which is an LED pulser simulating scintillator light on the PMT photocathode. The pulser signals are broadcast to all of the front-end channels on a given Front-End Card/Board, but any pattern of active channel outputs can be configured by downloading the appropriate channel enable mask. The SFE has two internal types of test pulses: an analog pulse injected at the SFE input and a digital pulse applied to the TMC inputs which can be enabled for testing of the appropriate part of the module.

#### Self-triggering and external triggering:

All front ends have the ability to self-trigger on single channels (noise, cosmics, etc.). In addition, each Control Unit has an external trigger input which can be used to initiate data readout.

#### B2. Diagnostic Data Processing.

The data from diagnostic running or calibration can be analyzed by the front-end Digital Signal Processor (DSP), or the VME processor in the readout crate, or the Level 3 nodes, or the host computer. The VME processors are Motorola 680xx based single board computers. There are a number of legacy 68020 (Omnibyte VSBC-20) based modules left over from Run I which will be predominantly used in the collision hall VME crates. The muon readout crates will be equipped with newer, higher performance CPU cards based on the Motorola 68040.

#### B3. Levels of Testing.

We anticipate five levels at which diagnostics and calibrations might take place. We list these starting from the most local to the most global level, which is probably the order in which these tools will be developed.

#### Front-End Level:

Each Control Unit will be equipped with a DSP, which has 96 Kbytes of program and data memory. The primary purpose of the DSP is to buffer the data from the front end while a Level 2 decision is pending. The DSP, however, can run diagnostic sequences when it is not in data taking mode. These diagnostics can involve the pulsers, or self-triggering on noise or cosmics. The DSP can accumulate statistics on each channel and later pass the results up through the readout system. It may also be possible for the DSP to calculate calibration constants and store them in its memory. In any case, it is anticipated that the calibration constants will be available to the DSP when it is

formatting and buffering data, so that it may do pedestal subtraction, etc. The DSP will be able to control the pulser lines, thus allowing event data to be processed before triggering the next event. In this way, each DSP could be performing independent diagnostics/calibration on each module at any time when the experiment is not taking data.

Systems required:

- Detector module (or pulser)
- Front-End Unit
- Control Unit

#### Readout Crate Level:

As in Run I, each readout crate will have a VME processor. This device could run programs to accumulate data from any of the MRC's in the crate, just as it did from the MAC cards in Run I. This would be the Run II version of "daq\_local". The RS-232 port on the VME processor can be connected to a terminal to provide a control interface and display results. An Ethernet interface, if available, could also be used for this purpose.

Systems required:

- Detector module (or pulser)
- Front-End Unit
- Control Unit
- MRC and readout crate

#### Readout Crate and Vertical Interconnect (VI) Level:

This is the same idea as the popular "mu\_local" (aka "VAX\_local") program of Run I. The VME processor will still manage the accumulation of data as in "daq local", but instead of analyzing the data itself, it will pass it on through the Vertical Interconnect and the Token Ring to the host computer for more sophisticated analysis and optional recording of events.

System required:

- Detector module (or pulser)
- Front-End Unit
- Control Unit
- MRC and readout crate
- Vertical Interconnect
- Host computer

#### Multiple Readout Crates and Vertical Interconnect Level:

A deficiency of test triggering in Run I was the inability to coordinate the data taking from multiple muon crates without using the D0 DAQ system. A special Trigger Fanout Card (TFC) described later in this chapter, allows for multiple crate synchronization. It distributes a specific sub-set of the TFW timing and control signals which can originate from any of the MFCs. This module must be connected to all the MFCs included in the particular local configuration.

System required:

Detector module (or pulser)  
 Front-End Unit  
 Control Unit  
 Multiple MRCs and readout crates  
 TFC connected to these crates  
 Vertical Interconnect  
 Host computer

#### D0 DAQ Level:

Here, the triggers will be managed by the TFW and the data will be read out in the normal way through the VBD onto the data cables. This requires the resources of essentially the whole D0 data acquisition system. This is the mode in which calibration was done in Run I. Synchronization of the various elements might not be trivial.

Systems required:

Detector module (or pulser)  
 Front-End Unit  
 Control Unit  
 MRC and readout crate  
 VBD  
 Level 3  
 Trigger framework  
 D0 DAQ  
 Host computer

#### B4. Details of Local Triggering

Local triggering is an important tool for diagnostics and was heavily used in Run I. In this mode, the front ends are running continuously, until some simple condition is satisfied in the detector, such as the firing of one channel. This local trigger is sent to the Control Unit. The Control Unit can generate its own Level 1 and Level 2 accepts and rejects, so the flow of data is controlled locally. The control unit reads the data from the front end and can then either send the data to the MRC for readout, or apply more sophisticated requirements using the DSP and only send out the event satisfying these stricter conditions. The Control Unit notifies the MRC that it has data to be read out either over the standard HOTLink data connection from the FE to the MRC, or over the UART serial link. The trigger is passed from the MRC to the MFC via the VME backplane, and the MFC then generates the VME interrupt and the processor coordinates the readout.

For all FEs there is an internal trigger condition provided by means of channel ORs. This signal will trigger the readout and possible data processing. The DSP in the FE will be able to analyze the event and either store it or discard it, and enable the next trigger. Individual channel masking allows for generating any trigger pattern. More sophisticated trigger conditions could also be implemented in the DSPs. Early estimates indicated that a multi-deck coincidence algorithm, for example, could be executed in the DSP in a time around 10..50  $\mu$ s.

The PDT FEB generates a 24 channel OR and transfers it to the Control Board. The CB has four maskable inputs which are in turn OR'ed to produce a global PDT internal trigger.

Each MDC has an OR of the 192 channels on that card. Each MDRC will see the local triggers from up to 12 MDCs, and these will feed in to a programmable AND-OR network.

The scintillator will operate similarly to the MDTs. The SFEs will generate triggers corresponding to the OR of 48 PMT latches. These will feed in to an AND-OR network on the SRC. Since there is only one deck of scintillation counters in a given layer, there is no obvious desire for implementing coincidence logic.

As mentioned earlier, each Control Unit will have an external trigger input. This could be used, for example, to feed in the trigger from a cosmic ray telescope for chamber testing in the assembly hall. The external trigger would be the equivalent of the n-deck coincidence signal from the front ends in the case of the PDTs, and the equivalent of the output of the Control Unit trigger AND-OR network in the case of the other detectors. In addition, each control unit will have a trigger output, with the same equivalence relationship. This allows for such possibilities as using a local trigger from the MDTs to read out a nearby group of scintillators, or vice versa.

#### B5. Rate Limitations

In general, the readout rate limitations for each level of testing will depend on the size of the events and the complexity of the algorithms used in the diagnostics. Some rules of thumb can be given for approximating the maximum event rate. For the DSP level readout, the time spent can be estimated as follows:

1. Two cycles/word for shift from input FIFO to buffer
2. Two cycles/word for shift from buffer to output FIFO
3. Overhead per data set (10-50 cycles)
4. Two cycles/word for any additional operation on each data word (e.g. pedestal subtraction)

Each cycle takes 20 ns for the ADSP21csp-01. The absolute minimum is the sum of 1, 2, and 3 above; 4 depends on the specific task. The timing for any specific algorithm can be determined with the DSP simulator.

Transfers from the DSP to the MRC can go at 16 Mbytes/sec (125 ns/word), so this rate limit is very similar to that imposed by the DSP. Consequently, the maximum rates should be similar for the first two modes of diagnostic readout.

Transfer of events out of the readout crate is considerably slower. The Vertical Interconnect, Token Ring, and Gateway together limit the transfer rate to about 5 ms/word. The rate can be further constrained if the Gateway is shared with other processes. In Run I, we typically ran in this mode at 10's of hertz without any problem for small local cosmic events.

In local triggering on cosmic rays, the events tend to be very small (3 or 4 hits/event) and the event rate is usually limited by the actual cosmic flux rather than any bottlenecks in the readout. Pulsing mode is the other extreme, where the occupancy can be 100%. The fastest possible readout to the MRCs would be about 10kHz for pulsing a single module, or 1kHz for pulsing a crate of MDTs or scintillators. Such events could be transferred out through the VI at a maximum rate of about 200 Hz for a single module. Faster readout is possible through the VBD to the data cable, but more system resources are required for this mode.

In diagnostic and calibration applications, events are usually analyzed in real time and are not written to disk. The rate limitations above do not take into account the time required for analysis done on the events in the DSP , VME processor, L3 node, or host computer; only such things as buffering and formatting are included in these baseline numbers. In practice, the analysis processing time is most likely to be the rate limiting step for calibration pulsing.

## B6. Software Development

So far, little work has been done on a software for Run II diagnostics and calibration. Some of the code from Run I might be salvageable, but much new code has to be written:

### DSP:

The DSP is a new item, so no code exists from Run I. The standard readout mode code is in development now. The code for diagnostic modes has not been started.

### VME processor:

Since the VME processors will be reading out MRCs instead of ADCs and MACs, that part of the code has to be rewritten. Some of the daq\_local histogramming and user interface code might be salvageable. The server (client?) for the VI might be reused as well. Of course, the data format will change, and the code must reflect that. We expect that the time critical parts of the code will be written in 68K assembly language. Compilers also exist for C and C++, and these might be more appropriate for writing the user interfaces, etc.

### Host computer:

It is believed that the CDAQ protocol will still be used for communicating between the host computer and the Token Ring. This would mean that the host side interface of mu\_local might have to undergo little change. Hopefully , many of the nice features of mu\_local can be salvaged (histogramming, event displays, etc.) although the old graphics package (DI3000), user interface (COMPAC) and host operating system (VMS) will probably all have to be changed. In addition, the mu\_local code will have to be extended to give appropriate displays and histograms for the new detectors which did not exist in Run I.

The program comm\_tkr will be maintained and can be used to download commands to the VME processors and settings to the 1553's Remote Terminals on the Control Units. This is an experiment wide utility provided by the on-line software group. The hardware

database is currently based on a VMS specific implementation of RDB. This will have to be replaced. In the mean time, there is the hope that some means of using the physical hardware addresses for downloading will be available.

The data acquisition framework for full system calibration is also an experiment wide utility; we expect the on-line group again to provide the "calib" framework in Run II. Exactly what the host computer will be is still uncertain, but Windows and Unix are strong candidates for the operating system.

### *C. Muon Readout Card.*

#### C1. Introduction.

The Muon Readout Card (MRC) is a part of D0 Muon Readout System and provides an interface between D0 DAQ and muon front ends. The Muon Readout Cards are located in readout crates in the Movable Counting House (MCH). We use existing 9U X 280mm VME crates with custom back-planes to minimize the cost of the upgrade. Having only sequential logic and no processor the MRC performs the following functions:

- Receives data from front-end electronics (FE) and buffers it in internal RAM;
- Provides an alternate (as opposed to MIL-1553B) control path to the FE digital signal processor (DSP) via a universal asynchronous receiver/transmitter (UART)
- Transfers timing and control signals from Muon Fanout Card (MFC) to FE and status information from FE to MFC.

Each MRC has two independent identical sections (A and B) connected to two front-end units. A block diagram of the MRC is shown in Fig. I-5. The data is transferred from the front-end readout controller via copper coaxial cable using a Cypress HOTLink chipset (CY7B923/933). We use its lowest frequency setting of 160 Mbit/s to accommodate our transmission line bandwidth. With 360 feet of coaxial cable we have achieved error free transmission using an active cable compensation chip. The MRC receives 16 timing and control signals from the Muon Fanout Card and transmits five status signals.

Each MRC section includes an eight Kbyte dual port memory buffer for data storage, a 32 bit status/control register, a serial communication controller (SCC) to communicate with the DSP processor and transmitters and receivers for 20 control and timing signals in each section. A VME slave interface and the transmitters and receivers for the J2 backplane are common for both sections. Sixteen control signals are transmitted to and from the front-end readout controller using twist and flat cable. Three timing signals encoded into one line, Tevatron RF and serial data are transmitted on three coaxial cables whose length is typically 280 feet.

For the twist and flat cable, differential current drivers are used at the transmitter end, and current feedback amplifiers and high speed comparators are used at the receiver end. The amplifiers have a feedback compensation adjusted for the cable attenuation. A Comlinear cable driver and cable equalizer operating in PECL (Positive ECL) mode are

used at each end of the coaxial cable for driving and receiving differential signals. To reject common mode voltages between the receivers and the transmitters, RF transformers are used to convert from differential to single ended at the transmit end and back at the receive end.

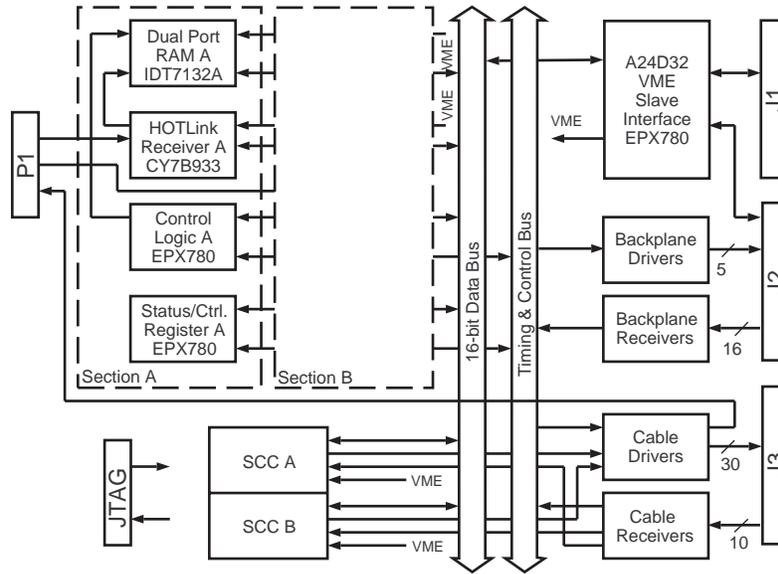


Fig. I-5. Muon Readout Card. VME - VME command, SCC - Serial Communication Controller.

Two special control characters are used to indicate the beginning and end of the data transmission. A K28.0 character indicates beginning of the event and K23.7 character is the end of event data marker. These characters are used by the HOTLink control logic implemented in the first prototype in an Altera FLASHLogic chip to initialize its address register and will not be stored. The HOTLink chips use K28.5 pad characters to keep the receiver synchronized with the transmitter and to align the incoming bit stream. The control logic ignores these characters which allows an intermittent byte stream to be sent. There is a time-out counter preset to 4 ms to prevent 'hanging' of the link.

Event data from the HOTLink receiver is written into one port of the memory, while the second port is accessible to VME for both writes as well as reads. The status register includes BUSY and ERROR signals coming from the front-end readout controller and a set of control and status bits. BUSY 1, BUSY 2, ERROR 1, ERROR 2 and the SERVICE REQUEST signals are wire ORed on five J2 backplane lines and transmitted to the MFC. Each of these signals may interrupt the VME processor using the interrupt controller in the MFC. The SERVICE REQUEST is the OR of internal interrupt sources which include the HOTLink control logic and the UARTs.

A Zilog Z16C30 Serial Communication Controller (SCC) is used in the first MRC prototype. It provides a 1 Mbit/s data rate which has been tested using the cable connection described earlier. The SCC has two independent sections each of which uses two 16 bit access VME addresses. A faster SCC (AM85C30) with a 2.5 Mbit/s transfer rate will be used in the final design.

Each MRC consists of several functional units which are described in the subsequent paragraphs.

## C2. HOTLink Receiver CY7B933 and its Control Logic.

HOTLink Receiver CY7B933 in MRC and HOTLink Transmitter CY7B923 in the FE are point-to-point serial links used for transferring data at 160 M Bit/sec in one direction from FE to MRC.

The HOTLink receiver accepts a serial bit stream and, using an integrated PLL clock synchronizer, recovers the timing information necessary for data reconstruction. To properly align the incoming bit stream to byte boundaries, a counter tracking bits within a byte must be initialized. The framing logic block in CY7B933 checks the incoming bit stream for a unique pattern that defines the byte boundaries. This logic looks for a K28.5 character. Once found, the counter in the Clock Sync block is synchronously reset, thus "framing" the data to the correct byte boundaries. The bit stream is de-serialized, decoded, and checked for transmission errors. The recovered byte is presented in parallel form at the byte rate (16 MHz).

The Framing Logic in the Receiver is controlled by the Reframe Enable (RF) input signal on the CY7B933. When RF is held HIGH, each SYNC character (K28.5) is detected, the shifter will frame the data that follows. When RF held LOW, the reframing logic is disabled. The incoming data stream is then continuously deserialized and decoded using byte boundaries set by the internal byte counter. Bit errors in the data stream will not cause alias SYNC characters to reframe the data erroneously.

Eight bits of data are loaded into the HOTLink Transmitter in the FE then serial data is shifted out of the differential Positive ECL (PECL) serial port and transmitted over the coaxial ASTRO cable. At the MRC the signal is transformer coupled to a Comlinear CLCO14 receiver chip which then drives the HOTLink receiver input.

The reference clock frequency for the clock/data synchronizer is 16 MHz. A LOW on the Data Output Ready (RDY) pin of HOTLink Receiver indicates that new data has been received and is ready to be delivered. A missing pulse on RDY shows that the received data is a pad character.

The data outputs (Q0-Q7, SC/D and RVS) all change state simultaneously, and are aligned with RDY and CKR within specified limits, and are interfaced directly to external memory (in our case, a dual port RAM).

The HOTLink Control Logic on the first prototype is contained in one Altera EPX780 for each FE but will be implemented with Philips PZ or Altera 5000 series CPLD chips in the final design. The Control Logic contains an 8-bit register for the HOTLink outputs clocked by the RDY pulse, a 12-bit RAM Address Counter, a 16-bit Time-out Counter and logic for controlling both the HOTLink and the transfer of data from the CPLD to the appropriate RAM chip.

The DSTREAM bit is set on receipt of a K28.0 character and reset upon receiving a K23.7 character. The Dual port RAM Address Counter is incremented on the edge of the RDY pulse and cleared on receipt of a K27.3 character. The MRESET and RESET pulses originating from the on-card Control and Status Register (CSR) as well as the pulse

INIT\_FR generated from the INIT signal also serve to reset DSTREAM and clear the RAM Address Counter. Overflow of the RAM Address Counter disables any further writes to RAM, freezes the counter value and sets the OVF\_DSTR bit in the CSR.

When INIT is issued by the TFW, the HOTLinks are re-framed by the INIT\_FR signal. The REFRAM bit is set and the RDY pin is checked after a four clock cycle delay (see the HOTLink description). The RDY signal coming after this delay sets the REFD bit in the CSR indicating the reframe ended and resets the REFRAM bit.

In Built-In-Self-Test (BIST) Mode, enabled by the BISIN bit in the CSR, the BISTEN bit is set low and the HOTLink Receiver CY7B933 switches to BIST mode. The BIST loop consists of a 511 byte transfer. Reframing in this mode is done in the same manner as described above. If there no invalid codes were detected during BIST, the BISOK bit is set indicating that BIST has run without errors.

A 16-bit Time-Out Counter (approximately 4 ms span in our case) is incremented by the HOTLink CKR clock signal. The MRESET, RESET bits in the CSR, the INIT\_FR from the TFW, and receipt of a K23.7 character all reset BISTEN and set REFD. If the Time-Out Counter is not reset after normal termination of the current operation, the TOUT bit is set after 4 ms. Separate condition bits identifying the various sources of time-out (TOUT\_DSTR, TOUT\_REFR and TOUT\_BIST) are implemented in the CSR.

If an invalid symbol was received during DSTREAM or BIST the corresponding bit in the CSR (RVS\_DSTR or RVS\_BIST) is set.

### C3. Two-channel High-Speed Serial Communication Controller AM85C30.

The SCC is intended for direct communications between the VME processor in the muon readout crates and each of the DSPs in the FE. This connection is necessary for exchanging data between FE and a VME processor for testing and diagnostic operational modes. We plan to replace Zilog Z16C30 dual-channel SCC presently implemented on the first prototype with an AMD AM85C30 which has a higher transmission rate (2.5 Mbits/s).

The Zilog SCC is used in MRC in 16-bit non-multiplexed mode. In this case all internal registers in each channel are accessed indirectly using the address pointer in the Channel Command/Address Register (CCAR) in each channel. The address of the desired register is first written to the CCAR and then the selected register is accessed; the pointer in the CCAR is automatically cleared after this access. The Transmit Data Register (TDR, write only) and Receive Data Register (RDR, read only) are accessed directly using the separate D/C pin, without disturbing the contents of the pointer in the CCAR.

There are six sources of interrupts in each channel of the SCC: Receive Status, Receive Data, Transmit Status, Transmit Data, I/O Status and Device Status, arranged on the internal interrupt daisy chain in this priority order. The SCC doesn't require Interrupt Acknowledge Cycles (but supports this mode), so /SITACK and /PITACK input interrupt acknowledge pins are simply pulled up. Software can read the Interrupt Pending (IP) and Interrupt Under Service (IUS) bits in the Daisy Chain Control Register (DCCR).

The AM85C30 is an enhanced serial communications controller designed for use with any conventional 8-bit bus. The device contains two independent, full duplex channels,

two baud rate generators per channel, a digital phase-locked loop per channel, character counters for both receiver and transmitter in each channel, and 32-byte data FIFO for each receiver and transmitter.

**C4. Eight Kbyte Dual Port RAM.**

The Dual Ported RAM holds data from one event from the each FE. The RAM has a maximum size of 8 Kbytes and is implemented with 2Kx8 Dual-Port Static RAM chips. There are four such chips for every FE interface section. The bytes of data from CY7B933 (HOTLink) are written sequentially to port A of memory chips. Port B of these chips is available for writing and reading from VME.

**C5. Communications between MRC and MFC.**

There will be one Muon Fanout Card (MFC) and 11 to 13 MRCs in each muon readout crate. Each MRC receives 15 signals from and transmits five signals to the MFC (see Table I-2). Two fast signals from the MFC are transmitted to the MRCs using differential PECL lines. Synergy SY10ELT22 PECL differential transmitters are used in the MFC and Motorola MC10116 differential line receivers are used in the MRCs for these signals. The other signals from the MFC (INIT, L1ACC, L1REJ, L2ACC, L2REJ and Xing<0-7>) are TTL levels. 74FCT16244 16 bit latches are used as receivers for these signals.

Table I-2. MRC interconnections in the VME crate..

| <b>Signal</b>  | <b>Source</b> | <b>Dest.</b> | <b>Type</b> | <b>Transmitter</b> | <b>Receiver</b> |
|----------------|---------------|--------------|-------------|--------------------|-----------------|
| RF 53 MHz      | FO            | MRCs         | PECL lines  | SY10ELT22          | CLC014          |
| Encoded Timing | FO            | MRCs         | PECL lines  | SY10ELT22          | CLC014          |
| INIT           | FO            | MRCs         | TTL line    | FCT16244           | FCT16244        |
| L1 ACC         | FO            | MRCs         | TTL line    | FCT16244           | FCT16244        |
| L2 ACC         | FO            | MRCs         | TTL line    | FCT16244           | FCT16244        |
| L2 REJ         | FO            | MRCs         | TTL line    | FCT16244           | FCT16244        |
| Xing #         | FO            | MRCs         | TTL lines   | FCT16244           | FCT16244        |
| ERROR1         | MRCs          | FO           | OC, wire OR | 74BCT760 (OC)      | FCT16244        |
| ERROR 2        | MRCs          | FO           | OC, wire OR | 74BCT760 (OC)      | FCT16244        |
| BUSY 1         | MRCs          | FO           | OC, wire OR | 74BCT760 (OC)      | FCT16244        |
| BUSY 2         | MRCs          | FO           | OC, wire OR | 74BCT760 (OC)      | FCT16244        |
| SRQ            | MRCs          | FO           | OC, wire OR | 74BCT760 (OC)      | FCT16244        |
| STR            | FO            | MRCs         | TTL line    | FCT16244           | FCT16244        |

Each MRC transmits five signals to the MFC: BUSY1, BUSY2, ERROR1, ERROR2 and SRQ. These signals notify the MFC about specific events (interrupts from UARTs, BEG\_DATA, END\_DATA, and HOTLink Status) and can trigger the MFC Interrupt Controller. All the signals are driven with 74BCT760 open collector buffers and are wire ORed on the back-plane with the same signals of other MRCs in the crate. All these signals are connected to the A and C lines of the J2 VME backplane (See Appendix A).

C6. Communications Between MRC and Front Ends.

The MRC has two types of connections to the FE. There are 20 communication signals between one section of the MRC and each of two Front-End Sections sent via twist and flat cable (see Table I-3).

Table I-3. Interconnections between FE and MRC (one section, twisted pairs).

| Signal     | Source | Dest. | Type   | Transmitter | Receiver |
|------------|--------|-------|--|-------------|----------|
| INIT       | MRC    | FE    | twisted pair                                 | 75110A      | AD8002   |
| L1 ACC     | MRC    | FE    | twisted pair                                 | 75110A      | AD8002   |
| L2 ACC     | MRC    | FE    | twisted pair                                 | 75110A      | AD8002   |
| L2 REJ     | MRC    | FE    | twisted pair                                 | 75110A      | AD8002   |
| Xing<0..7> | MRC    | FE    | twisted pair                                 | 75110A      | AD8002   |
| DONE       | MRC    | FE    | twisted pair                                 | 75110A      | AD8002   |
| TxDAT      | MRC    | FE    | twisted pair                                 | 75110A      | AD8002   |
| RxDAT      | FE     | MRC   | twisted pair                                 | 75110A      | AD8002   |
| ERROR 1    | FE     | MRC   | twisted pair                                 | 75110A      | AD8002   |
| ERROR2     | FE     | MRC   | twisted pair                                 | 75110A      | AD8002   |
| BUSY 1     | FE     | MRC   | twisted pair                                 | 75110A      | AD8002   |
| BUSY 2     | FE     | MRC   | twisted pair <td>75110A</td> <td>AD8002</td> | 75110A      | AD8002   |
| STRB       | MRC    | FE    | twisted pair                                 | 75110A      | AD8002   |

Fifteen of these signals (INIT, L1ACC, TxDAT, L2ACC, L2REJ, Xing<0..7>, DONE and STRB) are outputs going to FE; five signals (ERROR1, ERROR2, BUSY1, BUSY2 and RxDAT) are inputs from the FE.

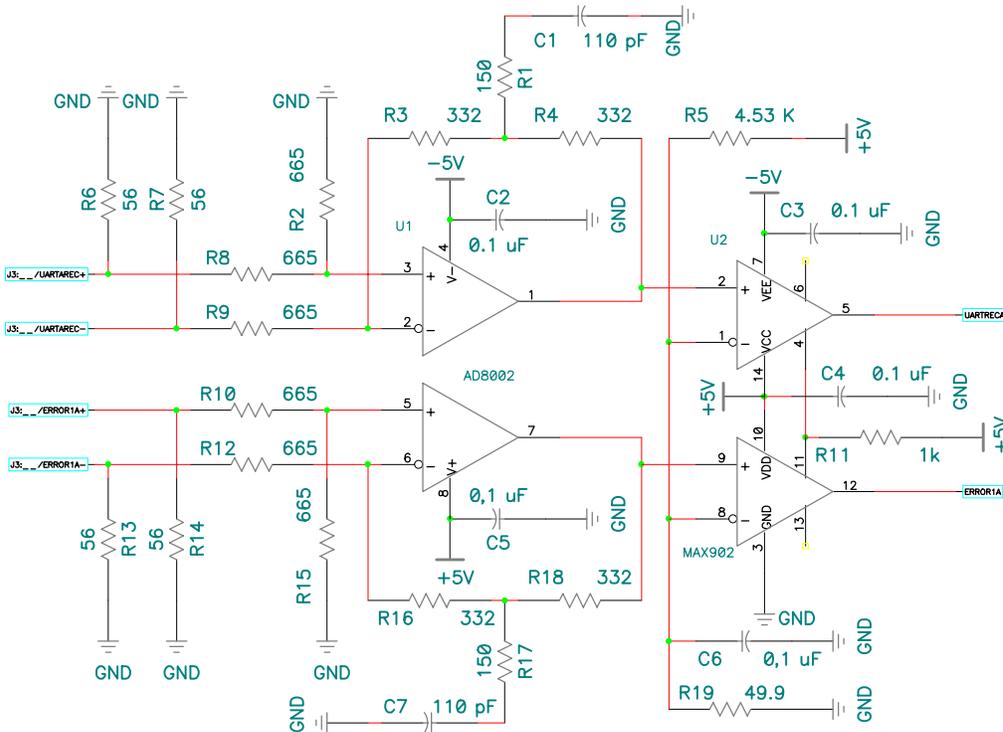


Fig. I-6. Muon twist and flat cable receiver.

The receivers for ERROR1, ERROR2, BUSY1, BUSY2 and RxDAT signals are based on AD8002 current feedback operational amplifiers and MAX902 voltage comparators. A peaking RC feedback network is used to compensate for cable attenuation of the high frequency portion of the signals (

Fig. I-6). All other signals (INIT, L1ACC, TxDAT, L2ACC, L2REJ, STRB and Xing<0..7> are transmitted to the FE using 75110A current drivers.

Table I-4. Interconnections between FE and MCH (coaxial cable).

| Signal         | Source | Dest. | Type    | Transmitter | Receiver |
|----------------|--------|-------|---------|-------------|----------|
| RF (53 MHz)    | MRC    | FE    | coaxial | CLC006      | CLC014   |
| Encoded Timing | MRC    | FE    | coaxial | CLC006      | CLC014   |
| L2 DATA        | FE     | L2    | coaxial | CLC006      | CLC014   |
| L3 DATA        | FE     | MRC   | coaxial | CLC006      | CLC014   |

The second type, high speed connections to the FE are made on existing ASTRO ribbon coaxial cable. The MRC sends and receives signals from and to FE crates. The connector on the MRC has signals for two front-end controllers and must be split into two cables to feed two FEs. Two fast timing signals (RF, Encoded Timing) are transmitted via coaxial ASTRO cables. These signals are transmitted by CLC006 drivers and are transformer coupled to convert differential outputs to single ended signal (Fig. I-7).

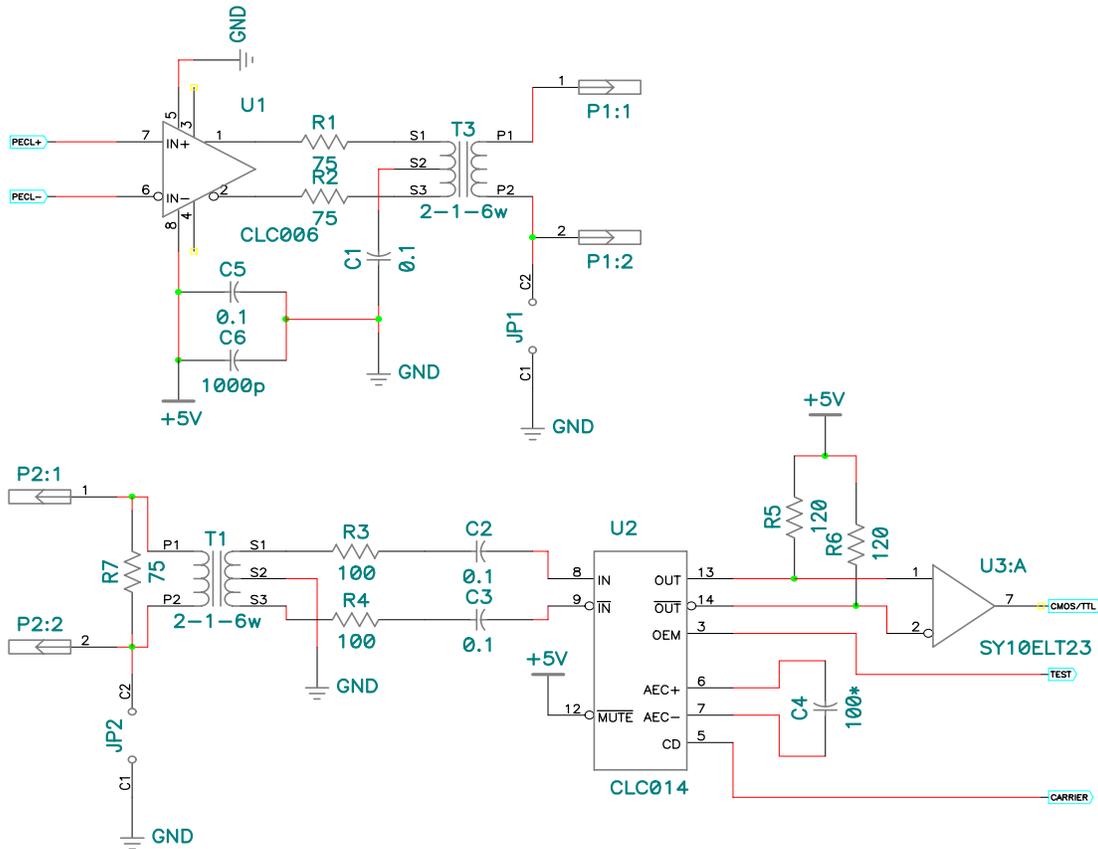


Fig. I-7. Muon serial data driver and receiver.

The L3 DATA is transformer coupled on the MRC to a CLC014 differential cable equalizer/receiver. The CLC014 output drives the HOTLink Receiver. L2 data arrives at the Movable Counting House patch crate on ASTRO ribbon coaxial cable and is split off on a passive board and sent to the Level 2 system. The pin-outs for the connectors are listed in Appendix B.

#### C7. VME Interface.

The MRC has a 32-bit VME Slave Interface consisting of:

- Input buffers for VME address and control signals
- VME address decoding
- VME 32-bit Data Transceivers
- VME command decoder

A memory map of the RAM buffers and I/O ports in the MRC is shown in Table I-19, Appendix C. It is possible to select a Base address by means of DIP switches (address bits A16-A31). 74FCT16244 chips are used as input buffers and 74FCT16500 as Data Transceivers. The VME address and command decoder for both sections of MRC is based on a single CPLD chip.

#### C8. 32-bit Status Register.

There is one 32-bit Control/Status Register (CSR) in each MRC section (Table I-20, Appendix D). It consists of:

- BUSY1, BUSY2 and ERROR1 originating from the FE. ERROR2 is a LOGICAL OR of error sources within the MRC (OVF, RVS and TOUT signals from the HOTLink Receivers)
- mask bits for BUSY1, BUSY2, ERROR1, ERROR2 and ERROR1\_S bit for setting the ERROR1 signal by software
- TOUT, RVS and OVF bits for emulating the corresponding HOTLink error conditions in software
- RESET bit for resetting the ERROR bits (TOUT, RVS and OVF) in the CSR and resetting the HOTLink Control Logic
- REF bit (Reframe Mode of CY7B933)
- DONE bit (sends DONE signal to FE)
- CONN bit indicating (when HIGH) that connection with HOTLink Transmitter in FE board is valid (LOW means that connection has failed)
- SRQ bit for setting/resetting the SRQ signal in software
- SRQ\_R bit for resetting SRQ Trigger
- DSTREAM bit indicating (when HIGH) that a Data Transfer from FE board is in progress
- BIST bit for switching the HOTLink into Built In Self-Test (BIST) mode
- BISOK bit indicating BIST status

- TOUT\_DSTR, TOUT\_BIST, TOUT\_REFR, RVS\_DSTR, RVS\_BIST and OVF\_DSTR bits indicating HOTLink errors
- (TOUT, RVS, OVF) Hot Link Control Logic Errors
- (DSTR), Reframe (RFR) and Built-In Self-Test (BIST)
- INTSCC Interrupt Request from SCC

CSR for each section is based on a separate CPLD chip.

#### C9. Mechanical

The MRC is a single width VME 9U x 280mm module. There are 16 LEDs on the front panel (seven for each channel and two for power) indicating the following conditions:

- Lost connection between FE board and MRC (DISCONN, red);
- Data Transfer from FE board is in progress (DSTREAM, green);
- ERROR1 present (ERROR1, red);
- ERROR2 present (ERROR2, red);
- BUSY1 present (BUSY1, red);
- BUSY2 present (BUSY2, red);
- SRQ present (SRQ, green);
- +5 V and -5.2 V power supply on (yellow).

There is a 16-pin AMP connector for the ribbon coaxial cable on the front panel.

#### C10. Changes from the First Prototype.

There are a number of small changes which are to be made from the first prototype. The main changes are in the clock receiver logic, and the use of alternate CPLDs in place of the discontinued EPX780. These CPLDs are not pin for pin compatible with the EPX780. Since the EPX780 is no longer in production we are forced to make the substitution. The following shows the changes which will need to be made.

In the first prototype the data from the FE came via ASTRO cable and fed into a transformer coupled compensating network on the MRC. This network coupled the MC10H116 receiver with cable. The output of the MC10H116 then fed the CY7B933 HOTLink chip. In the new design the compensating network has been replaced with a COMLINEAR (CLC014) cable receiver chip which requires fewer parts although transformer coupling is still used.

The new design has the SYNC gap, GAP and FC encoded. The high speed signals are still received differentially on the MRC from the back-plane and are then transmitted to the FE via ASTRO cable (See Introduction chapter for details).

#### C11. Downloading, Control and Monitoring.

The operation of the system will require downloading, controlling, and monitoring of data and registers within the D0 muon system. This will be done via the VME based 680xx processors at system start-up, at system failure, or when the system needs new information. The destination for normal data is the VBD. The 680xx VME crate

controller will respond to interrupts from the MRC via the MFC. The software routine will initialize a DMA controller within the VBD thus informing that there is data to be readout.

#### C12. Diagnostic and Test Features.

The D0 muon MRC module will attempt to provide as much testing facility on-board as possible. The functions of the board which require external detection or generation are the input receivers and the custom backplane and connections to the FE.

The test stand software will run diagnostic tests on incoming and suspect or broken cards which have been removed from the D0 muon system. There are two types of diagnostic tests: single module diagnostics and system or multiple module diagnostics. For some test a VME processor, an FE and a MFC will be needed to communicate with the MRC module. Some possible test routines are:

- writing to module registers
- reading from module status registers
- reading module data
- mode setups
- triggers tests
- buffers tests
- data validity tests

There are two type of data validity tests. The slower yet more flexible test uses VME to generate patterns for reading and writing control and data registers. In a faster test the MRC will receive data at full speed through its data input connectors. The Control Board could serve as this test data source.

Some of the test stand diagnostics software will run from a remote terminal and will be implemented with TCL. This will permit the code to be ported to the actual D0 system. The connection to the MRC will be made through the VME crate controller.

The current test stand software has the following features.

- The graphics and human interface part of the code independent of the VME code.
- The VME processor code can execute quickly and can use the VME DEBUG commands.
- The VME code can be downloaded such that each diagnostic routine can be executed independently without having to build a large program. This may mean it will employ the standard debug command set as well as additional custom code.
- The VME code will communicate to the human interface in short cryptic messages. These messages will be designed to interface with the human interface software which will exist on a remote machine. These messages can be interpreted as text but are not designed as

the best visual interface. The current version runs on a PC under NT or Windows 95.

- The code has built in looping for each routine and will report responses at a rate determined by the users request. That is, if you select a mode that reports only on error, the VME code will execute until an error occurs or until the routine completes without error. If the user selects mode report all actions the routine will give detailed reports of all actions as they occur. Other modes will be described later.
- For now the graphic interface is TCL/TK.
- The code on the PC is broken into the TCL/TK interface and C code executables which are called by a mailbox type interface to the TCL/TK.
- The software that interfaces to the VME code from the TCL/TK interface will be transparent to the user and is dependent on the VME processor. For the processor with only an RS232 interface we will use a connection through a terminal server or a direct connection. If the processor has an Ethernet connection (i.e. VME167) we will also connect via rlogin through the terminal server. Each processor has its own startup mode. Each will require an interface to download the programs.
- The programs that run on the VME processor will run to completion and exit for each command. This will aid implementing them in the field.

#### *D. Muon Fanout Card (MFC)*

##### *D1. Introduction.*

The Muon Fanout Card is an interface between the TFW and the muon readout crate. The MFC receives timing, control and trigger information from the TFW via the Serial Communication Link (SCL [10]), and distributes it on J2 user defined lines. The SCL is a D0 standard interface daughter card which converts serial data to parallel. The MFC communicates with the TFW by sending ERROR 1, BUSY 1, ERROR 2, BUSY 2 and INACK. Error signals indicate error conditions associated with Level 1 or Level 2 activities. Busy signals indicate availability of the event buffers.

The TFW provides two types of accelerator gap signals for Geographic Sectors. One gap per beam turn is used by the L1 trigger system to synchronize its input FIFOs receiving data from the different front-end systems. This gap is called sync gap and during this interval, pad characters are sent to the L1 trigger system. The other two gaps can be used, for example, for pulsing the front-ends at a time it is known there will be no beam triggers. Because of the limited number of connections between the platform and the movable counting house, a scheme for encoding three signals onto one line is used for the gaps and First Crossing signal (FC). The Tevatron RF is transferred unaltered on one coax to the readout controller. A phase locked loop is used there to remove jitter, and to restore duty cycle symmetry, a requirement of the TDC chips.

The MFC includes a VME A32D16 slave interface, FIFO memories for the beam crossing and turn numbers, an interrupt controller, a real time clock, three control/status registers, a timing sequencer and counters for TWF decisions. The MFC is controlled by the VME processor in the readout crate. ERROR 1, ERROR 2, BUSY 1, BUSY 2 from each MRC are wire OR'ed on J2. The OR of these backplane signals as well as INIT and L2 Accept can interrupt the VME processor. To localize the interrupt source the processor reads status registers in the MFC and MRCs and calls the appropriate service routine. The block-diagram of the MFC is shown in Fig. I-8.

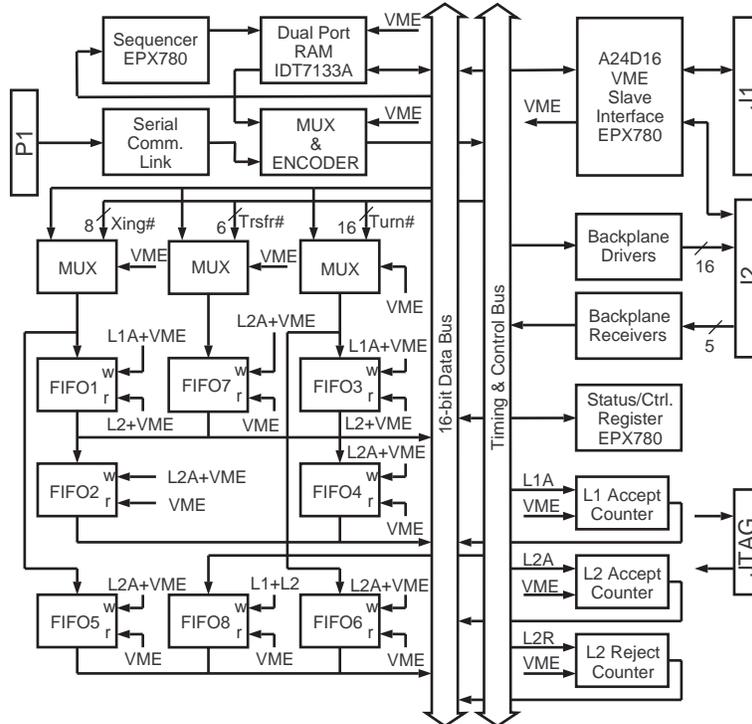


Fig. I-8. Muon Fanout Card. L1A - L1 Accept, L2A - L2 Accept, L2R - L2 Reject, L2 = L2A + L2R, VME - VME command.

Each L1 or L2 TFW decision is uniquely identified by a specific crossing and turn number. All TFW decisions along with their trigger numbers are stored in FIFOs and transmitted to the front ends via the MRCs. All the FIFOs are 256 deep which is much more than the 16 L1 buffers and eight L2 buffers required by the D0 DAQ specification. FIFO1, FIFO2 and FIFO3, FIFO4 are used to mirror the state of the front-end data buffers. Crossing numbers pass through FIFOs one, two and five, and turn numbers pass through FIFOs three, four and six.

For each L1 Accept, an associated 8-bit beam crossing number is stored in FIFO1. At each L2 Accept, a crossing number is moved from FIFO1 to FIFO2. At the same time, the crossing number issued by the TFW is stored in FIFO5. Sixteen bit beam turn numbers move through FIFOs three, four and six in a manner identical to the crossing numbers.

When the VME processor builds the event, it reads one word from FIFO2 and FIFO4 and compares these numbers with those from FIFO5 and FIFO6 which contain the trigger

numbers corresponding to the most recent L2 Accept. In this way, on a trigger by trigger basis, synchronization is checked. FIFO8 is used to store a sequential record of all TFW decisions. The depth of the storage is fixed at 256 triggers. The record is readable by VME for diagnostic purposes. Three 12 bit counters for scaling TFW decisions provide an additional diagnostic.

In addition, the GS is required to append an L3 transfer number furnished by the TFW to event data (FIFO7). These numbers are used by the D0 DAQ system for checking data consistency.

Because of the sequential order of the trigger decisions, checking event synchronization is relatively simple. The crossing and turn numbers associated with a given TFW L1 decision remain attached to an event while it passes through all trigger decision levels. In the muon system, the crossing number is transmitted to the front ends and checking is performed by the front-end readout controllers, but the turn number is generated locally by the readout controllers and is attached to the events by the DSP. This number is verified by the VME processor during event building. If there is a mismatch between two turn numbers an ERROR 2 is generated.

The ability to run locally for the purposes of system installation and checkout has proven to be very important in Run I of D0. The MFC has the ability to emulate the SCL by means of an internal pattern generator based on a 2Kx16 dual port RAM. The sequencer can run in both single cycle and continuous mode. The RAM contents are loaded from the VME bus. Another important diagnostic feature is a real time clock. As required by the D0 DAQ specification, each error condition, initialization procedure and any system specific condition has to be recorded. All related information including trigger numbers and a time stamp are written as a record into a file containing the 16 most recent entries. This information has to be available to the standard D0 on-line tools like CDAQ.

Differential PECL drivers have been successfully tested for distribution of the time critical signals such as RF clock, FC and encoded gap signals. The rest of the signals use standard VME levels and terminations.

The MFC is fitted with a VME interrupter with the five inputs connected to the MRC wire OR lines and a sixth input for the initialization signal from the TFW.

During initialization, the MFC receives BUSY1 signal from each FE to confirm initialization process in the same way as it is specified for INACK signal [11]. Each FE raises its BUSY 1 as soon as INIT signal is set and drops it when initialization is complete. The MFC generates INACK signal as a logical function of INIT and BUSY 1 signals received from FEs.

The essential functions of the Muon Fanout Card as a part of D0 muon readout system are listed below:

- interchanges serial data and parallel status information with a Trigger Framework (TFW) system
- transforms serial data received from TFW to parallel timing and trigger signals and data

- encodes TFW data into 10-bit words according to ANSI X3T11 Fibre Channel specification and ships them via serial interface to Muon Trigger Fanout Card (TFC)
- receives 10-bit encoded serial data from TFC and decodes it to parallel timing and trigger signals and data
- generates timing and trigger signals and data internally to emulate the TFW's timing and trigger signals and data for testing purposes
- stores timing, trigger, status and error information in a FIFO pipeline and non-volatile memory
- interrupts the VME processor module upon receiving the corresponding signals from the MRC, TFW, and internal circuitry
- communicates with the VME processor module via a VME bus interface to supply timing, trigger, status, and error information for use by the on-line software.

## D2. Hardware Description

The MFC consists of the following functional units:

- a) Serial Command Link Receiver Module (SCL Receiver Mezzanine Card)
- b) TFC Interface including:
  - Packet Encoder
  - Packet Decoder
  - Encoder/Decoder
  - Fibre Channel Transmitter
  - Fibre Channel Receiver
- c) TFW Signals Emulator including:
  - Sequencer
  - Dual Port Memory
  - Sequencer Interface
  - 53.1047 MHz Oscillator
  - Frequency Divider
- d) Control and Status Registers
- e) Error Record Circuitry including:
  - Error Record Controller and
  - Timekeeping Non-Volatile Memory
- f) Trigger Signal Multiplexer
- g) Power Reset Circuitry
- h) Front-End Timing Signal Encoder including:
  - Timing Signal Encoder
  - Frequency Multiplier
- i) Timing Signal Drivers and Buffers
- j) FIFO Pipeline including:
  - FIFO Controller together with:
    - ◊ L1ACC Counter

- ◊ L2ACC Counter
- ◊ L2REJ Counter
- ◊ FIFO Status Register
- L1ACC\_TN FIFO Memory
- L2DIR\_TN FIFO Memory
- TFW\_TN FIFO Memory
- L2SIM\_TN FIFO Memory
- L2SIM\_XN FIFO Memory
- L1ACC\_XN FIFO Memory
- L2DIR\_XN FIFO Memory
- TFW\_XN FIFO Memory
- k) Interrupt Controller
- l) Address Decoder
- m) VME Bus Interface including:
  - VME BUS Interface Chip
  - VME BUS Signal Buffers

### D3. Serial Command Link Receiver Module

The Serial Command Link (SCL) Receiver Module is implemented as an SCL Receiver Mezzanine Card and is described in the SCL Specification [10]. The SCL Receiver Mezzanine Card accepts a stream of 16 bit data at 53 MHz on its G-link input connector SCL\_IN and converts it back into the original timing and trigger information as originally transmitted by the TFW.

The following signals and data are transmitted from the TFW to the MFC via the SCL Receiver Mezzanine Card:

- |               |   |   |   |          |
|---------------|---|---|---|----------|
| • L1TN 00..15 | - | L1 Trigger Number                               | - | 16 lines |
| • L1XN 00..07 | - | L1 Crossing Number                              | - | 8 lines  |
| • L1AQ 00..06 | - | L1 Accept Qualifier                             | - | 7 lines  |
| • RF          | - | 53.1047 MHz Clock                               | - | 1 line   |
| • STR         | - | 7.59 MHz Clock                                  |   |          |
| • FX          | - | First Crossing                                  |   |          |
| • BX          | - | Beam Crossing                                   |   |          |
| • SGAP        | - | Synch Gap (no L1 Accepts)                       |   |          |
| • GAP         | - | Gap (L1 Accepts allowed)                        |   |          |
| • L1ACC       | - | L1 Accept                                       |   |          |
| • L1DEC       | - | L1 Decision (Enable signal for L1ACC)           |   |          |
| • L2ACC       | - | L2 Accept                                       |   |          |
| • L2REJ       | - | L2 Reject                                       |   |          |
| • L2DEC       | - | L2 Decision (Enable signal for L2ACC and L2REJ) |   |          |
| • INIT        | - | Initialization                                  |   |          |

The SCL Receiver Mezzanine Card also provides status information to the TFW via its SCL\_STAT output connector. This status information comes from the MRC and is stored in the Control & Status Register of the MFC and can be sent to the TFW by the MFC.

All signals and data coming from the TFW to the MFC, except RF and STR, are updated on the rising edge of STR.

#### D4. TFC Interface

The TFC distributes major timing and trigger signals to all Muon Readout Crates (Geographical Sections [11]). This allows the synchronization of several Muon crates while in local data taking and testing modes (see section E).

The TFC interface consists of a Packet Encoder and Decoder and an 8b/10b Encoder/Decoder which are implemented in three CPLDs (Altera 7128). They are used with a Fiber Channel Transmitter (AMCC S2042) and Receiver (AMCC S2043) to provide a high speed serial interface between the TFC and the MFC.

The Packet Encoder transforms the information coming from the SCL Mezzanine Card into a series of four bytes synchronized by the RF signal. The contents of these words are as follows:

- Byte 1: RF, FX, INIT, GAP, SGAP, L1ACC, L2ACC, L2REJ
- Byte 2: L1XN 00..07
- Byte 3: L1TN 00..07
- Byte 4: L1TN 08..15

L1ACC and L2ACC signals in this case are not the same as L1ACC and L2ACC signals coming directly out of the SCL Mezzanine Card but rather a logical AND combination of these signals with L1DEC and L2DEC correspondingly.

The Packet Decoder accepts a stream of four 8 bit words from the 8b/10b Encoder/Decoder and transforms them into the corresponding TFW signals. The output from the Packet Decoder changes synchronously with the STR signal derived from the incoming RF\_SYS signal, which is derived by the Fiber Channel Receiver from a serial signal sent by the TFC.

#### D5. Internal Sequencer

The timing sequencer is intended for testing the MRCs and MFC itself without connection to the TFW. It is based on combination of RAM (IDT7M1014 Dual Port Memory) and special logic to transform RAM data into timing and trigger patterns which mimics the TFW. The contents of RAM are loaded by the VME processor via the Sequencer Controller realized in an Altera 8000 Series CPLD. The following word bit pattern is implemented in the TFW Signal Emulator:

Table I-5.

|       |      |      |      |      |      |      |      |      |      |
|-------|------|------|------|------|------|------|------|------|------|
| Bit # | 08   | 07   | 06   | 05   | 04   | 03   | 02   | 01   | 00   |
| Data  | TN08 | TN07 | TN06 | TN05 | TN04 | TN03 | TN02 | TN01 | TN00 |
| Bit # | 17   | 16   | 15   | 14   | 13   | 12   | 11   | 10   | 09   |
| Data  | XN01 | XN00 | TN15 | TN14 | TN13 | TN12 | TN11 | TN10 | TN09 |

|       |    |    |      |      |       |       |       |      |      |
|-------|----|----|------|------|-------|-------|-------|------|------|
| Bit # | 26 | 25 | 24   | 23   | 22    | 21    | 20    | 19   | 18   |
| Data  | BX | FX | INIT | XN07 | XN06  | XN05  | XN04  | XN03 | XN02 |
| Bit # | 35 | 34 | 33   | 32   | 31    | 30    | 29    | 28   | 27   |
| Data  |    |    |      |      | L2REJ | L2ACC | L1ACC | SGAP | GAP  |

The logic that transforms contents of the RAM into trigger patterns is realized in an Altera 8000 Series CPLD. The Sequencer uses RF/2 and STR signals produced by the MFC'S internal clock generator of 53.1047 MHz and a frequency divider realized in an Altera 7032 PLD. The memory depth accessed by the sequencer during its cycle is programmable and is defined by the contents of the Number Of Words register (NOW register), which is set in the Computer Access Mode by the processor module.

There are two modes of operations for the Sequencer:

- Single cycle Mode (SM)
- Continuous Mode (CM)

In the SM, the Sequencer executes single sequence of programmed reads from RAM after receiving START signal from the processor module. In CM, it repeats this sequence continuously till being stopped by the processor module which issues STOP command to the Sequencer Mode register residing inside Sequencer Interface. The contents of the Sequencer Mode register is as follows:

Table I-6.

|       |    |    |    |    |    |    |        |      |
|-------|----|----|----|----|----|----|--------|------|
| Bit # | 07 | 06 | 05 | 04 | 03 | 02 | 01     | 00   |
| Data  |    |    |    |    |    |    | Enable | Mode |
| Bit # | 15 | 14 | 13 | 12 | 11 | 10 | 09     | 08   |
| Data  |    |    |    |    |    |    |        |      |

When the sequencer is busy executing sequences of RAM read cycles, it issues a busy signal which can be read by the VME processor from the Sequencer Status register. The contents of this register is shown in the Table I-7:

Table I-7.

|       |    |    |    |    |    |      |        |      |
|-------|----|----|----|----|----|------|--------|------|
| Bit # | 07 | 06 | 05 | 04 | 03 | 02   | 01     | 00   |
| Data  |    |    |    |    |    | Busy | Enable | Mode |
| Bit # | 15 | 14 | 13 | 12 | 11 | 10   | 09     | 08   |
| Data  |    |    |    |    |    |      |        |      |

The Sequencer is implemented in an Altera 8000 Series CPLD.

#### D6. Control and Status Registers

There is one control and one status register in the MFC. The Control register sets the operating mode for the card. There are four modes of operations in MFC:

- external
- system
- internal

- VME access.

In the internal mode of operation, MFC gets its timing and control signals from the internal sequencer. In external mode, the same signals come from the Serial Command Link Receiver Module. The TFC supplies these signals in the system mode. VME access mode is used for programming the contents of Control Register and the dual port memory in the internal sequencer. These modes can be set either by the VME processor or by a MODE switch on the front panel of the card. Modes set by the VME processor override those set by the MODE switch.

It is sometimes desirable for test purposes to imitate the status signals from the MRC, which include L1ERR, L2ERR, L1BUSY, and L2BUSY signals, by settings bits in a register from the VME processor. It is also useful to use an internal signal to emulate both busy signals (L1BUSY, L2BUSY). To do this, the Control Register includes bits for setting and masking status signals and a mask bit for the INIT signal. When a mask bit is set to one, the corresponding signal is set.

The Control Register is a write/read register accessible from VME. Writes to the Control Register have the following bit assignments:

Table I-8.

|       |              |            |             |            |             |        |             |        |
|-------|--------------|------------|-------------|------------|-------------|--------|-------------|--------|
| Bit # | 07           | 06         | 05          | 04         | 03          | 02     | 01          | 00     |
| Data  | INIT_M<br>SK | SYS_S<br>W | EXT_S<br>W  | INT_S<br>W | CAM         | SYS_PR | EXT_P<br>R  | INT_PR |
| Bit # | 15           | 14         | 13          | 12         | 11          | 10     | 09          | 08     |
| Data  | BU2_M<br>SK  | L2BUS<br>Y | BU1_M<br>SK | L1BUS<br>Y | ER2_M<br>SK | L2ERR  | ER1_M<br>SK | L1ERR  |

Control Register reads have the following bit assignments:

Table I-9.

|       |       |       |            |            |       |       |     |      |
|-------|-------|-------|------------|------------|-------|-------|-----|------|
| Bit # | 07    | 06    | 05         | 04         | 03    | 02    | 01  | 00   |
| Data  | L2DEC | L1DEC | L2BUS<br>Y | L1BUS<br>Y | L2ERR | L1ERR | SRQ | INIT |
| Bit # | 15    | 14    | 13         | 12         | 11    | 10    | 09  | 08   |
| Data  |       |       |            |            | CAM   | SYS   | EXT | INT  |

The status information provided by Status Register is the final product of logical operations on status signals coming from the MRCs and from the Control Register.

#### D7. Error Record Circuitry

Each Geographic Section in the D0 Muon System has to maintain a 16 entry deep record of diagnostic information available for later analysis (see DO DAQ Geographic Section Specification [11]). Error Record Circuitry is provided for this purpose. This circuitry makes an entry for each error reported to the TFW as well as for each transition of the INIT signal. These entries contain status information from the latest event, the turn and crossing numbers associated with this event, and a time stamp supplied by a local real time clock.

The Error Record Circuitry uses a Dallas Semiconductor DS1643 8 KB Nonvolatile Timekeeping RAM, which provides the following timing data called Time of Event:

- Year (00 - 99)
- Month (01 - 12)
- Date (01 - 31)
- Day (01 - 07)
- Hour (00 -23)
- Minute (00 - 59)
- Seconds (00 - 59)

The Error Record includes:

- Time of Event (8 bytes)
- L1ACC\_TN\_LAST (2 bytes)
- L1ACC\_XN\_LAST (2 bytes)
- L2ACC\_TN\_LAST (2 bytes)
- L2ACC\_XN\_LAST (2 bytes)
- L2REJ\_TN\_LAST (2 bytes)
- L2REJ\_XN\_LAST (2 bytes)
- Control Register (2 bytes)
- Status Registers (32 bytes)
- L1ACC Counter (2 bytes)
- L2ACC Counter (2 bytes)
- L2REJ Counter (2 bytes)
- Auxiliary Information (194 bytes)

for the total of 256 bytes per record.

Sixteen such records are placed in nonvolatile memory with some additional information. The data has Big Endian byte ordering. Shown below is the memory map of the DS1643:

Table I-10.

| Starting Address        | Size (bytes) | Comment         |
|-------------------------|--------------|-----------------|
| Starting Address + 0000 | 256          | Error record 01 |
| Starting Address + 0100 | 256          | Error record 02 |
| Starting Address + 0200 | 256          | Error record 03 |
| Starting Address + 0300 | 256          | Error record 04 |
| Starting Address + 0400 | 256          | Error record 05 |
| Starting Address + 0500 | 256          | Error record 06 |
| Starting Address + 0600 | 256          | Error record 07 |
| Starting Address + 0700 | 256          | Error record 08 |
| Starting Address + 0800 | 256          | Error record 09 |
| Starting Address + 0900 | 256          | Error record 10 |
| Starting Address + 0A00 | 256          | Error record 11 |
| Starting Address + 0B00 | 256          | Error record 12 |

|                         |      |                              |
|-------------------------|------|------------------------------|
| Starting Address + 0C00 | 256  | Error record 13              |
| Starting Address + 0D00 | 256  | Error record 14              |
| Starting Address + 0E00 | 256  | Error record 15              |
| Starting Address + 0F00 | 256  | Error record 16              |
| Starting Address + 9000 | 2    | Last message address pointer |
| Starting Address + 9002 | 206  | Reserved                     |
| Starting Address + 90D0 | 2    | GS ID                        |
| Starting Address + 90D2 | 2    | GS Status                    |
| Starting Address + 90D4 | 44   | GS Mailbox area              |
| Starting Address + 9100 | 3584 | User defined NVRAM area      |
| Starting Address + 9F00 | 248  | Reserved                     |
| Starting Address + 9FF8 | 8    | DS1643 registers             |

The Timekeeping Memory's starting address is set by the FCM'S Address Decoder.

All Turn Numbers and Crossing Numbers are stored in six 16-bit registers on L1 accepts and L2 accepts or rejects. Storing is disabled when the corresponding L1ERR or L2ERR signals come up from the FE . The registers and logic to control this memory are implemented in Altera 8000 Series CPLD.

#### D8. Trigger Signal Multiplexer

The Trigger Signal Multiplexer accepts timing and trigger signals from three sources (TFW, TFC, and internal sequencer) and chooses one according to the mode of operation. It also provides the logic to form a proper reset (RST) signal and to qualify the L1 Accept and L2 Accept or Reject signals with the L1 and L2 decision signals.

#### D9. Power Reset Circuitry

The Power Reset Circuitry uses a Dallas Semiconductor DS1232 chip to produce a reset pulse when the power supply voltage crosses a 4.5 V threshold. A reset can also be generated by pushing a front panel button.

#### D10. Front-End Timing Signal Encoder

This encoder is described in the introduction chapter of this document. It employs a Startech ST49C101 multiplier to double the reference frequency to 106 MHz for clocking an internal synchronous state machine. The encoder accepts the three timing signals FC, GAP, and SGAP and encodes them into a continuous 106 MHz non-return to zero DC balanced data stream. This logic is implemented in a Altera 7032 CPLD.

#### D11. Trigger Signals Drivers and Buffers

The following signals are sent to the J2 VME backplane connector by the MFC: RF, ENC, STR, INIT, L1ACC, L2ACC, L2REJ, XN 0..7. The following signals are received from the J2 VME backplane connector by the MFC: L1ERR, L2ERR, L1BUSY, L2BUSY, SRQ (See Table I-14, Appendix A).

RF and ENC are differential high frequency signals that are transmitted by Synergy SY10ELT22 PECL drivers (Fig. I-9).

All other signals are TTL and are transmitted and received by Texas Instruments SN75121 dual line drivers or SN75122 triple line receivers.

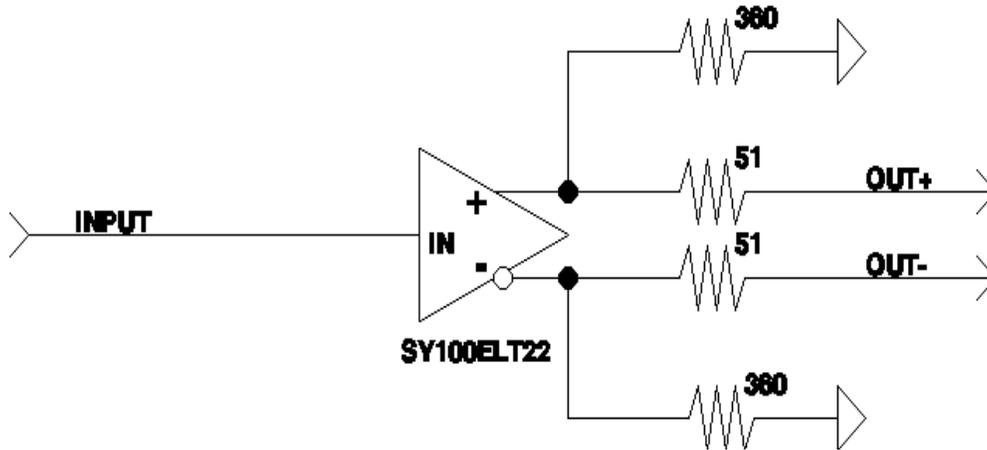


Fig. I-9. Schematic diagram of the differential PECL driver.

#### D12. FIFO Pipelines

FIFO Pipelines using eight Integrated Device Technology IDT72205LB CMOS 256×18 SyncFIFO™ memory chips. All the FIFOs are controlled by the FIFO Controller. In addition to providing logic to perform FIFO control, it also includes registers for storing FIFO status and three L1 and L2 decision counters to check event synchronization. The FIFO Controller is implemented in an Altera 8000 Series CPLD. The memory map of the FIFOs is shown in the Table I-11.

Table I-11.

| Starting Address  | Size (bytes) | Comment  |
|-------------------|--------------|--|
| Base Address + 00 | 2            | L1ACC_XN Write                                   |
| Base Address + 02 | 2            | L2SIM_XN Write                                   |
| Base Address + 04 | 2            | L1ACC_TN Write                                   |
| Base Address + 06 | 2            | L2SIM_TN Write                                   |
| Base Address + 08 | 2            | L1DIR_XN Write                                   |
| Base Address + 0A | 2            | L2DIR_TN Write                                   |
| Base Address + 0C | 2            | TFW_AQ [15..08]<br>&<br>TFW_XN [07..00]<br>Write |
| Base Address + 0E | 2            | TFW_TN Write                                     |
| Base Address + 00 | 2            | L1ACC_XN Read                                    |
| Base Address + 02 | 2            | L2SIM_XN Read                                    |
| Base Address + 04 | 2            | L1ACC_TN Read                                    |
| Base Address + 06 | 2            | L2SIM_TN Read                                    |
| Base Address + 08 | 2            | L1DIR_XN Read                                    |

|                   |   |   |
|-------------------|---|---|
| Base Address + 0A | 2 | L2DIR_TN Read   |
| Base Address + 0C | 2 | TFW_AQ [15..08]<br>&<br>TFW_XN [07..00]<br>Read                     |
| Base Address + 0E | 2 | TFW_TN Read   |
|                   |   |   |
| Base Address + 10 | 2 | L1ACC Counter<br>Write  |
| Base Address + 12 | 2 | L2ACC Counter<br>Write  |
| Base Address + 14 | 2 | L2REJ Counter<br>Write  |
|                   |   |   |
| Base Address + 20 | 2 | L1ACC Counter<br>Read   |
| Base Address + 22 | 2 | L2ACC Counter<br>Read   |
| Base Address + 24 | 2 | L1REJ Counter<br>Read   |
|                   |   |   |
| Base Address + 26 | 2 | FIFO Status Register<br>[15..08 – Empty]<br>[07..00 – Full]<br>Read |
|                   |   |   |
| Base Address + 28 | 2 | Spare Read or Write   |

### D13. Interrupt Controller

The Interrupt Controller uses two Advanced Micro Devices AM9519A Universal Interrupt Controller capable of handling up to a total of 16 prioritized maskable interrupt requests with four programmable responses for each interrupt. The Interrupt Controller processes the following MFC interrupt requests in order of descending priority:

- |                           |   |        |                  |
|---------------------------|---|--------|------------------|
| 1. DMA_DONE               | * | IRQ_00 | highest priority |
| 2. SRQ                    | * | IRQ_01 |                  |
| 3. L1ERR                  | * | IRQ_02 |                  |
| 4. L2ERR                  | * | IRQ_03 |                  |
| 5. INIT (rising edge)     | * | IRQ_04 |                  |
| 6. L1BUSY                 | * | IRQ_05 |                  |
| 7. L2BUSY                 | * | IRQ_06 |                  |
| 8. L1DEC                  | * | IRQ_07 |                  |
| 9. L2DEC                  | * | IRQ_08 |                  |
| 10. L1ACC                 | * | IRQ_09 |                  |
| 11. L2ACC                 | * | IRQ_10 |                  |
| 12. L2REJ                 | * | IRQ_11 |                  |
| 13. FOVFL - FIFO overflow | * | IRQ_12 |                  |
| 14. FEMPTY - FIFO empty   | * | IRQ_13 | lowest priority  |

#### D14. Address Decoder and Card ID

There are eight segments in the 32-bit VME address space that are associated with the MFC internal memory and I/O devices. Their starting addresses are given in the following table:

Table I-12.

| Starting Address             | Size (bytes) | Comment                    |
|------------------------------|--------------|----------------------------|
| Card Base Address + 00000000 | 1K           | FIFO Controller            |
| Card Base Address + 00000200 | 1K           | Control & Status Registers |
| Card Base Address + 00000400 | 1K           | Sequencer Interface        |
| Card Base Address + 00000600 | 1K           | Card ID Switches           |
| Card Base Address + 00000800 | 1K           | Interrupt Controller 1     |
| Card Base Address + 00000A00 | 1K           | Interrupt Controller 2     |
| Card Base Address + 00000C00 | 1K           | Error Record Controller    |
| Card Base Address + 00000E00 | 1K           | Spare                      |
| Card Base Address + 00001000 | 56K          | Timekeeping Memory         |
| Card Base Address + 0010000  | 64K          | Dual Port Memory           |

The Card Base Address is defined by VME Bus Interface. The MFC provides a card identification number (ID) and a card serial number (SN) for reading by the VME processor. Both these numbers are set by switches connected to the card information logic (SN) and to the VME Bus Interface Circuitry (ID). The Address decoder together with the card ID logic is implemented in an Altera 7064 CPLD.

#### D15. VME Bus Interface

VME Bus Interface uses an Interface Technology IT9010 Interface chip which performs 32-bit address decoding. Assigning the card base address is done by setting the contents of specific fields in three registers inside the IT9010: the address space field in the ID register, the required memory field in the device type register, and the contents of offset register.

The VME bus signal buffers include address and data buffers, interrupt buffers, and control buffers. All these buffers are either Texas Instruments SN75121 dual line drivers or SN75122 triple line receivers. They process TTL signals on J1 connector of the VME backplane.

#### D16. Mechanical

The MFC is a single width VME 9U x 280mm card. The front panel is shown in Fig. I-10. The front panel includes:

- 13 LEDs indicating the following conditions:
  - 1) TFW (green) - timing and control signals and data from TFW are normally transferred by SCL Receiver
  - 2) VME (green) - VME access in progress
  - 3) SEQ (green) - timing and control signals generated by the internal sequencer
  - 4) CAM (green) - computer access mode has been set by VME
  - 5) ERROR1 (red) - there is an L1ERROR signal coming from the MRCs
  - 6) ERROR2 (red) - there is an L2ERROR signal coming from the MRCs
  - 7) +5 (yellow) - +5V power is on
  - 8) -5 (yellow) - -5V power is on
  - 9) INT MODE - internal mode
  - 10) EXT MODE - external mode
  - 11) SYS MODE - system mode
  - 12) unknown1 - SCL'S indicator
  - 13) unknown2 - SCL'S indicator

*Comment: when both ERROR1 and ERROR2 LEDs are flashing, this means that an internal failure has occurred.*

- SCL\_IN - high frequency G-link input connector to connect MFC to TFW.
- Two LEMO connectors TFC\_IN and TFC\_OUT to connect the MFC to the TFC
- A LEMO connector to provide output of RF frequency for monitoring
- MODE switch to manually set MFC's mode of operation;
- RST push button to manually reset the module.

#### D17. Software issues

The MFC requires initialization from VME. This will be part of the on-line software routines, which will initialize all the modules in the muon readout crate.

This routine has to check the internal dual port and timekeeping memories, all FIFOs and I/O registers. It has to set up the VME bus interface chip and both interrupt controller chips, clear the error entries inside the Error Record Controller and the L1 and L2 decision counters inside the FIFO Controller, and set up the Control Register for the desired mode of operation.

In stand alone mode, the software initializes the module after a power up as before, with the additional tasks specific to testing the module. This includes loading the patterns for the internal sequencer, etc.

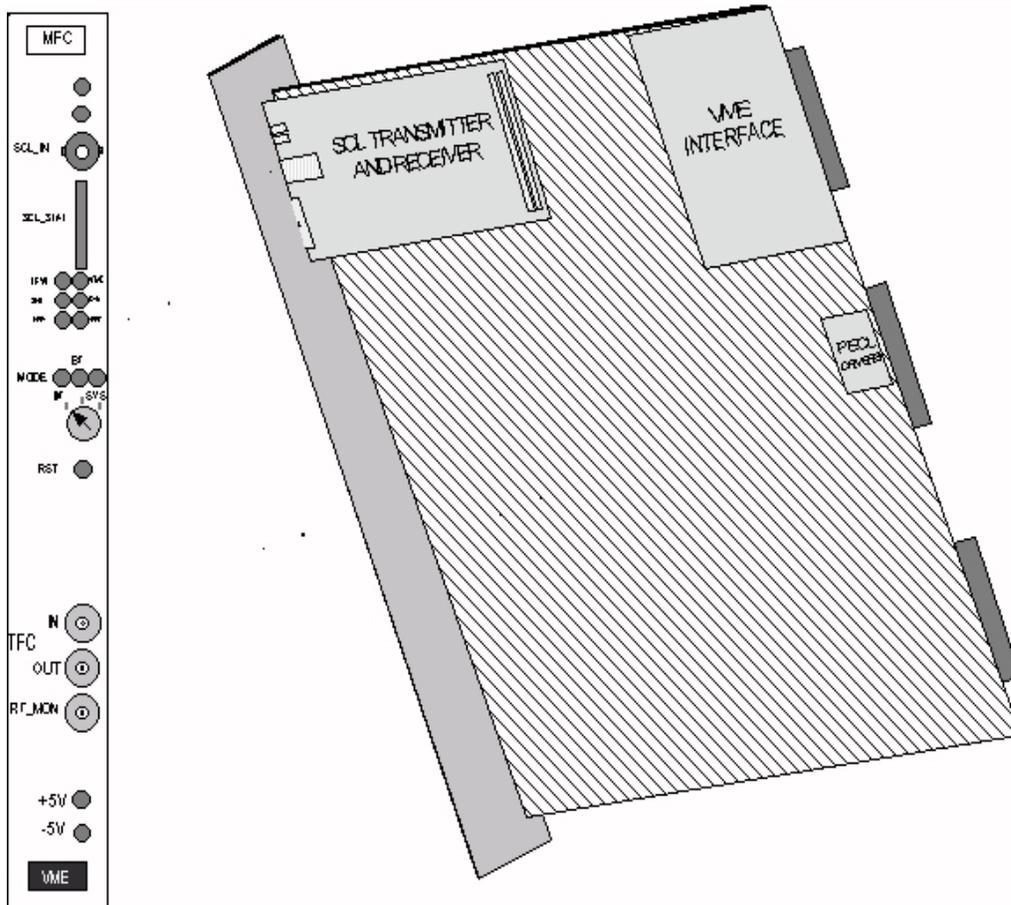


Fig. I-10. MFC front panel.

### E. Muon Trigger Fanout Card (TFC)

#### (a) Introduction

The synchronization of several muon crates in local data taking and testing modes was always an issue during Run I at D0. There are many advantages to be had should such a feature be implemented:

- the ability to readout and combine information from different detectors in “VAX local” mode, thus allowing small scale physics analysis of the data
- the ability to run locally all or any part of the muon system with beam, cosmic triggers or pulsers without involving the TFW and D0 DAQ
- the ability to mimic almost all of the TFW functions without having the TFW running which allows for the debugging of the muon

system independently using simple tools like a scope or a logic analyzer

In order to implement this synchronization, one needs to understand what “VAX local” means. In Run I there were several programs developed to allow the user to run a VAX based program which collected data from one muon crate (or module), transfer it via the Vertical Interconnect (VI) to the VAX and process it. Such programs allowed independent tests to be done in parallel with different crates and were found to be very useful tools. The attempts to do this with several crates simultaneously within one program were not very successful due to the asynchronous nature of the VI interface.

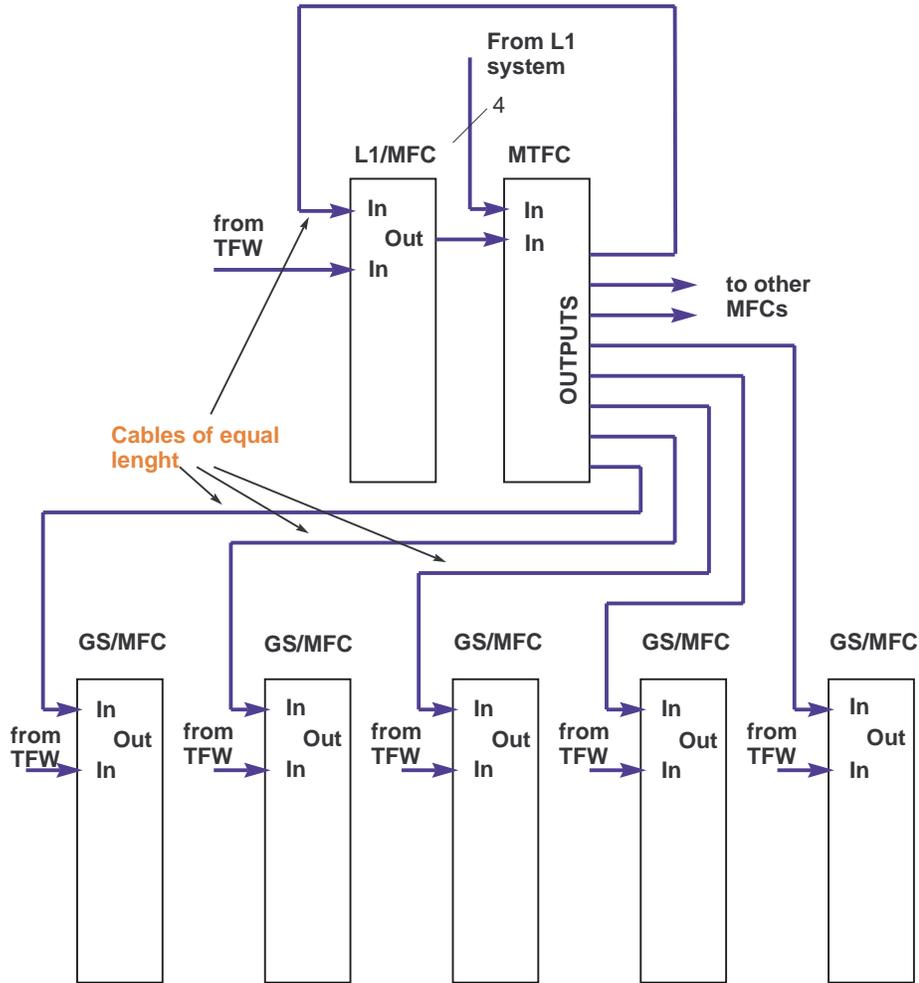
(b) Trigger Fanout Card Conceptual Design

This problem is addressed in the Run II configuration. One can imagine having a VME module (Trigger Fanout Card) that distributes the major timing signals and at least L1 decisions to all muon readout crates (GSs). The data readout can be performed in the usual manner via the VIs, but trigger control will be similar to the standard TFW control with a few minor differences. The Trigger Fanout Card (TFC) has to have the following features:

- four maskable inputs for trigger signals received from the L1 system or external source (NIM)
- one high speed serial input for timing and control signals received from an external source (MFC)
- sixteen serial outputs to provide timing and control signals for the MFCs
- an internal 53.1047 MHz quartz oscillator
- an internal “busy” latch set by a trigger and reset by a VME command
- an internal programmable crossing counter (8 bit)
- an internal programmable turn counter
- an internal FIFO memory for delayed L2 decisions
- a VME slave interface

The serial links for this implementation can be the Cypress HOTLink used by the FEs operating at 302.9 Mbit/s. This transmits four bytes every 132 ns. The clock frequency for the HOTLink chips has to be  $4/7 \cdot 53.1047$  MHz. The set of signals for serial transfers can be arranged in a manner similar to the SCL:

- INIT
- 53.1047 MHz (recovered clock phase locked to the HOTLink RCLK pin)
- First Crossing
- GAP
- SYNC GAP
- L1 Accept



*Additional Muon Fanout Card features:*

- one serial input for the MFC synchronization
- one output with serial data encoded timing signals

*Muon Trigger Fanout features:*

- one serial input for the MFC synchronization
- four maskable inputs from L1 system (NIM)
- 16 outputs with serial data encoded timing signals
- internal 53.1047 MHz quartz oscillator
- internal "READY" latch controlled by VME
- internal programmable crossing counter (8 bit)
- VME slave interface

Fig. I-11. Block-Diagram of the Muon Trigger Fanout Card.

- L2 Accept (delayed copy of L1 Accept)
- Crossing Number (8 bit)

- Turn Number (16 bit)

The additional feature necessary to implement to the MFCs are as follows:

- a serial transmitter re-transmitting the SCL signals with the output at the front panel connector
- a serial receiver to accommodate timing and control signals distributed by the TFC

It should be noted that the cable connection between TFC and MFCs is quite short (no longer than 20'). It is easy to provide equal cable lengths for all the MFC connections and eliminate unwanted re-adjustment of the timing delays within the front ends. Though due to the additional propagation delay for the timing signals coming from the TFW it may be necessary to make common change within all the front ends when collecting data from the beam in the local mode.

Appendix A.

D0 MUON VME BACKPLANE

Table I-13. D0 Muon Backplane J1 Connector.

| Pin | A        | B        | C         |
|-----|----------|----------|-----------|
| 1   | D00      | BBSY/    | D08       |
| 2   | D01      | BCLR/    | D09       |
| 3   | D02      | ACFAIL/  | D10       |
| 4   | D03      | BG0IN/   | D11       |
| 5   | D04      | BG0OUT/  | D12       |
| 6   | D05      | BG1IN/   | D13       |
| 7   | D06      | BG1OUT/  | D14       |
| 8   | D07      | BG2IN/   | D15       |
| 9   | GND      | BG2OUT/  | GND       |
| 10  | SYSCLK   | BG3IN/   | SYSFAIL/  |
| 11  | GND      | BG3OUT/  | BERR/     |
| 12  | DS1/     | BR0/     | SYSRESET/ |
| 13  | DS0/     | BR1/     | LWORD/    |
| 14  | WRITE/   | BR2/     | AM5       |
| 15  | GND      | BR3/     | A23       |
| 16  | DTACK/   | AM0      | A22       |
| 17  | GND      | AM1      | A21       |
| 18  | AS/      | AM2      | A20       |
| 19  | GND      | AM3      | A19       |
| 20  | IACK/    | GND      | A18       |
| 21  | IACKIN/  | SERCLK   | A17       |
| 22  | IACKOUT/ | SERDAT   | A16       |
| 23  | AM4      | GND      | A15       |
| 24  | A07      | IRQ7/    | A14       |
| 25  | A06      | IRQ6/    | A13       |
| 26  | A05      | IRQ5/    | A12       |
| 27  | A04      | IRQ4/    | A11       |
| 28  | A03      | IRQ3/    | A10       |
| 29  | A02      | IRQ2/    | A09       |
| 30  | A01      | IRQ1/    | A08       |
| 31  | -12V     | +5VSTDBY | +12V      |
| 32  | +5V      | +5V      | +5V       |

Table I-14. D0 Muon Backplane J2 Connector.

| Pin | A               | B        | C               |
|-----|-----------------|----------|-----------------|
| 1   | GND             | +5V      | GND             |
| 2   | <b>STRB</b>     | GND      | <b>RF+</b>      |
| 3   | GND             | RESERVED | <b>RF-</b>      |
| 4   | <b>INIT</b>     | A24      | GND             |
| 5   | GND             | A25      | <b>ENC+</b>     |
| 6   | <b>L1ACC</b>    | A26      | <b>ENC-</b>     |
| 7   | GND             | A27      | GND             |
| 8   | <b>L2ACC</b>    | A28      | <b>XN00</b>     |
| 9   | GND             | A29      | GND             |
| 10  | <b>L2REJ</b>    | A30      | <b>XN01</b>     |
| 11  | GND             | A31      | GND             |
| 12  | <b>RESERVED</b> | GND      | <b>XN02</b>     |
| 13  | GND             | +5V      | GND             |
| 14  | <b>RESERVED</b> | D16      | <b>XN03</b>     |
| 15  | GND             | D17      | GND             |
| 16  | <b>SRQ</b>      | D18      | <b>XN04</b>     |
| 17  | GND             | D19      | GND             |
| 18  | <b>BUSY1</b>    | D20      | <b>XN05</b>     |
| 19  | GND             | D21      | GND             |
| 20  | <b>BUSY2</b>    | D22      | <b>XN06</b>     |
| 21  | GND             | D23      | GND             |
| 22  | <b>ERR1</b>     | GND      | <b>XN07</b>     |
| 23  | GND             | D24      | GND             |
| 24  | <b>ERR2</b>     | D25      | <b>RESERVED</b> |
| 25  | GND             | D26      | GND             |
| 26  |                 | D27      |                 |
| 27  |                 | D28      |                 |
| 28  |                 | D29      |                 |
| 29  |                 | D30      |                 |
| 30  |                 | D31      |                 |
| 31  |                 | GND      |                 |
| 32  |                 | +5V      |                 |

Note: The MFC uses the J1 connector and B row of the J2 connector on a VME backplane to communicate with the VME processor. The pin assignments for rows A and C on the J2 connector are specific to D0 Muon and are defined in the table above.

Table I-15. D0 Muon Backplane J3 Connector.

| <b>Pin</b> | <b>A</b>        | <b>B</b>        | <b>C</b>        |
|------------|-----------------|-----------------|-----------------|
| 1          | GND             | GND             | GND             |
| 2          | XN00B- (J8:2)   | XN00B+ (J8:1)   | XN01B- (J8:4)   |
| 3          | XN01B+ (J8:3)   | XN02B- (J8:6)   | XN02B+ (J8:5)   |
| 4          | XN03B- (J8:8)   | XN03B+ (J8:7)   | XN04B- (J8:10)  |
| 5          | XN04B+ (J8:9)   | XN05B- (J8:12)  | XN05B+ (J8:11)  |
| 6          | XN06B- (J8:14)  | XN06B+ (J8:13)  | XN07B- (J8:16)  |
| 7          | XN07B+ (J8:15)  | INITB- (J8:18)  | INITB+ (J8:17)  |
| 8          | L1ACCB- (J8:20) | L1ACCB+ (J8:19) | ERR2B- (J8:22)  |
| 9          | ERR2B+ (J8:21)  | L2ACCB- (J8:24) | L2ACCB+ (J8:23) |
| 10         | L2REJB- (J8:26) | L2REJB+ (J8:25) | TxDATB- (J8:28) |
| 11         | TxDATB+ (J8:27) | DONEB- (J8:30)  | DONEB+ (J8:29)  |
| 12         | STRBB- (J8:32)  | STRBB+ (J8:31)  | RxDATB- (J8:34) |
| 13         | RxDATB+ (J8:33) | ERR1B- (J8:36)  | ERR1B+ (J8:35)  |
| 14         | BUSY1B- (J8:38) | BUSY1B+ (J8:37) | BUSY2B- (J8:40) |
| 15         | BUSY2B+ (J8:39) | XN00A- (J7:2)   | XN00A+ (J7:1)   |
| 16         | XN01A- (J7:4)   | XN01A+ (J7:3)   | XN02A- (J7:6)   |
| 17         | XN02A+ (J7:5)   | XN03A- (J7:8)   | XN03A+ (J7:7)   |
| 18         | XN04A- (J7:10)  | XN04A+ (J7:9)   | XN05A- (J7:12)  |
| 19         | XN05A+ (J7:11)  | XN06A- (J7:14)  | XN06A+ (J7:13)  |
| 20         | XN07A- (J7:16)  | XN07A+ (J7:15)  | INITA- (J7:18)  |
| 21         | INITA+ (J7:17)  | L1ACCA- (J7:20) | L1ACCA+ (J7:19) |
| 22         | ERR2A- (J7:22)  | ERR2A+ (J7:21)  | L2ACCA- (J7:24) |
| 23         | L2ACCA+ (J7:23) | L2REJA- (J7:26) | L2REJA+ (J7:25) |
| 24         | TxDATA- (J7:28) | TxDATA+ (J7:27) | DONEA- (J7:30)  |
| 25         | DONEA+ (J7:29)  | STRB- (J7:32)   | STRB+ (J7:31)   |
| 26         | RxDATA- (J7:34) | RxDATA+ (J7:33) | ERR1A- (J7:36)  |
| 27         | ERR1A+ (J7:35)  | BUSY1A- (J7:38) | BUSY1A+ (J7:37) |
| 28         | BUSY2A- (J7:40) | BUSY2A+ (J7:39) | GND             |
| 29         | GND             | GND             | GND             |
| 30         | GND             | GND             | GND             |
| 31         | GND             | GND             | GND             |
| 32         | - 5V            | -5 V            | -5 V            |

Table I-16. D0 Muon Backplane J7/J8 Connectors.

| <b>Pin</b> | <b>Signal</b> | <b>Pin</b> | <b>Signal</b> |
|------------|---------------|------------|---------------|
| 1          | Xing0+        | 2          | Xing0-        |
| 3          | Xing1+        | 4          | Xing1-        |
| 5          | Xing2+        | 6          | Xing2-        |
| 7          | Xing3+        | 8          | Xing3-        |
| 9          | Xing4+        | 10         | Xing4-        |
| 11         | Xing5+        | 12         | Xing5-        |
| 13         | Xing6+        | 14         | Xing6-        |
| 15         | Xing7+        | 16         | Xing7-        |
| 17         | INIT+         | 18         | INIT-         |
| 19         | L1ACC+        | 20         | L1ACC-        |
| 21         | ERR2+         | 22         | ERR2-         |
| 23         | L2ACC+        | 24         | L2ACC-        |
| 25         | L2REJ+        | 26         | L2REJ-        |
| 27         | TxDAT+        | 28         | TxDAT-        |
| 29         | DONE+         | 30         | DONE-         |
| 31         | STRB+         | 32         | STRB-         |
| 33         | RxDAT+        | 34         | RxDAT-        |
| 35         | ERR1+         | 36         | ERR1-         |
| 37         | BUSY1+        | 38         | BUSY1-        |
| 39         | BUSY2+        | 40         | BUSY2-        |
| 41         | GND           | 42         | GND           |
| 43         | GND           | 44         | GND           |
| 45         | GND           | 46         | GND           |
| 47         | GND           | 48         | GND           |
| 49         | GND           | 50         | GND           |

Notes:

1. J7 is connected to Section A of the MRC. J8 is connected to Section B of the MRC.
2. Ten pins (41-50) of J8 are connected to GND at the backplane. Ten pins (41-50) of J7 are connected to GND within the VME module.
3. TxDAT denotes the MRC's UART transmitter output. RxDAT denotes the MRC's UART receiver input.

Appendix B.

MRC AND FE COAXIAL CABLE CONNECTORS

Table I-17. AMP 103167-5 16 PIN header connector mounted on MRC PCB

| Pin | Signal            |
|-----|-------------------|
| 1   | L3 DATAA+         |
| 2   | L3 DATAA-         |
| 3   | RFA+              |
| 4   | RFA-              |
| 5   | Encoded Timing A+ |
| 6   | Encoded Timing A- |
| 7   | NC                |
| 8   | NC                |
| 9   | L3 DATAB+         |
| 10  | L3 DATAB-         |
| 11  | RFB+              |
| 12  | RFB-              |
| 13  | Encoded Timing B+ |
| 14  | Encoded Timing B- |
| 15  | NC                |
| 16  | NC                |

Note: (+) indicates signal wire, (-) indicates cable shield.

Table I-18. AMP 103167-1 eight pin header connector mounted on FE PCB

| Pin | Signal          |
|-----|-----------------|
| 1   | L3 DATA+        |
| 2   | L3 DATA-        |
| 3   | RF+             |
| 4   | RF-             |
| 5   | Encoded Timing+ |
| 6   | Encoded Timing- |
| 7   | L2 TRIG+        |
| 8   | L2 TRIG-        |

Note: (+) indicates signal wire, (-) indicates cable shield.

Appendix C.

**MUON READOUT CARD MEMORY MAP**

Table I-19. MRC addresses

| Address         | Starting Address Offset | Length (bytes) | Status Read/Write | Assigned  |
|-----------------|-------------------------|----------------|-------------------|---|
| 220000...221FFF | 0                       | 8K             | R/W               | Dual-Port RAM Section A                               |
| 224000          | 16K                     | 1              | W                 | Reset SCC AM85C30                                     |
| 214010          | 16K + 16                | 4              | R/W               | CSR Section A   |
| 228000...229FFF | 32K                     | 8K             | R/W               | Dual-Port RAM Section B                               |
| 22C000          | 48K+3                   | 2              | R/W               | SCC Channel B; access to all internal registers       |
| 22C004          | 48K+7                   | 2              | R/W               | SCC Channel A; access to all internal registers       |
| 22C008          | 48K+11                  | 2              | R/W               | SCC Channel B; direct access to TDR and RDR registers |
| 22C00C          | 48K+15                  | 2              | R/W               | SCC Channel A; direct access to TDR and RDR registers |
| 22C010          | 48K + 16                | 4              | R/W               | CSR Section B   |

Note: All addresses start from Base Address ( N \* 64K, N=0...255). In the table above the base address is assumed to be 220000.

CSR data format (16 bit LOW)

|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| vme | D15 | D14 | D13 | D12 | D11 | D10 | D09 | D08 | D07 | D06 | D05 | D04 | D03 | D02 | D01 | D00 |
| csr | D07 | D06 | D05 | D04 | D03 | D02 | D01 | D00 | D15 | D14 | D13 | D12 | D11 | D10 | D09 | D08 |

CSR data format (16 bit HIGH)

|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| vme | D15 | D14 | D13 | D12 | D11 | D10 | D09 | D08 | D07 | D06 | D05 | D04 | D03 | D02 | D01 | D00 |
| csr | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D00 | D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 |

Zilog Z16C30 Serial Communication Controller Data format

|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| vme | D15 | D14 | D13 | D12 | D11 | D10 | D09 | D08 | D07 | D06 | D05 | D04 | D03 | D02 | D01 | D00 |
| scc | D07 | D06 | D05 | D04 | D03 | D02 | D01 | D00 | D15 | D14 | D13 | D12 | D11 | D10 | D09 | D08 |

Appendix D.

MUON READOUT CARD STATUS REGISTER

Table I-20.

| Bit # | Read/Write | WRITE    |   | READ      |  |
|-------|------------|----------|---|-----------|--|
|       |            | NAME     | REMARKS   | NAME      | REMARKS                                |
| 0     | R          | -        | -   | BUSY1     | FE signal                              |
| 1     | R          | -        | -   | BUSY2     | FE signal                              |
| 2     | R          | -        | -   | ERROR1    | FE signal + Set Register               |
| 3     | R          | -        | -   | ERROR2    | Error2 Sources OR * Mask Register      |
| 4     | R/W        | BUSY1_M  | Busy1 Mask Register                                 | BUSY1_M   | Busy1 Mask Register                    |
| 5     | R/W        | BUSY2_M  | Busy2 Mask Register                                 | BUSY2_M   | Busy2 Mask Register                    |
| 6     | R/W        | ERROR1_M | Error1 Mask Register                                | ERROR1_M  | Error1 Mask Register                   |
| 7     | R/W        | ERROR1_S | Error1 Set Register                                 | ERROR1_S  | Error1 Set Register                    |
| 8     | R/W        | TOUT_S   | Setting of Time-out Error                           | TOUT      | Time-Out Error Status                  |
| 9     | R/W        | RVS_S    | Setting of RVS Error                                | RVS       | RVS Error Status                       |
| 10    | R/W        | OVF_S    | Setting of Overflow Error                           | OVF       | OVF Error Status                       |
| 11    | W          | RESET    | Reset TOUT, RVS, OVF Bits and CY7B933 Control Logic | -         | -                                      |
| 12    | R/W        | ERROR2_M | Error2 Mask Register                                | ERROR2_M  | Error2 Mask Register                   |
| 13    | R          | -        | -   | CONN      | MRC-FE Connection                      |
| 14    | R/W        | SRQ_R    | Reset SRQ Trigger                                   | DSTREAM   | CY7B933 Data Transfer Status           |
| 15    | R/W        | DONE     | Send DONE signal to FE                              | SRQ_DSTR  | "1" when DSTREAM ended                 |
| 16    | R/W        | REF      | Reframe the CY7B933                                 | REFD      | CY7B933 has reframed                   |
| 17    | R/W        | SRQ_M    | Service Request Mask                                | SRQ_M     | Service Request Mask                   |
| 18    | R/W        | SRQ      | SRQ to Fan-out                                      | SRQ       | SRQ Status                             |
| 19    | R/W        | BIST     | Set BIST Mode                                       | BISOK     | BIST Status from CY7B933 Control Logic |
| 20    | R          | -        | -   | TOUT_DSTR | Data Transfer time-out                 |
| 21    | R          | -        | -   | TOUT_BIST | Self-Test time-out                     |
| 22    | R          | -        | -   | TOUT_REFR | Reframe time-out                       |
| 23    | R          | -        | -   | RVS_DSTR  | RVS during Data Transfer               |
| 24    | R          | -        | -   | RVS_BIST  | RVS during Self-Test                   |
| 25    | R          | -        | -   | OVF_DSTR  | OVF during Data Transfer               |
| 26    | R          | -        | -   | INTSCC    | Interrupt from SCC                     |
| 27    |            | -        | -   | -         | -                                      |
| 28    |            | -        | -   | -         | -                                      |
| 29    |            | -        | -   | -         | -                                      |
| 30    |            | -        | -   | -         | -                                      |
| 31    |            | -        | -   | -         | -                                      |