

# Specification for muon readout crate software

## Introduction

The main task of this specification is to give guidelines for the design of working program serving muon readout crates. The specification is based on D0 documents and other sources describing

- DAQ Geographic Section GS (synonym of a muon readout crate)
- D0 Run II online computing system
- Muon L2 & L3 data formats,
- MFC, MRC, VBD,
- MVME162LX,
- VxWorks real-time OS
- EPICS
- Cross software development system for Motorola 68k CPUs

## Muon readout crates in the D0 DAQ hardware

D0 detector data streams pass on hardware objects from up to down. These objects (systems & subsystems) are shown as follows. It is assumed that the reader is familiar with the abbreviations used.

| Object                      | Location          | Subsystems            |                       |                       |                      |
|-----------------------------|-------------------|-----------------------|-----------------------|-----------------------|----------------------|
| Muon Detectors & L1 Trigger | D0 Collision hall | PDT                   | MDT                   | SC                    | L1 Trigger           |
| Muon Detector electronics   | D0 Collision hall | FEB                   | ADB, MDC              | SFE                   | MTC                  |
| Muon Front-end Control Unit | D0 Collision hall | CB                    | MDRC, M68k CPU        | SRC, M68k CPU         | MTCM                 |
| Muon Readout VME crates     | MCH               | MFC,MRC,VBD, M68k CPU | MFC,MRC,VBD, M68k CPU | MFC,MRC,VBD, M68k CPU | MFC,MRC,VBD M68k CPU |

  

|                       |                     |   |
|-----------------------|---------------------|---|
| L3 Readout            | MCH                 | VRC(Vertical Readout Controller), SB(Segment Bridge), MPM(Multi Port Memory)  |
| L3 Filter Nodes       | DAB2                | PC Farm   |
| D0 Central UNIX Hosts | DAB2                | 1 Gb/s & 100 Mb/s Ethernet Switch, AlphaServer 4000 UNIX Hosts, D0 detector control & monitoring, Event monitoring, Control room activities |
| FCC                   | Feynman CD Building | Logging to tape, off-line processing.   |

Muon subsystem passes data stream separately from its detector to front-end electronics and to Front-end VME Control Unit for pipelining and other processing necessary for L2 and L3 Levels. In case of PDT subsystem the CB (Control Board) performs functions of a Front-end VME crate. Muon readout crates receive L3 data from front-end Control units, check for errors and transmit L3 data to the next level of selection and processing. Data to L3 filter nodes are sent via VBD (VME Buffer Driver).

## Hardware components of the muon readout crate and data links

Each muon readout crate consists of the following modules:

| Module type                        | Parameters  | Number of modules |
|------------------------------------|---|-------------------|
| MVME162LX-222a Embedded Controller | CPU MC68040, 32-bit, 25 MHz, 4MB RAM, 128KB SRAM with battery backup, 1 Mb Flash memory with MVME162BUG installed, 8K by 8 NVRAM/TOD clock, Ethernet AUI port with additional transceiver JD50 to 10BaseT (twisted pairs), four serial ports, VMEbus interface A32/D32, VMEbus interrupter and VMEbus interrupt handler   | 1                 |
| VME Buffer Driver (VBD)            | 30 Mb/s VME transfer rate, rapid error recovery, on-board diagnostic, two buffers of 256 KB each. Every buffer has port to VME memory and port to external I/O. The I/O port works under control of independent readout controller with token ring readout arbitration.   | 1                 |
| VBD Bus Terminator (Term)*         | Front panel VBD bus terminator. There are only two terminators in the system of Muon Readout Crates.  |                   |
| Trigger Fanout Card (TFC)*         | Two modes of operation: internal timing from sequencer, external timing from Trigger Framework (TFW). It provides both local data acquisition from different muon detectors and local testing of any part of the muon system.<br>There is only one TFC in the system of Muon Readout Crates.  | 1                 |
| Muon Fanout Card (MFC)             | Three sources of timing signals: TFW by means of SCL (16 bit at 53 MHz), TFC via Lemo and built-in timer-sequencer controlled by VME master CPU. Fanout all timing to front-end crates through VME local dedicated bus and MRCs. Hardware for crossing and turn number checking based on FIFOs.<br>Continuous hardware error handling. VMEbus interface, VMEbus interrupter.  | 1                 |
| Muon Readout Card (MRC)            | Two identical interfaces (A and B) to two front-end crates (systems). Every interface has 160 Mb/s HOTLink receiver of L3 data from front-end crates and 8 Kb dual-port memory. There are three channels for communicating with front-end crates: 1) micro-coax four line port for RF53MHz, ENC, L3DATA and L2DATA, 2) parallel connection for control of the front-ends, 3) serial controller for communication with front-end DSPs. | Up to 12          |

|   |   |   |   |   |   |   |   |   |    |                      |    |    |    |
|---|---|---|---|---|---|---|---|---|----|----------------------|----|----|----|
| M | V | T | T |   |   | M | M | M | M  | Up to 12 MRCs max... | M  |    |    |
| V | B | E | F |   |   | F | R | R | R  |                      | R  |    |    |
| M | D | R | C |   |   | C | C | C | C  |                      | C  |    |    |
| E |   | M | * |   |   |   | 1 | 2 | 3  |                      | 1  |    |    |
| 1 |   | * | * |   |   |   |   |   |    |                      | 2  |    |    |
| 6 |   |   |   |   |   |   |   |   |    |                      |    |    |    |
| 2 |   |   |   |   |   |   |   |   |    |                      |    |    |    |
|   |   |   |   |   |   |   |   |   |    |                      |    |    |    |
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | ...                  | 19 | 20 | 21 |

Positions of modules in a VME crate are fixed due the predefined disposition of cables connected to the backplane.

Modules marked with (\*) are not present in all crates.

## Addressing and Data Modes in Muon Readout VME Crates

All status and control registers have to be accessible via standard A24:D16 data mode. Short I/O data addressing mode is specifically required only for VBD Control memory. Byte wide data access mode D08(OE) is not necessary to implement as required by the VME standard.

The following is a list of existing data and addressing modes for Muon Readout Crates only:

**VME Buffer Driver** is a A24:D32:D16:D08(OE) master. As a master the VBD works in DMA mode using preprogrammed information in registers serving as pointers to buffers and word counters. In Run II the standard addressing mode to program the DMA transfers will be used. VBD's DMA controller supports block and non-block data transfers. As a slave VBD has Control memory for CSRs, pointers and error codes in short I/O space and accepts A16:D16 commands.

**Muon Fanout Card** is a A24:D16 slave. It has 8 Kbyte non-volatile memory, for errors and configuration information. All MFC's status and control registers are accessible via standard addressing mode with 16-bit data transfers.

**Muon Readout Card** is a A24:D32:D16 slave. It has 64K bytes of status registers and memory. MRC's control/status registers can be accessed via 16-bit data transfers and its memory can be accessed via 16- or 32-bit data transfers.

Readout Crate **VME processor (MVME162LX-222a)** has a default A32:D32 mode for both master and slave interfaces. Since there is no devices in Muon Readout Crates, which provide A32 mastership, it is changed to a standard A24 mode. A four Mbyte RAM is placed by default at Slave addresses \$C00000-\$FFFFFF. MVME162's Master interface is configurable and will access addresses from \$00000000 to \$00FFFFFF in the standard address mode. Full memory maps for short I/O and standard addressing modes are shown in these two tables respectively.

Muon Readout Crate short I/O address map.

| Address range | Module | Comment             |
|---------------|--------|---------------------|
| \$0000-\$9FFF | N/A    | Reserved            |
| \$A000-\$BFFF | VBD    | Control memory 8 KB |
| \$C000-\$FFFF | N/A    | Reserved            |

Muon Readout Crate standard address map

| Address range      | Module  | Comment                   |
|--------------------|---------|---------------------------|
| \$000000-\$1FFFFFF | N/A     | Reserved                  |
| \$200000-\$20FFFF  | TFC     | Status registers & memory |
| \$210000-\$21FFFF  | MFC     | Status registers & FIFOs  |
| \$220000-\$22FFFF  | MRC (1) | Event buffers & registers |
| \$230000-\$23FFFF  | MRC (2) | Event buffers & registers |
| \$240000-\$24FFFF  | MRC (3) | Event buffers & registers |
| .....              | .....   | Up to 12 MRCs             |
| \$300000-\$37FFFF  | N/A     | Reserved                  |
| \$380000-\$3FFFFFF | VBD     | Buffer Memory             |
| \$000000-\$FFFFFF  | 162LX   | VME Master                |
| \$400000-\$BFFFFFF | N/A     | Reserved                  |
| \$C00000-\$FFFFFF  | 162LX   | RAM (VME Slave)           |

## Environment for software development and routine operation

This environment is based on D0 EPICS (Experimental Physics and Industrial Control System) that is a set of software tools and applications developed by EPICS collaboration and maintained at Fermilab by Computing Division. D0 EPICS project includes VxWorks kit.

As an example of the working environment one may use a combination of the development system deployed on one of D0 SGI (or LINUX) host computers running under UNIX-like OS'es and executive real-time VxWorks kernel in MVME162LX memory.

This system implements a "Host (Server) – Target (Client-d0olmuoXX)" model of a development and application system. UNIX gives wide possibilities for program development and creation of a graphical user interface as well VxWorks provides wide set of real-time solutions. The use of two complementary and cooperating operating systems lets each do what it does best. The development system permits to edit, compile, link, to store real-time code for 68k CPUs, but then run and debug that real-time code on VxWorks.

This mode of operation is possible due to the extensive use of the network.

| Requirements to the program  |
|--|
| 1) There are at least 16 readout VME crates in the muon system.  |
| 2) Each one is controlled by a mvme162LX computer running the VxWorks kernel.  |
| 3) Each one must run the same application program during the data acquisition.   |
| 4) The differences between muon subsystems are reflected in configuration files.   |
| 5) The storage location for the configuration file is defined as a part of the non-volatile memory of MFC residing in a given crate and "protected" by a checksum. |
| 6) Each readout crate allows one telnet session for operator. The applications may be loaded and started manually from VxWorks shell.                              |
| 7) Each readout crate is a "target" executing both broadcast and target-specific commands of the main D0 coordinating programs.                                    |
| 8) There are two ways to boot: By pushing reset button and by operator command from console.   |

## Detailed sequence of actions in the muon readout crate programs.

### *Program Mure\_run*

#### Start point.

Disable system interrupts on the working VME IRQ level.  
Check MFC NVRAM. (The function vxMemProbe( ) is used here and everywhere to probe the existence of memory location.)  
Check configuration file checksum using Motorola's checksum algorithm.  
Initialize Last message address Pointer to Error Record 0,  
Copy program configuration word PCW to MFC NVRAM.  
Print program header, hostname, options and computer date and time.  
Log to NVRAM Error Records the beginning of the start-up phase.  
Allocate array for L3 Crate Header aligned to four byte boundary.  
Initialize L3 Crate Header with default values.  
Prepare array mrc\_Number[ ] according to the GS Configuration word.

#### Initialize and test MFC.

Stop the MFC embedded sequencer  
Do MFC software reset.  
Check the presence and do W/R test of Sequencer Memory.  
Check the presence of MFC registers.  
Initialize MFC by setting the default values to all bits.  
Initialize SCL receiver.  
Set the MFC to the mode TFW (external control).

#### Initialize and test TFC.

(No action at the moment)

#### Initialize and test MRCs.

Disable all MRCs (both declared and undeclared in Config file).  
Begin loop.  
    Select MRC section using configuration file.  
    Check the presence and test Dual Port RAM of the section selected.  
    Check the presence of CSR and SCC registers.  
    Initialize the serial Communication controller (SCC) of the section selected.  
    Send "Break" character to Front-End Control System via SCC.  
    Test the presence of the FE-MRC connection, set masks.  
    Reset MRC: Reframe HOTLink.  
    Reset SRQ, set DONE, Enable Section.  
    Check all status bits.  
Loop ends when all sections of the MRCs are initialized and tested.

#### Initialize and test VBD.

Check VBD Control memory is present.  
Set Enable Control memory bit in CSR.  
Set Crate type.  
Set event # Address, Crate ID Address.  
Set data and word count Access Mode by writing D-Control value.  
Set event # and crate ID Access mode by writing P-Control value.  
Set I/O Address modifier.  
Put list of word count pointers at 0x1000. Terminate it by 0 terminating word.  
Put list of data block pointers at 0x1800.  
Disable control memory access.  
Reset the VBD by writing 1 into CSR bit 0. Wait for 200 ms. VBD is ready to start DMA.

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### Initialize the VME interrupt system

Link interrupt processing subroutine itr\_SRQ to VME hardware interrupt.  
Link interrupt processing subroutine itr\_L2Acc to VME hardware interrupt.  
Link interrupt processing subroutine itr\_VBDdone to VME hardware interrupt.  
Link interrupt processing subroutine itr\_TFWinit to VME hardware interrupt.  
Set initial values to MFC's on-board VME Interrupt Controller.  
Set initial values to the Interrupt Master & Slave Controller chips.

↓

### Prepare for main wait loop

If we need to store data locally then allocate 1Mbyte buffer in mvme162's RAM and prepare header.  
Send EOI to reset both interrupt controller chips, reset MFC interrupt input registers.  
Enable interrupt from TFW init signal.  
Wait for the first init-from-TFW interrupt, execute procedure, enable other three interrupts.  
If the Sequencer mode is selected then load and start MFC sequencer.  
Log to NVRAM Error Records the end of the start-up phase and start of data acquisition.

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### Main waiting loop

Repeat main program loop waiting for any of four interrupts and checking exit condition.  
If there was a new itr\_TFWinit then increment its counter.  
If the exit condition is found then exit the loop.  
Until exit flag in MFC NV RAM is false.  
Disable system interrupts on the working VME IRQ level.  
Analyse and print the reason of exit.  
If sequencer mode is on then stop sequencer.  
Clear all interrupts. Disable the interrupt system. Free RAM data buffer.  
Exit.

### Procedure to record errors in MFC NVRAM.

Increment total number of errors.  
Update last Error Record Pointer.  
Copy time stamp to Error Record.  
Form Error Record according to required format.  
Set bit in GS status register of MFC.  
Exit the program on fatal error.

### TFW INIT Interrupt

Store Xing, Turn numbers and status in MFC NV memory (see GS spec)  
Set to zero MFC internal L1ACC, L2ACC, L2REJ counters.  
Re-frame HOTLink receivers.  
Clear error bits in status registers.  
Check for front-ends to complete INIT polling MRC Busy1 bits.  
Insert INIT\_ACK for TFW.  
Wait for INIT ends, then store Xing, Turn numbers and status in MFC NV memory.  
If exist report time-out and other errors to GS status register.  
Send EOI; return from interrupt.

### L2Acc Interrupt

Increment L2Acc counter.  
Send EOI; return from interrupt.

## SRQ Interrupt

Disable SRQ interrupts.  
Save output of FIFO5 and FIFO6 to separate locations.  
Get output FIFO2 and FIFO4 and compare to contents FIFO5 and FIFO6 correspondingly.  
If there is no coincidence, then process the event as an error.  
Repeat sequential polling of all SRQ and MRC time-out bits  
Until all SRQs are present or a time-out bit is set instead.  
If there is time-out error then store patch data in the MRC dual port memory.  
If all SRQs are present check there are no errors on RVS, T-o, connection error.  
If there is an error then mark event as erroneous.  
Check match of FIFO5 and FIFO6 to the content of XN and TN in all MRC dual port memories.  
If there is error then report error to NVRAM.  
Prepare header and trailer data for L3 event.  
Start VBD DMA transfer by setting SLV\_Ready bit.  
Send EOI bit, return from interrupt.

## VBD DONE interrupt

If we are in local mode then store data from MRC buffers to RAM buffer.  
Enable MRC "Buffer available" signals.  
Reset SLV\_Ready bit.  
Enable SRQ interrupt.  
Send EOI, return from interrupt.

### Program *Mure\_stop*

Change the Program End Word (NVPEW) located in MFC NVRAM to stop mure\_run program.

### Program *Mure\_errors*

Set working pointer to last NVRAM Error Record, input number of records to show.  
For every record print time stamp, error code, contents of FIFOs, counters and registers.

### Program *Mure\_event*

Print to screen the content of last event received from the selected MRC section (front-end system).

### Program *Mure\_mon*

Input period of time to show events and errors.  
Show periodically the last event received and recorded errors if they are present using mure\_event and mure\_errors subroutines.

### Program *Mfc\_setup*

Begin main loop.  
Print menu with options:  
1. Show configuration of GS VME Crate in MFC NVRAM  
    Print current configuration.  
2. Change configuration of GS VME Crate in MFC NVRAM  
    Input user name, password, GS ID, time update prompt. Print configuration.  
    Input crate configuration word. Print changed configuration  
3. Exit  
    Input user's selection, execute.  
End main loop. Exit

### L3 data format

The following table shows an allocation of data words in the arrays for transmission to L3 processing. To be short as possible the example is given for two data modules. All additional data modules may be inserted between the two shown.

Guidelines to L3 data format are as follows:

- The L3 data consist of L3 Muon Crate Header and a number of L3 Muon Modules.
- L3 Muon Crate Header consists of three 32-bit words.
- L3 Muon Module that comes from Front-end system consists in its turn of L3 Muon Module Header, L3 Muon front-end Data words and optional L3 Muon Trailer.
- L3 Muon Module Header consists of eight 16-bit words.
- L3 Muon front-end Data Words have the length of 16 bit.
- L3 Muon Module Trailer is added by Front-end system in case when the number of module words is odd.

#### ***L3 Muon Module Header generated by software in case of transfer errors ( Patch data)***

| Item                          | Size    | Value  | Comments  |
|-------------------------------|---------|--------|---|
| Zero word                     | 16 bits | 0x0000 | According to Muon Data Formats to L2 & L3           |
| VBD Word Count                | 16 bits | 0x0004 | According to Muon Data Formats to L2 & L3           |
| Front-end word Count          | 16 bits | 0x0006 | According to Muon Data Formats to L2 & L3           |
| Module ID                     | 16 bits | 0x03ff | Non-existing Layer, Barrel, Octant (maximum values) |
| Crossing Number               | 16 bits | 0x0000 | Default value                                       |
| Turn Number                   | 16 bits | 0x0000 | Default value                                       |
| Event Status Register (upper) | 16 bits | 0x0200 | Bit 9 is used to indicate patch data                |
| Event Status Register (lower) | 16 bits | 0x0000 | Default value                                       |

| Group Item            | Item                          | Size (bits) | Range                    | Description   |
|-----------------------|-------------------------------|-------------|--------------------------|---|
| L3 Muon Crate Header  | Crate Header Word Count       | 32          | 2                        | Length of the muon crate header in 32 bit words   |
|                       | Crate ID/Status               | 32          | 0..(2 <sup>32</sup> -1)  | Bits 00-15 Error/Status<br>Bits 16-31 Crate ID  |
|                       | Number of modules read        | 32          | 0..24                    | Number of Muon modules read   |
| L3 Muon Module Header | Zero word                     | 16          | 0                        | Upper 16 bits of the 32 bit VBD word count. Always is equal to 0 to exclude counts > (2 <sup>16</sup> -1) |
|                       | VBD Word Count                | 16 or 32    | 0.. (2 <sup>16</sup> -1) | Exclusive total word count to end of module array. If it is odd, then Padding word is added.              |
|                       | Front-end Word Count          | 16          | 0.. (2 <sup>16</sup> -1) | Inclusive number of 16-bit words in data block  |
|                       | Module ID                     | 16          | 0..(2 <sup>16</sup> -1)  | Defines Layer, Barrel, Octant, Detector type.   |
|                       | Crossing Number               | 16          | 0.. (2 <sup>8</sup> -1)  | Error bit is set for the TFW if the local crossing number differs from the L1 event crossing number       |
|                       | Turn Number                   | 16          | 0.. (2 <sup>16</sup> -1) | Local Turn number from front-end system   |
|                       | Event Status Register (upper) | 16          | 0.. (2 <sup>16</sup> -1) | Defined in document on L2 & L3 Muon Data formats  |
|                       | Event Status Register (lower) | 16          | 0.. (2 <sup>16</sup> -1) | Defined in document on L2 & L3 Muon data formats  |
| L2 Muon Data          | Data                          | 16          | 0.. (2 <sup>16</sup> -1) | First Muon front-end subsystem Data Word  |
|                       | Data<br>.....                 |             |                          | Muon front-end subsystem Data Words   |
|                       | Data                          | 16          | 0.. (2 <sup>16</sup> -1) | Last Muon front-end subsystem Data Word   |
| L3 Muon Trailer       | Padding word                  | 16          | 0xAA55                   | Is added only when Front-end Word Count is odd  |
| L3 Muon Module Header | Zero word                     | 16          | 0                        | Upper 16 bits of the 32 bit VBD word count. Always is equal to 0 to exclude counts > (2 <sup>16</sup> -1) |
|                       | VBD Word Count                | 16 or 32    | 0.. (2 <sup>16</sup> -1) | Exclusive total word count to end of module array. If it is odd, then Padding word is added.              |
|                       | Front-end Word Count          | 16          | 0.. (2 <sup>16</sup> -1) | Inclusive number of 16-bit words in data block  |
|                       | Module ID                     | 16          | 0(2 <sup>16</sup> -1)..  | Defines Layer, Barrel, Octant, Detector type.   |
|                       | Crossing Number               | 16          | 0.. (2 <sup>8</sup> -1)  | Error bit is set for the TFW if the local crossing number differs from the L1 event crossing number       |
|                       | Turn Number                   | 16          | 0.. (2 <sup>16</sup> -1) | Local Turn number from front-end system   |
|                       | Event Status Register (upper) | 16          | 0.. (2 <sup>16</sup> -1) | Defined in document on L2 & L3 Muon Data formats  |
|                       | Event Status Register (lower) | 16          | 0.. (2 <sup>16</sup> -1) | Defined in document on L2 & L3 Muon data formats  |
| L3 Muon Data          | Data                          | 16          | 0.. (2 <sup>16</sup> -1) | First Muon front-end subsystem Data Word  |
|                       | Data<br>.....                 |             |                          | Muon front-end subsystem Data Words   |
|                       | Data                          | 16          | 0.. (2 <sup>16</sup> -1) | Last Muon front-end subsystem Data Word   |
| L3 Muon Trailer       | Padding word                  | 16          | 0xAA55                   | Is added only when Front-end Word Count is odd  |

**VBD memory map and registers.**

**Short VME Addressing (A16:D16) Base Address is 0xFFFFA000**

| ## | Hex address | Size | Memory block or register        | Write/read |
|----|-------------|------|---------------------------------|------------|
| 1  | 0000        |      | CSR0                            |            |
| 2  | 0002        |      | CSR1                            |            |
| 3  | 0004        |      | CSR2                            |            |
| 4  | 0006        |      | CSR3                            |            |
| 5  | 0008        |      | Crate Type                      |            |
| 6  | 000A        |      | Event Number                    |            |
| 7  | 000C        |      | Crate ID                        |            |
| 8  | 0010        |      | D-Control                       |            |
| 9  | 0012        |      | P-Control                       |            |
| 10 | 0014        |      | I/O Address                     |            |
| 11 | 0100        |      | ERRCNT                          |            |
| 12 | 0104        |      | ERRORLIST                       |            |
| 13 | 1000        |      | WCPOINTERS list terminated by 0 |            |
| 14 | 1800        |      | DATAPointERs list               |            |

**VME Addressing (A24:D32) VBD base address is 0xF0380000**

| ## | Hex address | Size   | Memory block or register | Write/read |
|----|-------------|--------|--------------------------|------------|
| 15 | F0380000    | 256 Kb | Memory Buffer 0          | W/R        |
| 16 | F03C0000    | 256 Kb | Memory Buffer 1          | W/R        |

**Allocation of bits in VBD's CSR0**

**0xFFFFA000 - CSR0**

| 07                 | 06               | 05                                    | 04                              | 03                 | 02                 | 01                     | 00       |
|--------------------|------------------|---------------------------------------|---------------------------------|--------------------|--------------------|------------------------|----------|
| Reset VBD          | Reset Error FIFO | Disable transmit VBD buffer after DMA | Disable write to control memory | Time-out Upper Bit | Time-out Lower Bit | SelectDMA Buffer (0/1) | DMAGO    |
| 15                 | 14               | 13                                    | 12                              | 11                 | 10                 | 09                     | 08       |
| Error on CSR write | Reserved         | Reserved                              | Reserved                        | Reserved           | Reserved           | Reserved               | Reserved |

**Allocation of bits in VBD's CSR2**

**0xFFFFA004 - CSR0**

| 07        | 06             | 05          | 04       | 03                       | 02                       | 01                                  | 00                                  |
|-----------|----------------|-------------|----------|--------------------------|--------------------------|-------------------------------------|-------------------------------------|
| Reserved  | Reserved       | Reserved    | Reserved | DMA in progress Buffer 1 | DMA in progress Buffer 0 | Buffer 1 Status 0 – VME, 1-Ext.Port | Buffer 0 Status 0 – VME, 1-Ext.Port |
| 15        | 14             | 13          | 12       | 11                       | 10                       | 09                                  | 08                                  |
| DMA Error | Read-out error | Token Error | Reserved | Reserved                 | Reserved                 | Reserved                            | Reserved                            |

**TFC memory map and allocation of bits in registers**

**VME Addressing (A24:D16), TFC base address is 0xF0200000**

| ## | Hex address | Size  | Memory block or register                                   | Write/read |
|----|-------------|-------|--|------------|
| 1  | 0000        | 16 Kb | Dual Port Pattern Memory                                   |            |
| 2  | 4000        | 2     | TFC control register, CSR0                                 |            |
| 3  | 4002        | 2     | TFC status/control register, CSR1                          |            |
| 4  | 4022        | 2     | TFC HOTLink control register, CSR2                         |            |
| 5  | 4024        | 2     | TFC Fine & Coarse FC synchronization preset register, CSR3 |            |
| 6  | 4028        | 2     | TFC Channel mask and L2 delay register, CSR4               |            |
| 7  | 402A        | 2     | Crossing number and trigger delay register, CSR5           |            |

**0xF0204000 - CSR0 Control register**

| 15 | 14 | 13 | 12 | 11              | 10           | 09            | 08          | 07 | 06 | 05 | 04          | 03            | 02         | 01          | 00          |
|----|----|----|----|-----------------|--------------|---------------|-------------|----|----|----|-------------|---------------|------------|-------------|-------------|
| NC | NC | NC | NC | SINGL TRIG MODE | EXT TRIG ENB | EXT TRIG MODE | SEQ/TFW SEL | NC | NC | NC | TFC BRD RES | CLR TRIG CNTR | DO SYN SEQ | CLR TRG LAT | SET FE INIT |

**0xF0204002 – CSR1 status/control register**

| 15 | 14 | 13      | 12     | 11      | 10     | 09       | 08      | 07       | 06 | 05      | 04     | 03           | 02          | 01      | 00       |
|----|----|---------|--------|---------|--------|----------|---------|----------|----|---------|--------|--------------|-------------|---------|----------|
| NC | NC | L2 BUSY | L2 ERR | L1 BUSY | L1 ERR | INIT ACK | SCL ACK | TFC BUSY | NC | TFC ERR | SCL SL | SCL DATA ERR | SCL SYN ERR | SCL RDY | SCL INIT |

**0xF0204022 – CSR2 HOTLink control register**

| 15  | 14  | 13  | 12  | 11  | 10  | 09  | 08  | 07 | 06 | 05 | 04 | 03  | 02  | 01  | 00  |
|-----|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|-----|-----|-----|-----|
| TD7 | TD6 | TD5 | TD4 | TD3 | TD2 | TD1 | TD0 | NC | NC | NC | NC | TST | SVS | BSE | TEN |

TD7..TD0 -Test pattern, TST -Test en., SVS – Send violation symbol, BSE – BIST en., TEN – Transmit en.

**0xF0204024 – CSR3 Fine & Coarse FC synchro preset register**

| 15  | 14  | 13  | 12  | 11  | 10  | 09  | 08  | 07 | 06 | 05 | 04 | 03 | 02  | 01  | 00  |
|-----|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|----|-----|-----|-----|
| FC7 | FC6 | FC5 | FC4 | FC3 | FC2 | FC1 | FC0 | NC | NC | NC | NC | NC | FF2 | FF1 | FF0 |

FC7..FC0 - First crossing coarse counter preset (18.9 ns step), FF2..FF0 – First crossing fine delay preset

**0xF0204028 – CSR4 Channel mask and L2 pipeline delay register**

| 15  | 14  | 13  | 12  | 11 | 10 | 09  | 08  | 07  | 06  | 05  | 04  | 03  | 02  | 01  | 00  |
|-----|-----|-----|-----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| CH4 | CH3 | CH2 | CH1 | NC | NC | PD9 | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |

CH1..4 - Channel enable, PD9..PD0 - L2 decision delay preset (1..1023, 132 ns step)

**0xF020402A – CSR5 Crossing number and trigger delay register**

| 15 | 14 | 13  | 12  | 11  | 10  | 09  | 08  | 07  | 06  | 05  | 04  | 03  | 02  | 01  | 00  |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| NC | NC | LD5 | LD4 | LD3 | LD2 | LD1 | LD0 | CR7 | CR6 | CR5 | CR4 | CR3 | CR2 | CR1 | CR0 |

LD5..LD0 – Extrn. trigger delay (20..63, 132 ns step), CR5..CR0 - Extrn. trigger crossing # preset (1..159)

**Pattern memory data format (Pointer XN, Pointer TN, Event XN, Event TN, Terminator Word)**

| 15  | 14  | 13  | 12  | 11   | 10  | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|-----|-----|-----|-----|------|-----|----|----|----|----|----|----|----|----|----|----|
| 0   | 0   | 0   | 0   | 0    | 0   | 0  | 0  | X7 | X6 | X5 | X4 | X3 | X2 | X1 | X0 |
| T15 | T14 | T13 | T12 | T11  | T10 | T9 | T8 | T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 |
| 1   | L2R | L2A | L1A | 0    | 0   | 0  | 0  | X7 | X6 | X5 | X4 | X3 | X2 | X1 | X0 |
| T15 | T14 | T13 | T12 | T11  | T10 | T9 | T8 | T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 |
| 0   | 0   | 0   | 0   | TM=1 | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**MFC memory map, registers and bits.**

**MFC base address is 0xF0210000**

| ## | Hex address | Size  | Memory block or register   | Write/read |
|----|-------------|-------|--|------------|
| 1  | 0000..3FFF  | 16 KB | Sequencer Dual Port Memory   | W/R        |
| 2  | 4000..5FFF  | 8 KB  | Error Records and Timekeeping Memory                                       | W/R        |
|    | 4000        | 256   | Error record 01  |            |
|    | 4100        | 256   | Error record 02  |            |
|    | 4200        | 256   | Error record 03  |            |
|    | 4300        | 256   | Error record 04  |            |
|    | 4400        | 256   | Error record 05  |            |
|    | 4500        | 256   | Error record 06  |            |
|    | 4600        | 256   | Error record 07  |            |
|    | 4700        | 256   | Error record 08  |            |
|    | 4800        | 256   | Error record 09  |            |
|    | 4900        | 256   | Error record 10  |            |
|    | 4A00        | 256   | Error record 11  |            |
|    | 4B00        | 256   | Error record 12  |            |
|    | 4C00        | 256   | Error record 13  |            |
|    | 4D00        | 256   | Error record 14  |            |
|    | 4E00        | 256   | Error record 15  |            |
|    | 4F00        | 256   | Error record 16  |            |
|    | 5000        | 2     | Last Message Address Pointer   |            |
|    | 5002        | 206   | Reserved   |            |
|    | 50D0        | 2     | GS ID  |            |
|    | 50D2        | 2     | GS Status  |            |
|    | 50D4        | 44    | GS Mailbox area  |            |
|    | 5100        | 32    | GS Configuration file  |            |
|    | 5120        | 3562  | User defined NVRAM area  |            |
|    | 5F00        | 248   | Reserved   |            |
|    | 5FF8        | 1     | DS1643 Control ( W+R bits)   |            |
|    | 5FF9        | 1     | Seconds + OSC  |            |
|    | 5FFA        | 1     | Minutes  |            |
|    | 5FFB        | 1     | Hour   |            |
|    | 5FFC        | 1     | Day of week + FT   |            |
|    | 5FFD        | 1     | Date   |            |
|    | 5FFE        | 1     | Month  |            |
|    | 5FFF        | 1     | Year   |            |
| 3  | 6000..6FFF  | 4 KB  | FIFO Controller and Memory, Trigger Data Counters                          |            |
|    | 6000        | 2     | L1ACC_XN (FIFO 1) push from TFW when L1ACC                                 | W/R        |
|    | 6002        | 2     | L2SIM_XN (FIFO 2) push from FIFO1 when L2ACC                               | W/R        |
|    | 6004        | 2     | L1ACC_TN (FIFO 3) push from TFW when L1ACC                                 | W/R        |
|    | 6006        | 2     | L2SIM_TN (FIFO 4) push from FIFO3 when L2ACC                               | W/R        |
|    | 6008        | 2     | L2DIR_XN (FIFO 5) push from TFW when L2ACC                                 | W/R        |
|    | 600A        | 2     | L2DIR_TN (FIFO 6) push from TFW when L2ACC                                 | W/R        |
|    | 600C        | 2     | L2DIR_AQ (FIFO 7) push from TFW when L2ACC<br>(this is L3 TRANSFER NUMBER) | W/R        |
|    | 600E        | 2     | TFW_XN (FIFO 8) push from TFW when L1ACC,<br>L2ACC or L2REJ                | W/R        |
|    | 6010        | 2     | L1ACC Counter at the time of an error                                      | W/R        |
|    | 6012        | 2     | L2ACC Counter at the time of an error                                      | W/R        |
|    | 6014        | 2     | L2REJ Counter at the time of an error                                      | W/R        |
|    | 6016        | 2     | L1ACC Counter (total number)   | W/R        |
|    | 6018        | 2     | L2ACC Counter (total number)   | W/R        |
|    | 601A        | 2     | L2REJ Counter (total number)   | W/R        |

|    |            |      |   |     |
|----|------------|------|---|-----|
|    | 601C       | 2    | FIFO Status 1   | R   |
|    | 601E       | 2    | FIFO Status 2   | R   |
|    | 6020       | 2    | FIFO 1 Threshold (bits 0 - 4 are used)                      | W   |
|    | 6022       | 2    | FIFO 2 Threshold (bits 0 - 4 are used)                      | W   |
|    | 6024       | 2    | FIFO 3 Threshold (bits 0 - 4 are used)                      | W   |
|    | 6026       | 2    | FIFO 4 Threshold (bits 0 - 4 are used)                      | W   |
|    | 6028       | 2    | FIFO 5 Threshold (bits 0 - 4 are used)                      | W   |
|    | 602A       | 2    | FIFO 6 Threshold (bits 0 - 4 are used)                      | W   |
|    | 602C       | 2    | FIFO 7 Threshold (bits 0 - 4 are used)                      | W   |
|    | 602E       | 2    | FIFO 8 Threshold (bits 0 - 4 are used)                      | W   |
| 4  | 7000..7FFF | 4 KB | Reserved  |     |
| 5  | 8000..8FFF | 4 KB | Interrupt Chip 1 (Master) CA82C59A                          |     |
|    | 8000       |      | ICW1 ( 0x11 )   | W   |
|    | 8002       |      | ICW2 ( 0x50 ) For Interrupt Number 50                       | W   |
|    | 8002       |      | ICW3 ( 0x80 ) Slave is connected to Masters input IRQ7      | W   |
|    | 8002       |      | ICW4 ( 0x11 )   | W   |
|    | 8002       |      | OCW1 ( 0x00 ) Interrupts Mask for Master ( 1 - DisableIntr) | W/R |
|    | 8000       |      | OCW2 ( 0x27 )   | W/R |
|    | 8000       |      | OCW3 ( 0x08 )   | W/R |
| 6  | 9000..9FFF | 4 KB | Interrupt Chip 2 (Slave) CA82C59A                           |     |
|    | 9000       |      | ICW1 ( 0x11 )   | W   |
|    | 9002       |      | ICW2 ( 0x58 ) For Interrupt Number 58                       | W   |
|    | 9002       |      | ICW3 ( 0x07 ) Slave's Number is 7                           | W   |
|    | 9002       |      | ICW4 ( 0x01 )   | W   |
|    | 9002       |      | OCW1 ( 0x00 ) Interrupts Mask for Slave ( 1 - DisableIntr)  | W/R |
|    | 9000       |      | OCW2 ( 0x27 )   | W/R |
|    | 9000       |      | OCW3 ( 0x08 )   | W/R |
| 7  | A000..AFFF | 4 KB | VME Interrupt Controller                                    |     |
|    | A000       |      | Output Interrupt Register                                   | R   |
|    | A002       |      | Mode Register ( 0 - Level Triggered, 1 - Edge Triggered)    | W/R |
|    | A004       |      | Input Interrupt Register                                    | R   |
|    | A006       |      | Edge Selector ( 0 - Rising Edge, 1 - Falling Edge)          | W/R |
|    | A004       |      | Selective Reset Internal Interrupt Flip-flops ( 1 - Reset)  | W   |
| 8  | B000..BFFF | 4 KB | Reserved  |     |
| 9  | C000..CFFF | 4 KB | Control, Status & ID Registers                              |     |
|    | C000       |      | MFC Control Register  | W/R |
|    | C002       |      | HOTLink Control and Status Register                         | W/R |
|    | C004       |      | Error Register 1  | R   |
|    | C006       |      | Error Register 2  | R   |
|    | C008       |      | MFC Status Register   | R   |
|    | C00A       |      | INIT_XN (latched on both rising and falling edge of INIT)   | R   |
|    | C00C       |      | INIT_TN (latched on both rising and falling edge of INIT)   | R   |
|    | C00E       |      | Card ID (bits 15-08) & Serial Number (bits 07-00)           | R   |
| 10 | D000..DFFF | 4 KB | Sequencer Controller  |     |
|    | D004       | 2    | LW Data Register  | W/R |
|    | D006       | 2    | HW Data Register  | W/R |
|    | D008       | 2    | Number Of Words & Control Register (NOW)                    | W/R |
|    | D00A       | 2    | Sequencer Address Register                                  | W/R |
| 11 | E000..EFFF | 4 KB | Error Memory Controller                                     |     |
|    | E002       | 2    | L1&L2_TN Error register                                     | R   |
|    | E004       | 2    | L1&L2_XN Error register                                     | R   |
|    | E006       | 2    | L1&L2_AQ Error register                                     | R   |
|    | E008       | 2    | L1&L2_STAT Error register                                   | R   |
|    | E00A       | 2    | Data register   | W/R |
| 12 | F000..FFFF | 4KB  | Reserved  |     |

### **Error records in MFC NVRAM**

There are three types of errors recorded in the NVRAM Error Records.

FA: Fatal errors are found during initialization time. The first error found aborts the execution of the program. The format includes Time of event (00..07), Error Word (08..09), Empty space (0A..FF).

DA: Synchronization errors are found during data acquisition. The format is as shown in the table with all items filled.

TF: Errors during TFW initialization are found. Format is the same as for FA type records.

### **Format of Error records in MFC NV RAM.**

| Hex address | Item                                | Size (bytes) |
|-------------|-------------------------------------|--------------|
| 00          | Time of event in order of DS1643    | 8            |
| 08          | Error Code                          | 2            |
| 0A          | L1ACC Counter                       | 2            |
| 0C          | L2ACC Counter                       | 2            |
| 0E          | L2REJ Counter                       | 2            |
| 10          | L2ACC_TN_LAST                       | 2            |
| 12          | L2ACC_XN_LAST                       | 2            |
| 14          | L2DIR_TN                            | 2            |
| 16          | L2DIR_XN                            | 2            |
| 18          | MFC Status Register                 | 2            |
| 1A          | MFC HOTLink CSR                     | 2            |
| 1C          | MFC Error Register 1                | 2            |
| 1E          | MFC Error Register 2                | 2            |
| 20          | MRC1A CSRlo Status Register         | 2            |
| 22          | MRC1A XN                            | 2            |
| 24          | MRC1A TN                            | 2            |
| 26          | MRC1B CSRlo Status Register         | 2            |
| 28          | MRC1B XN                            | 2            |
| 2A          | MRC1B TN                            | 2            |
| 2C          | MRC2A CSRlo Status Register         | 2            |
| 2E          | MRC2A XN                            | 2            |
| 30          | MRC2A TN                            | 2            |
| ....        | .....                               | ....         |
| 9C          | MRC22B CSRlo Status Register        | 2            |
| 9E          | MRC22B XN                           | 2            |
| A0          | MRC22B TN                           | 2            |
| A2          | MRC23A CSRlo Status Register        | 2            |
| A4          | MRC23A XN                           | 2            |
| A6          | MRC23A TN                           | 2            |
| A8          | MRC23B CSRlo Status Register        | 2            |
| AC          | MRC23B XN                           | 2            |
| AE          | MRC23B TN                           | 2            |
| B0..FB      | Reserved                            |              |
| FC          | Total Number of Errors (Upper part) | 2            |
| FE          | Total Number of Errors (Lower part) | 2            |

### Configuration file format

The configuration file and operations with it must satisfy the following rules.

1. The configuration file is the single place where information on difference between crates is stored.
2. Each Muon Readout Crate must have its fixed configuration because of fixed positions of cables connected to backplane in every crate. The configuration word is used to inform the program which MRC sections are used. It is not intended to be used to change the configuration during the Run.
3. Positions of modules in VME crate slots are fixed.

| Module             | Station Number   | Comment   |
|--------------------|------------------|---|
| mvme162LX          | 1                |   |
| VBD                | 2                |   |
| VBD Bus Terminator | 3                | Optional. There is one for the VBD External Bus   |
| TFC                | 4                | Optional. Used for Local Mode.                    |
| MFC                | 7                |   |
| MRC                | 8                | First MRC in the crate. Lowest memory region      |
| MRC                | 9                | Second MRC in the crate. Next to up memory region |
| .....              |                  | Other MRCs in the crate.                          |
| MRC                | 8+(NumberOfMRCs) | Last MRC in the crate. Upper memory region        |
| Must be empty      | 20               |   |
| Must be empty      | 21               |   |

4. The number of MRCs depends on type of subsystem and may be 12 maximum.
5. Any access for modification or reading of the configuration files is performed by one special subroutine, that considers the configuration file as an encapsulated object with predefined operations on it.
6. There must be modal dialog between operator and a configuration program to set up configuration.
7. There must be time, date and name of operator in the configuration file.
8. There must be a general configuration file on some D0 server. This file must contain all configuration files for existing muon readout crates.
9. The configuration file for a given crate must be stored in the MFC's nonvolatile RAM at the starting address Base+5100.
10. The configuration file has the length of 32 bytes and contains Time and Date of this file creation, operators name, 32-bit configuration word, reserved zone filled with zeros and file checksum.
11. Bit positions of the configuration word are shown in the following.

1<sup>st</sup> (lower) byte of the configuration word

| Bits      | 7   | 6 | 5 | 4   | 3    | 2   | 1     | 0   |
|-----------|-----|---|---|-----|------|-----|-------|-----|
| Station # | 7   | 6 | 5 | 4   | 3    | 2   | 1     | N/A |
| Value     | MFC | 0 | 0 | TFC | TERM | VBD | 162LX | 0   |

2<sup>nd</sup> byte of the configuration word

| Bit       | 15    | 14    | 13    | 12    | 11    | 10    | 9     | 8     |
|-----------|-------|-------|-------|-------|-------|-------|-------|-------|
| Station # | 11    | 11    | 10    | 10    | 9     | 9     | 8     | 8     |
| Value     | MRC4B | MRC4A | MRC3B | MRC3A | MRC2B | MRC2A | MRC1B | MRC1A |

3<sup>rd</sup> byte of the configuration word

| Bit       | 23    | 22    | 21    | 20    | 19    | 18    | 17    | 16    |
|-----------|-------|-------|-------|-------|-------|-------|-------|-------|
| Station # | 15    | 15    | 14    | 14    | 13    | 13    | 12    | 12    |
| Value     | MRC8B | MRC8A | MRC7B | MRC7A | MRC6B | MRC6A | MRC5B | MRC5A |

4<sup>th</sup> (upper) byte of the configuration word

| Bit       | 31     | 30     | 29     | 28     | 27     | 26     | 25    | 24    |
|-----------|--------|--------|--------|--------|--------|--------|-------|-------|
| Station # | 19     | 19     | 18     | 18     | 17     | 17     | 16    | 16    |
| Value     | MRC12B | MRC12A | MRC11B | MRC11A | MRC10B | MRC10A | MRC9B | MRC9A |

The value of a given bit is 1 if the module is inserted into crate station or a section of a MRC is used, otherwise the value is 0.

**GS configuration file.**

| #  | Group Item           | Item                         | Size (bit) | Range                     | Encoding        |
|----|----------------------|------------------------------|------------|---------------------------|-----------------|
| 1  | Time & Date of entry | 0                            | 8          | 0                         | BCD             |
| 2  |                      | Seconds                      | 8          | 0..59                     | BCD             |
| 3  |                      | Minute                       | 8          | 1..59                     | BCD             |
| 4  |                      | Hour                         | 8          | 0..23                     | BCD             |
| 5  |                      | Day of week                  | 8          | 1..7 (Sunday=1)           | BCD             |
| 6  |                      | Date                         | 8          | 0..31                     | BCD             |
| 7  |                      | Month                        | 8          | 0..12                     | BCD             |
| 8  |                      | Year                         | 8          | 0..99                     | BCD             |
| 9  | Operators Name       | Letter 1                     | 8          | A..z                      | ASCII           |
| 10 |                      | Letter 2                     | 8          | A..z                      | ASCII           |
| 11 |                      | Letter 3                     | 8          | A..z                      | ASCII           |
| 12 |                      | Letter 4                     | 8          | A..z                      | ASCII           |
| 13 |                      | Letter 5                     | 8          | A..z                      | ASCII           |
| 14 |                      | Letter 6                     | 8          | A..z                      | ASCII           |
| 15 |                      | Letter 7                     | 8          | A..z                      | ASCII           |
| 16 |                      | Letter 8                     | 8          | A..z                      | ASCII           |
| 17 | Configuration word   | 1 <sup>st</sup> (Lower) byte | 8          | 0..1 for bits 1,2,3,4,7 * | By bit position |
| 18 |                      | 2 <sup>nd</sup> byte         | 8          | 0..1 for bits 8..15 *     | By bit position |
| 19 |                      | 3 <sup>rd</sup> byte         | 8          | 0..1 for bits 16..19 *    | By bit position |
| 20 |                      | 4 <sup>th</sup> (Upper) byte | 8          | 0                         |                 |
| 21 | Reserved Zone        |                              | 8          | 0                         |                 |
| 22 |                      |                              | 8          | 0                         |                 |
| 23 |                      |                              | 8          | 0                         |                 |
| 24 |                      |                              | 8          | 0                         |                 |
| 25 |                      |                              | 8          | 0                         |                 |
| 26 |                      |                              | 8          | 0                         |                 |
| 27 |                      |                              | 8          | 0                         |                 |
| 28 |                      |                              | 8          | 0                         |                 |
| 29 |                      |                              | 8          | 0                         |                 |
| 30 |                      |                              | 8          | 0                         |                 |
| 31 | Check sum            | Check sum (L)                | 8          | 0..255                    | Binary          |
| 32 |                      | Check sum (H)                | 8          | 0..255                    | Binary          |

\* Remark: other bits must be 0

**Allocation of bits in MFC registers**

**0xF021601C – FIFO Status 1 Register**

|                 |                 |                 |                 |                 |                 |                 |                 |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| 07              | 06              | 05              | 04              | 03              | 02              | 01              | 00              |
| FIFO08<br>EMPTY | FIFO07<br>EMPTY | FIFO06<br>EMPTY | FIFO05<br>EMPTY | FIFO04<br>EMPTY | FIFO03<br>EMPTY | FIFO02<br>EMPTY | FIFO01<br>EMPTY |
| 15              | 14              | 13              | 12              | 11              | 10              | 09              | 08              |
| FIFO08<br>FULL  | FIFO07<br>FULL  | FIFO06<br>FULL  | FIFO05<br>FULL  | FIFO04<br>FULL  | FIFO03<br>FULL  | FIFO02<br>FULL  | FIFO01<br>FULL  |

**0xF021601E – FIFO Status 2 Register**

|                   |                   |                   |                   |                   |                   |                   |                   |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| 07                | 06                | 05                | 04                | 03                | 02                | 01                | 00                |
| FIFO08<br>THR_OVF | FIFO07<br>THR_OVF | FIFO06<br>THR_OVF | FIFO05<br>THR_OVF | FIFO04<br>THR_OVF | FIFO03<br>THR_OVF | FIFO02<br>THR_OVF | FIFO01<br>THR_OVF |
| 15                | 14                | 13                | 12                | 11                | 10                | 09                | 08                |
| FIFO08<br>BUSY    | FIFO07<br>BUSY    | FIFO06<br>BUSY    | FIFO05<br>BUSY    | FIFO04<br>BUSY    | FIFO03<br>BUSY    | FIFO02<br>BUSY    | FIFO01<br>BUSY    |

**0xF021A004 – Input Interrupt Control Register ( R )**

|                                 |                                    |                                   |                       |                |                |                 |                      |
|---------------------------------|------------------------------------|-----------------------------------|-----------------------|----------------|----------------|-----------------|----------------------|
| 07                              | 06                                 | 05                                | 04                    | 03             | 02             | 01              | 00                   |
| IRQ<br>SLAVE<br>INTERR.<br>CHIP | IRQ07<br>INIT_<br>FALLING_<br>EDGE | IRQ06<br>INIT_<br>RISING_<br>EDGE | IRQ05<br>SRQ          | IRQ4<br>L2REJ  | IRQ3<br>L2ACC  | IRQ2<br>L1ACC   | IRQ1<br>VBD_<br>DONE |
| 15                              | 14                                 | 13                                | 12                    | 11             | 10             | 09              | 08                   |
| INIT_ACK_<br>VME                | IRQ14<br>MFC_INT_<br>ERROR         | IRQ13<br>FIFO<br>EMPTY            | IRQ12<br>FIFO<br>FULL | IRQ11<br>L2ERR | IRQ10<br>L1ERR | IRQ09<br>L2BUSY | IRQ08<br>L1BUSY      |

**0xF021A002 - VME Interrupt Controller Mode Register ( R/W )**

|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 15  | 14  | 13  | 12  | 11  | 10  | 09  | 08  | 07  | 06  | 05  | 04  | 03  | 02  | 01  | 00  |
| M15 | M14 | M13 | M12 | M11 | M10 | M09 | M08 | M07 | M06 | M05 | M04 | M03 | M02 | M01 | M00 |

M15..M00 bits select interrupt trigger mode: 0 - Edge triggering, 1 - Level triggering.

**0xF021A006 - VME Interrupt Controller Edge Selector ( R/W )**

|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 15  | 14  | 13  | 12  | 11  | 10  | 09  | 08  | 07  | 06  | 05  | 04  | 03  | 02  | 01  | 00  |
| E15 | E14 | E13 | E12 | E11 | E10 | E09 | E08 | E07 | E06 | E05 | E04 | E03 | E02 | E01 | E00 |

E15..E00 bits select interrupt trigger edge: 0 - positive (rising), 1 - negative (falling).

**0xF021A004 - VME Interrupt Controller Edge Flip-Flop Selective Reset Register ( W )**

|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 15  | 14  | 13  | 12  | 11  | 10  | 09  | 08  | 07  | 06  | 05  | 04  | 03  | 02  | 01  | 00  |
| R15 | R14 | R13 | R12 | R11 | R10 | R09 | R08 | R07 | R06 | R05 | R04 | R03 | R02 | R01 | R00 |

R15..R00 bits select edge triggered interrupt flip-flop that is to reset: 0 – no action, 1 - reset.

**0xF021A000 – Output Interrupt Control Register ( R )**

|                                 |                                    |                                   |                       |                |                |                 |                      |
|---------------------------------|------------------------------------|-----------------------------------|-----------------------|----------------|----------------|-----------------|----------------------|
| 07                              | 06                                 | 05                                | 04                    | 03             | 02             | 01              | 00                   |
| IRQ<br>SLAVE<br>INTERR.<br>CHIP | IRQ07<br>INIT_<br>FALLING_<br>EDGE | IRQ06<br>INIT_<br>RISING_<br>EDGE | IRQ05<br>SRQ          | IRQ4<br>L2REJ  | IRQ3<br>L2ACC  | IRQ2<br>L1ACC   | IRQ1<br>VBD_<br>DONE |
| 15                              | 14                                 | 13                                | 12                    | 11             | 10             | 09              | 08                   |
| INIT_ACK_<br>VME                | IRQ14<br>MFC_INT_<br>ERROR         | IRQ13<br>FIFO<br>EMPTY            | IRQ12<br>FIFO<br>FULL | IRQ11<br>L2ERR | IRQ10<br>L1ERR | IRQ09<br>L2BUSY | IRQ08<br>L1BUSY      |

### 0xF021C000 - MFC Control Register

|          |               |               |               |               |       |         |       |
|----------|---------------|---------------|---------------|---------------|-------|---------|-------|
| 07       | 06            | 05            | 04            | 03            | 02    | 01      | 00    |
| INIT_MSK | SYS<br>BY VME | EXT<br>BY VME | INT<br>BY VME | CAM<br>BY VME |       |         |       |
| 15       | 14            | 13            | 12            | 11            | 10    | 09      | 08    |
| BU2_MSK  | L2BUSY        | BU1_MSK       | L1BUSY        | ER2_MSK       | L2ERR | ER1_MSK | L1ERR |

MSK – mask, where 0 – set by MRC, 1 – set by program (VME). An event will be program simulated by writing 1 to bits 8,10,12,14 when corresponding bits 9,11,13,15 are set to 1.

### 0xF021C002 - HOTLink Control Register

|             |                    |                |                  |               |               |               |                |
|-------------|--------------------|----------------|------------------|---------------|---------------|---------------|----------------|
| 07          | 06                 | 05             | 04               | 03            | 02            | 01            | 00             |
| SLV_<br>RDY | RESET_<br>INIT_ACK | K28_SYS_<br>HL | RESET_<br>HL_ERR | RESET_<br>SW  | BISTEN_<br>HL | SVS_<br>HL    | REFR_<br>HL    |
| 15          | 14                 | 13             | 12               | 11            | 10            | 09            | 08             |
| -           | -                  | -              | -                | SYNC_<br>LOST | ACK_<br>SCL   | REFR_<br>RCVR | TRANSM_<br>ENA |

### 0xF021C004 - Error Register 1

|              |             |                |                |               |               |                |                |
|--------------|-------------|----------------|----------------|---------------|---------------|----------------|----------------|
| 07           | 06          | 05             | 04             | 03            | 02            | 01             | 00             |
| L2DEC        | L1DEC       | L2BUSY_<br>MRC | L1BUSY_<br>MRC | L2ERR_<br>MRC | L1ERR_<br>MRC | SRQ            | INIT           |
| 15           | 14          | 13             | 12             | 11            | 10            | 09             | 08             |
| SEQ_<br>BUSY | SCL_<br>ERR | SCL_<br>RDY    | INIT_ACK       | CAM           | SYST_<br>VME  | EXTERN_<br>VME | INTERN_<br>VME |

### 0xF021C006 - Error Register 2

|                  |                |                    |                    |                   |                   |                 |                |
|------------------|----------------|--------------------|--------------------|-------------------|-------------------|-----------------|----------------|
| 07               | 06             | 05                 | 04                 | 03                | 02                | 01              | 00             |
| SCL_SYN<br>C_ERR | CV_<br>ERR_TFC | CLK_<br>ERR_TFC    | FRAME_<br>ERR_TFC  | E4_ERR_<br>TFC    | E2_ERR_<br>TFC    | E1_ERR_<br>TFC  | E0_ERR_<br>TFC |
| 15               | 14             | 13                 | 12                 | 11                | 10                | 09              | 08             |
| TOUT_<br>REFR    | TOUT_<br>BIST  | L2BUSY<br>(MASKED) | L1BUSY<br>(MASKED) | L2ERR<br>(MASKED) | L1ERR<br>(MASKED) | SCL_<br>DATE_ER | MODE_<br>ERR   |

### 0xF021C008 - MFC Status Register

|                    |                     |                     |                    |                     |                       |                       |               |
|--------------------|---------------------|---------------------|--------------------|---------------------|-----------------------|-----------------------|---------------|
| 07                 | 06                  | 05                  | 04                 | 03                  | 02                    | 01                    | 00            |
| ID_<br>CNTR_<br>OK | SEQ_<br>CNTR_<br>OK | SIGN_<br>MUX_<br>OK | HL_<br>CNTR_<br>OK | ERR_<br>CNTR_<br>OK | INTER_<br>CNTR_<br>OK | LOADER_<br>VME_<br>OK | STAT_<br>OK   |
| 15                 | 14                  | 13                  | 12                 | 11                  | 10                    | 09                    | 08            |
| BISOK              | REFD                | DSTREAM             | CONN               | RVC_<br>GLOBAL      | RVC_<br>BIST          | OVF_<br>DTSTR         | RVC_<br>DTSTR |

### 0xF021C00A - INIT\_XN Register

|    |    |    |    |    |    |    |    |          |          |          |          |          |          |          |          |
|----|----|----|----|----|----|----|----|----------|----------|----------|----------|----------|----------|----------|----------|
| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07       | 06       | 05       | 04       | 03       | 02       | 01       | 00       |
| -  | -  | -  | -  | -  | -  | -  | -  | XN<br>07 | XN<br>06 | XN<br>05 | XN<br>04 | XN<br>03 | XN<br>02 | XN<br>01 | XN<br>00 |

This register is latched both on INIT rising edge and on INIT falling edge

### 0xF021C00C - INIT\_TN Register

|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
| TN |
| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |

This register is latched both on INIT rising edge and on INIT falling edge

**0xF021C00E - Card ID & Serial Number Register**

|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 15  | 14  | 13  | 12  | 11  | 10  | 09  | 08  | 07  | 06  | 05  | 04  | 03  | 02  | 01  | 00  |
| ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 | SN7 | SN6 | SN5 | SN4 | SN3 | SN2 | SN1 | SN0 |

**0xF021D008 - Number of Words and Sequencer Control Register**

|              |          |      |       |      |      |      |      |
|--------------|----------|------|-------|------|------|------|------|
| 07           | 06       | 05   | 04    | 03   | 02   | 01   | 00   |
| WN07         | WN06     | WN05 | WN04  | WN03 | WN02 | WN01 | WN00 |
| 15           | 14       | 13   | 12    | 11   | 10   | 09   | 08   |
| INIT_ACK_VME | INIT_VME | MODE | START | WN11 | WN10 | WN09 | WN08 |

**0xF021E002 - L1&L2\_TN Register**

|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
| TN |
| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |

**0xF021E004 - L1&L2\_XN Register**

|    |    |    |    |    |    |    |    |     |     |     |     |     |     |     |     |
|----|----|----|----|----|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07  | 06  | 05  | 04  | 03  | 02  | 01  | 00  |
| -  | -  | -  | -  | -  | -  | -  | -  | XN7 | XN6 | XN5 | XN4 | XN3 | XN2 | XN1 | XN0 |

**0xF021E006 - L1&L2\_AQ Register**

|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 15  | 14  | 13  | 12  | 11  | 10  | 09  | 08  | 07  | 06  | 05  | 04  | 03  | 02  | 01  | 00  |
| E15 | E14 | E13 | E12 | E11 | E10 | E09 | E08 | E07 | E06 | E05 | E04 | E03 | E02 | E01 | E00 |

**0xF021E008 - L1&L2 Status Register**

|    |    |      |       |       |       |       |       |
|----|----|------|-------|-------|-------|-------|-------|
| 07 | 06 | 05   | 04    | 03    | 02    | 01    | 00    |
| 0  | 0  | INIT | L2ERR | L1ERR | L2REJ | L2ACC | L1ACC |
| 15 | 14 | 13   | 12    | 11    | 10    | 09    | 08    |
| 0  | 0  | 0    | 0     | 0     | 0     | 0     | 0     |

Information is latched on ERROR Interrupt (on L1ERR or L2ERR)

**MRC memory map, registers and bits.**

**MRC base address is 0xF02y0000..0xF02yFFFF, where y=2,3,4,5,6,7,8,9,A,B,C,D.**

| ## | Hex address | Size | Memory block or register                           | Write/read |
|----|-------------|------|--|------------|
| 1  | 2000..3FFF  | 8 KB | Dual-Port RAM Section A (Changed in January, 2000) | W/R        |
| 2  | 4000        | 0    | Reset SCC AM85C30                                  | W          |
| 3  | 4010        | 4    | CSR of Section A                                   | W/R        |
| 4  | 8000..9FFF  | 8 KB | Dual-Port RAM Section                              | W/R        |
| 5  | C000        | 1    | SCC Channel B; Access to Control Registers         | W/R        |
| 6  | C004        | 1    | SCC Channel A; Access to Control Registers         | W/R        |
| 7  | C008        | 1    | SCC Channel B; Access to Data Registers            | W/R        |
| 8  | C00C        | 1    | SCC Channel A; Access to Data Registers            | W/R        |
| 9  | C010        | 4    | CSR of Section B                                   | W/R        |

**Allocation of bits in MRC CSR registers**

**0xF02y4010 (0xF02yC010) – Control/Status Register A (B) Highest 16 bits Read**

| 07          | 06          | 05         | 04         | 03        | 02          | 01                  | 00                |
|-------------|-------------|------------|------------|-----------|-------------|---------------------|-------------------|
| NOT_DEFINED | NOT_DEFINED | BISOK      | REFD       | DONE_TEST | SRQ_TEST    | ERROR2_TEST         | ERROR1_TEST       |
| 15          | 14          | 13         | 12         | 11        | 10          | 09                  | 08                |
| ERROR2_MASK | ERROR1_MASK | BUSY2_MASK | BUSY1_MASK | SRQ_MASK  | NOT_DEFINED | CSR_A_B<br>A=0, B=1 | DSTR_EN<br>STATUS |

**0xF02y4010 (0xF02yC010) – Control/Status Register A (B) Highest 16 bits Write**

| 07          | 06          | 05         | 04         | 03        | 02       | 01          | 00          |
|-------------|-------------|------------|------------|-----------|----------|-------------|-------------|
| SRQ_RESET   | DONE_RESET  | BIST       | REF        | DONE_TEST | SRQ_TEST | ERROR2_TEST | ERROR1_TEST |
| 15          | 14          | 13         | 12         | 11        | 10       | 09          | 08          |
| ERROR2_MASK | ERROR1_MASK | BUSY2_MASK | BUSY1_MASK | SRQ_MASK  | RESET    | NOT_DEFINED | DSTR_EN     |

**0xF02y4012 (0xF02yC012) – Control/Status Register A (B) Lowest 16 bits Read-only**

| 07     | 06      | 05        | 04        | 03       | 02       | 01       | 00               |
|--------|---------|-----------|-----------|----------|----------|----------|------------------|
| INTSCC | RVS_GLB | TOUT_REFR | TOUT_BIST | RVS_BIST | OVF_DSTR | RVS_DSTR | TOUT_DSTR        |
| 15     | 14      | 13        | 12        | 11       | 10       | 09       | 08               |
| ERROR2 | ERROR1  | BUSY2     | BUSY1     | SRQ      | DONE     | DSTREAM  | CONN<br>(MFC-FE) |

**States and Errors recorded by Muon Readout Crate Software**

| <i>Error Code</i> | <i>Error explanation</i>  | <i>Action</i> |
|-------------------|---|---------------|
| 0x0000            | No errors   | Transfer data |
|                   | <b>States of the Muon Readout code</b>                          |               |
| 0x0001            | Mure_run start_up is started                                    | Test hardware |
| 0x0002            | Mure_run data acquisition is started                            | Transfer data |
| 0x0004            | Mure_run data acquisition is stopped                            | Exit          |
|                   | <b>Errors detected during program start-up</b>                  |               |
| 0x4001            |   |               |
| 0x4002            | MFC Sequencer Memory is not found or has errors                 | Exit          |
| 0x4004            | Some registers are not found in the MFC                         | Exit          |
| 0x4008            | MFC SCL synchronization Error                                   | Exit          |
| 0x4010            | MRC Dual Port Memory is not found or has errors                 | Exit          |
| 0x4020            | Some registers are not found in the MRC                         | Exit          |
| 0x4040            | MRC HOTLink has synchronization error or cable is not connected | Exit          |
| 0x4080            | MRC HOTLink Reframe Error                                       | Exit          |
| 0x4100            | Some VBD registers were not found                               | Exit          |
| 0x4200            | VBD initialization was not successful                           | Exit          |
| 0x4400            | VBD RAM is not found or has errors                              | Exit          |
| 0x4800            | Some interrupt routines were not linked                         | Exit          |
| 0x5000            | MFC NVRAM Configuration file has checksum error                 | Exit          |
| 0x6000            | Reserved  |               |
|                   | <b>Errors detected during data acquisition</b>                  |               |
| 0x8001            | TFW XN sequence error   | Transfer data |
| 0x8002            | TFW TN sequence error   | Transfer data |
| 0x8004            | Software time-out of any SRQ                                    | Send patch    |
| 0x8008            | MRC hardware time-out   | Send patch    |
| 0x8010            | Front-End XN sequence error                                     | Transfer data |
| 0x8020            | Front-End TN sequence error                                     | Transfer data |
| 0x8040            | Event length in L3 Header is greater than 8K bytes              | Send patch    |
| 0x8080            | Reserved  |               |
| 0x8100            | Reserved  |               |
| 0x8200            | Reserved  |               |
| 0x8400            | Reserved  |               |
| 0x8800            | Reserved  |               |
| 0x9000            | Reserved  |               |
| 0xa000            | Reserved  |               |
|                   | <b>Errors detected during TFW initialization procedure</b>      |               |
| 0xc001            | MRC HOTLink has no connection to FE                             | Exit          |
| 0xc002            | MRC HOTLink Reframe Error during TFW INIT                       | Exit          |
| 0xc004            | Some FE did not set BUSY1 on TFW INIT                           | Exit          |
| 0xc008            | Some FE did not reset BUSY1 during TFW INIT                     | Exit          |
| 0xc010            | TFW did not remove INIT within 5 seconds after IACK reset       | Exit          |
| 0xc020            | Reserved  |               |
| 0xc040            | Reserved  |               |
| 0xc080            | Reserved  |               |
| 0xc100            | Reserved  |               |
| 0xc200            | Reserved  |               |
| 0xc400            | Reserved  |               |
| 0xc800            | Reserved  |               |
| 0xd000            | Reserved  |               |
| 0xe000            | Reserved  |               |

## Using the mure\_run program

### **Starting**

-> <Gomu      Delete previous task t\_mure\_run,  
                 Unload previous image of the program mure\_run  
                 Load new image of the program mure\_run  
                 Spawn new task t\_mure\_run as separate parallel process

### **Monitoring**

-> mure\_mon 5, 0x0022                      Monitor data, status and errors  
                 |                      ||                      during data taking  
                 |                      | section number  
                 |                      enable section bit  
                 |                      period in seconds

-> ^C                      Stop mure\_mon.  
                                 Let mure\_run continue data taking.  
                                 Operator may issue shell commands.

-> mure\_errors 3      Show last status/errors records registered in MFC NVRAM  
                         |  
                         number of records to show

### **Stopping**

-> mure\_stop                      Stop operation of mure\_run  
                                 Delete task mure\_run

### **Configuring**

-> mfc\_setup                      Run if you need to change configuration in the VME crate

### MCH3 Muon readout crates layout, 9/11/00

|   | M314                                  | M315   | M316                                  | M317                                  | M318                                  | M319                                  | M320   | M321                        | M322                          | M323   | M324                   |
|---|---------------------------------------|--|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|--|-----------------------------|-------------------------------|--|------------------------|
| 0 | d00lmuo24<br>South<br>FMSM<br>GS 0x30 | Power<br>Supply<br>314-0 316-0                                   | d00lmuo22<br>South<br>FMSS<br>GS 0x32 | d00lmuo11<br>West<br>CMWTP<br>GS 0x34 | d00lmuo12<br>East<br>CMETP<br>GS 0x38 | VRC7                                  | Power<br>Supply<br>319-0 321-0                               | d00lmuo20<br>L1C<br>GS 0x16 | d00lmuo18<br>L1mgr<br>GS 0x19 | Power<br>Supply<br>322-0 324-0                                   | parallel<br>processors |
| 1 | d00lmuo19<br>North<br>FMNM<br>GS 0x31 | Terminal   | d00lmuo17<br>North<br>FMNS<br>GS 0x33 | d00lmuoXX<br>West<br>CMWSP<br>GS 0x35 | d00lmuo23<br>East<br>CMESP<br>GS 0x39 | d00lmuo01<br>East<br>CMESC<br>0x3b    | Terminal   | d00lmuo29<br>L1S<br>GS 0x18 | d00lmuo08<br>L1N<br>GS 0x17   | Coaxial<br>Input Cnvtrs<br>(L2)                                  |                        |
| 2 | Spare<br>VME 1                        | Power<br>Supply<br>314-1 316-1<br>Power<br>Supply<br>314-2 316-2 | Spare<br>VME 2                        | d00lmuoXX<br>West<br>CMWBP<br>GS 0x36 | d00lmuoXX<br>East<br>CMEBP<br>GS 0x3a | d00lmuo06<br>West<br>CMWSC<br>GS 0x37 | Power<br>Supply<br>(blank)<br>Power<br>Supply<br>318-2 318-1 | CFT PS<br>tmngr R/O         | VEPA Crate                    | Power<br>Supply<br>322-1 324-1<br>Power<br>Supply<br>322-2 324-2 |                        |
| 3 |                                       | Power<br>Supply<br>317-1 317-0                                   |                                       | Power<br>Supply<br>----- 318-0        |                                       |                                       | Power<br>Supply<br>319-1 319-2                               |                             |                               | Power<br>Supply<br>321-2 321-1                                   |                        |

Last Updated on 9/11/00 by Darien Wood (moved VRC crates, fixed inconsistent crate numbering (0,1,2 instead of 1,2,3))  
 Host Names & GS ID added on 8/17/00 by I. N. Churin