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MINI-DRIFT TUBE READOUT CONTROLLER SPECIFICATION

Preliminary

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1. Introduction

The Mini-Drift Tube Readout Controller (MDRC) is a part of the D0 Muon Mini-Drift Tube Chamber Electronics[1]. The Mini-Drift Tube (MDT) Electronics includes on-chamber Amplifier-Discriminator Boards (ADB)[2], MDC[3] and Mini-Drift Tube Readout Controller. The MDC and MDRC are housed in 9U VME crates located on the detector platform. A block diagram of the MDT FE is shown in Fig. 1. Each crate carries up to 15 MDCs, an MDRC and a VME Master. MDCs running under control of the MDRC are continuously digitizing ADB data and sending raw hit information to the L1 Trigger. The MDRC is responsible for submitting L2 and L3 Data upon request of the Trigger Logic.

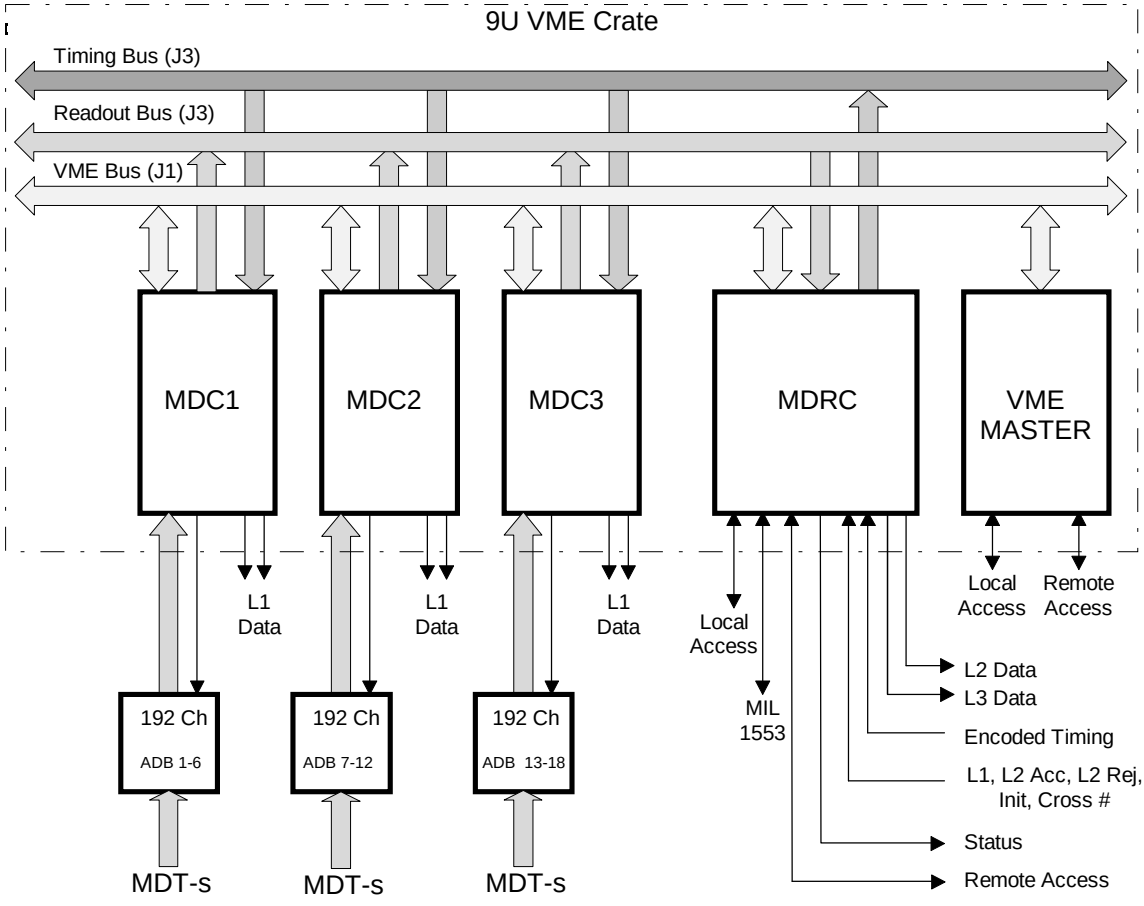


Fig. 1. MDT Front End Electronics

A set of serial control links provide flexibility in remote control and initializing procedures during setup and run. Block diagram of the MDRC in shown Fig. 2. The MDRC incorporates in it as many as four different functionalities: MDT Readout Controller, VME Slave, MDT Communication Controller and MDT Monitor.

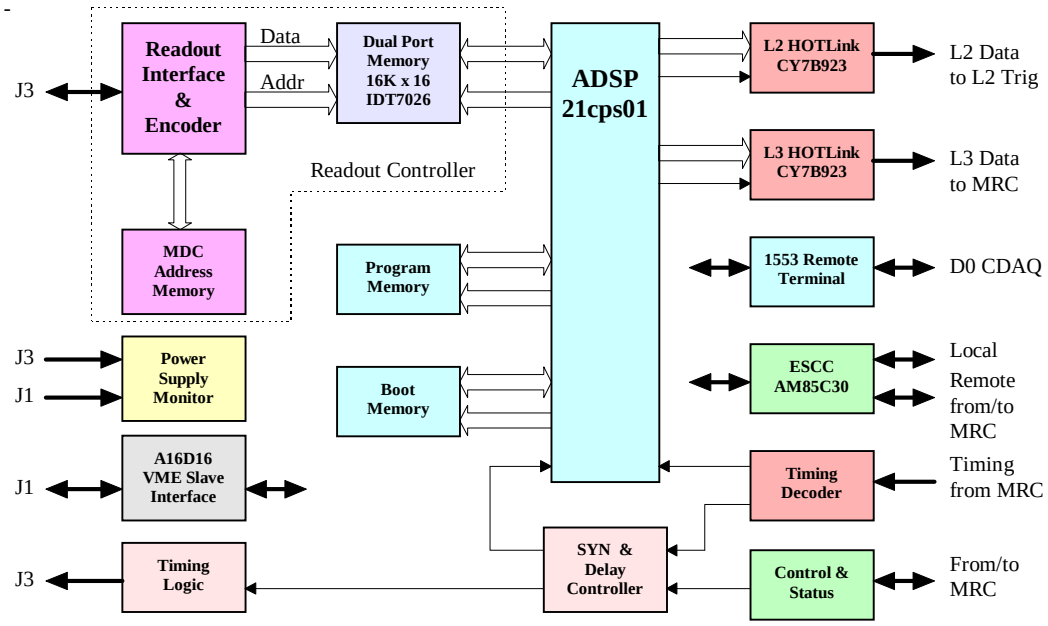


Fig. 2. MDRC Block Diagram

The MDRC as a Readout Controller can perform the following functions:

- receive encoded timing signals[45,] from the MRC, decode, adjust and pass it to the MDCs over the Timing Bus;
- upon receiving an L1 Accept signal:
  - ⇒ pass it to all MDCs in the crate to force them saving the corresponding event in the L1 FIFOs;
  - ⇒ read out saved data over the Readout Bus. Up to 15 MDCs can be served in a crate;
  - ⇒ check the validity of the data and signal to the MRC any errors occurred;
  - ⇒ sparsify and format the data and write it down into the Dual Port Memory to make it accessible for further processing with the DSP;
  - ⇒ send out formatted data to the L2 Trigger over the L2 HOTLink at a 160 Mbit/sec rate;
- process and reformat data for the L3 Trigger requirements;
- upon getting L2 Accept or L2 Reject signals either transmit data to the L3 Trigger over the L3 HOTLink or discard it.

The MDRC as a VME Slave has the A16D16 VME Slave Interface which has access to all downloadable and readable registers and memories of the module.

The MDRC as an MDT Communication Controller provides the following features:

- MIL 1553 Remote Terminal Interface;
- Local and Remote Serial Interface based on the Am85C30 - Enhanced Serial Communications Controller chip.

The MDRC as an MDT Monitor monitors the crate power supplies and temperature, and has comprehensive embedded testing capabilities of the MDCs and ADBs.

2. Mechanical Specification

The MDT Chamber Electronics is based on VME 9U crates widely used in D0. It is assumed that each MDT crate constitutes a stand-alone readout station within the D0 detector and therefore has to have an individual AC outlet available on the platform. The MDRC is implemented as 9U by 280 mm VME card. The MDRC uses three backplane connectors for the following functions:

- **J1/J2** connections for standard VME operations;
- custom **J3** connections for fast 64-bit wide data readout and for timing & control signals.

The rest of connectors are located on the front panel of the MDRC:

- 4- coaxial flat cable connector carrying:
  - ⇒ encoded timing information from MRC to MDRC;
  - ⇒ 53 Mhz RF clock from MRC to MDRC;
  - ⇒ L2 Trigger Data from MDRC;
  - ⇒ L3 Trigger Data from MDRC;
- A 50-pin ribbon cable connector carrying:
  - ⇒ INIT from MRC;
  - ⇒ L1 ACC from MRC;
  - ⇒ L2 ACC and L2 REJECT from MRC;
  - ⇒ CROSSING #, 8 bit from MRC;
  - ⇒ STRB and DONE from MRC.
  - ⇒ Remote Serial Interface from MRC;
  - ⇒ ERROR and BUSY from MDRC to MRC;
- MIL 1553 Serial Interface Connector;
- Local Serial Interface Connector;
- Output and input LEMO connectors for local triggering;
- LEDs indicating module status.

3. Timing Bus

The MDRC Timing Bus synchronizers operation of all MDCs in the crate using a single time critical signal line (RF/7 = 7,58628 MHz) on a custom J3 backplane. All the rest timing signals (/First Crossing, /L1 Accept, /Gap, and /Test) are resynchronized by a falling edge of the RF/7 inside the MDCs (Fig. 3). This approach has the following advantages:

- lower reference clock frequency transmitted over the backplane keeps it more quiet;
- the rest of timing signals are not really timing any more as they have significantly greater setup and hold times for resynchronization;
- MDC gate position adjustment requires just a single programmable silicon delay line.

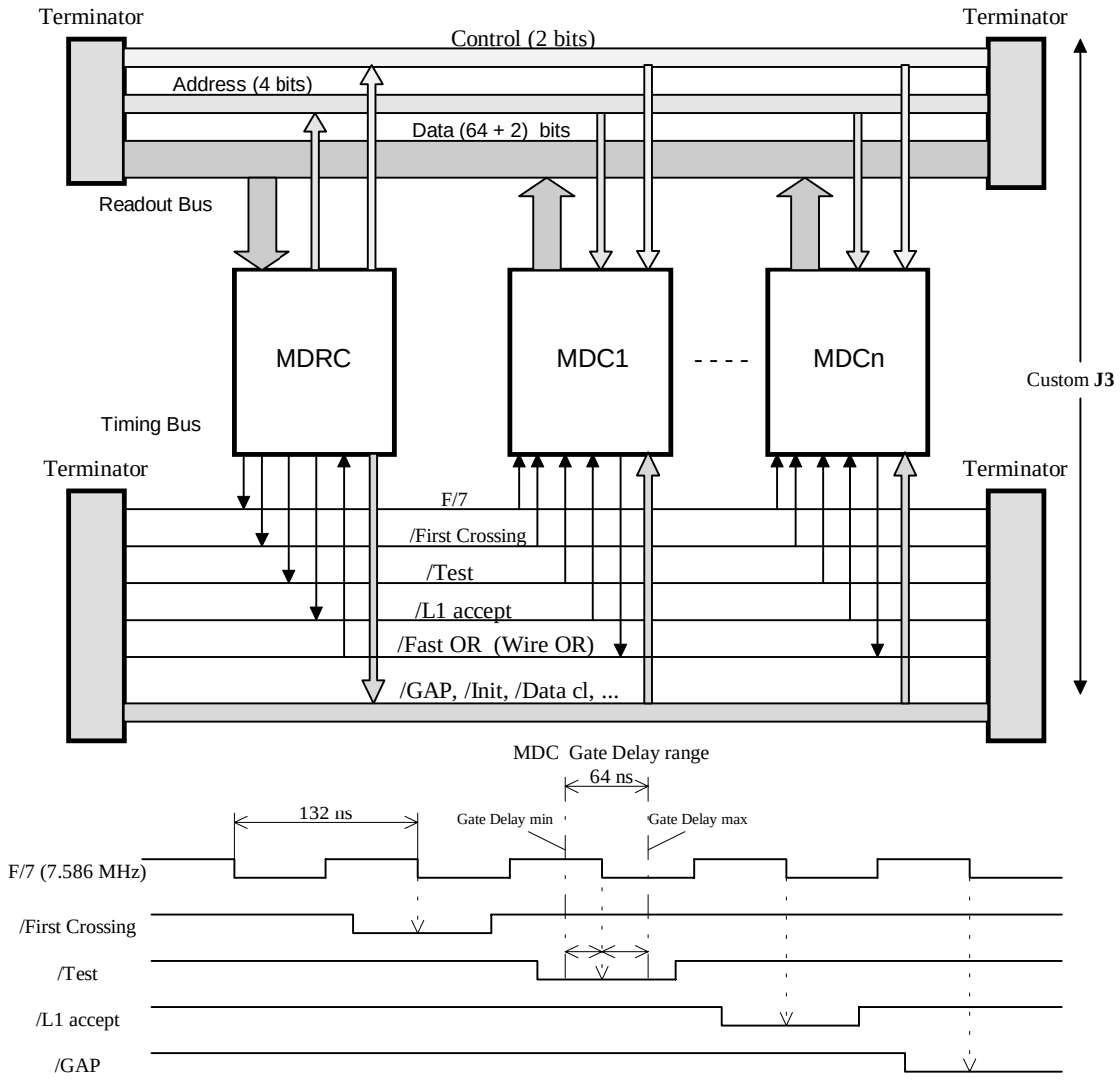


Fig. 3. MDT Readout and Timing block diagram

4. Readout Controller

A block diagram of the Readout Controller is shown in Fig. 4. The Readout Controller performs the following functions:

- maintains the data readout protocol with MDCs;
- supports two modes of data processing:
  - ⇒ Sparse Mode, when each hit is encoded into a separate 16-bit word while zeros are skipped, Table 1;
  - ⇒ Fixed Mode, when a single bit carries a channel hit information and all channels are present at the output, Table **1.** Sparse Mode Data Format.
  - ⇒ ;
- loads preformatted data into the Dual Port Memory, making it available for DSP processing;
- calculates the Data Block Length of the processed data and puts it as a header of the current block;

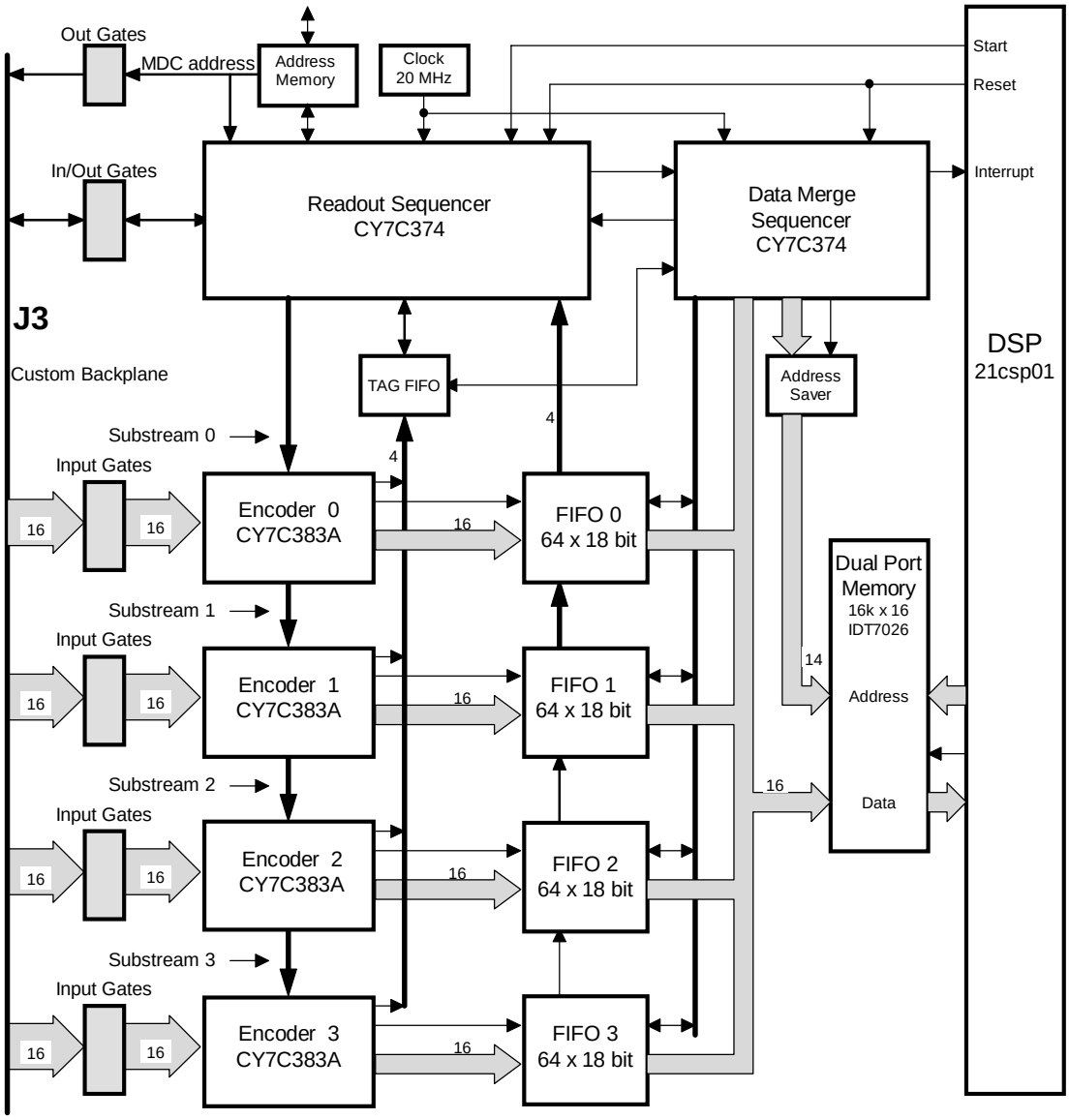


Fig. 4. MDRC Readout Interface block diagram.

To improve data peak throughput of the Readout Controller, input data stream is split into 4 Substreams, each of which is 16-bit wide and feeds a separate Encoder.

Encoder is implemented as a pipelined state machine, with an intrinsic processing delay of 300ns. While in Sparse Mode The Readout Controller is capable to maintain a steady readout and encoding rate at 80Mbyte/sec, if number of hits in each 16-bit word is below 6. If number of hits exceeds the specified value, each excessive hit holds the readout process by 50ns. The Encoder writes output data into a strobed FIFO. A dedicated Tag FIFO keeps marks of the not empty input words in each substream. This information is used later by the Data Merge Sequencer.

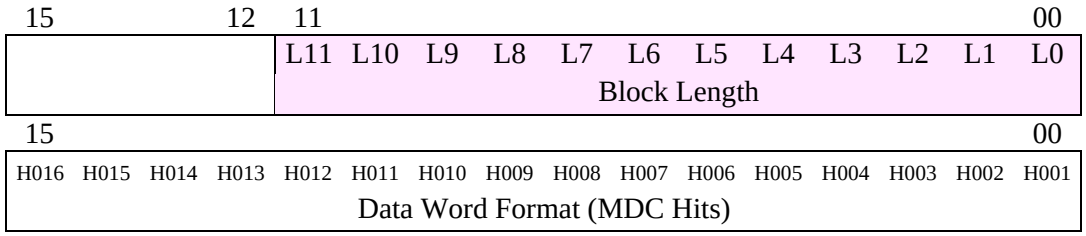
The Data Merge Sequencer combines 4 Substreams into a single output stream, writes it in the Dual Port Memory, calculates number of output data words and assigns it as a header to the event. In the Sparse Mode all hits are sorted in the ascending order. Number of data words in event may vary from 0 to number of MDCs in the crate times 192, Table 1. In the Fixed Mode no sparsification and encoding is performed. Number of output words is constant and equals to number of MDCs in the crate times 12, Table **1.** Sparse Mode Data Format.

. Readout rate in this case is independent of the number of hits in MDCs and sustained at 80 Mbyte/sec (900 ns/MDC).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	00
				L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	L0
				Block Length											
15	14	13	12	11	10	9	8	07	06	05	04	03	02	01	00
	T2	T1	T0	M3	M2	M1	M0	C7	C6	C5	C4	C3	C2	C1	C0
	Drift Time			MDC #				Channel #							

	Block Length = 2
	Data Word 1
	Data Word 2
	Block Length = 4
	Data Word 1
	Data Word 2
	Data Word 3
	Data Word 4
	Block Length = 5
	Data Word 1
	Data Word 2
	Data Word 3
	Data Word 4
	Data Word 5

Table 1. Sparse Mode Data Format.



	Block Length = (n x 12)
	Data Word 1 (MDC1 channels 016-001)
	Data Word 2 (MDC1 channels 032-017)
	Data Word 3 (MDC1 channels 048-033)
	Data Word 4 (MDC1 channels 064-049)
	Data Word 5 (MDC1 channels 080-065)
	Data Word 6 (MDC1 channels 096-081)
	Data Word 7 (MDC1 channels 112-097)
	Data Word 8 (MDC1 channels 128-113)
	Data Word 9 (MDC1 channels 144-129)
	Data Word 10 (MDC1 channels 160-145)
	Data Word 11 (MDC1 channels 176-161)
	Data Word 12 (MDC1 channels 192-177)
	Data Word 13 (MDC2 channels 016-001)
	Data Word 14 (MDC2 channels 032-017)
	Data Word 15 (MDC2 channels 048-033)
	Data Word 16 (MDC2 channels 064-049)
	Data Word 17 (MDC2 channels 080-065)
	Data Word 18 (MDC2 channels 096-081)
	Data Word 19 (MDC2 channels 112-097)
	…
	…
	…
	Data Word (n x 12) (MDCn channels 192-177)

Table 2 Fixed Mode Data Format

5. Synchronization

6. DSP

7. Serial Data Links

8. VME Interface

References

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[1] R. Janyanti, K. Johns, et al. The D0 Muon System Upgrade. D0 Note 2780, February 1996.

[2] G. Alexeev, B. Baldin, D. Denisov, S. Hansen, V. Tokmenin. On-Chamber Electronics for Muon Iarocci Mini-Drift Tubes (Technical Specification). D0 Note 2870, 04/02/96.

[3] B.Baldin, D.Denisov, V.Golovtsov, S.Hansen, P.Neustroev, L.Uvarov. Mini-Drift Tube Digitizing Card Specification. D0 Note 2988, 06/10/97.

[4] S.Hansen. Muon System Accelerator Timing Signal Transmission, 04/17/97.

[5] B. Baldin, S. Hansen. Proposed timing scheme for D0 detectors in RUN II. D0 Note 2705, 07/07/1995.