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MIL1553B_spec2.doc

MDRC MIL-1553B INTERFACE

Revision 2.0

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PRELIMINARY

I. MIL-1553B FORMATS

The following transfer formats are implemented in the MDRC MIL-1553B interface:

- Controller to RT transfer (receive or write)
- RT to Controller transfer (transmit or read)
- Mode command without data word

II. MIL-1553B RECEIVE/TRANSMIT COMMANDS

Sub-address (hex)	Description	Type	Word count	DPM Address, Block size (hex)
1	MDC, CSR0 – Pipeline Delay Register	R/W	15	0x020, 20
2	MDC, CSR0 – Gate Width Register	R/W	15	0x040, 20
3	MDC, CSR5 – Gate Delay Register	R/W	15	0x060, 20
4	MDC1, CSR2 – Channel Enable Register	R/W	12	0x080, 20
5	MDC2, CSR2 – Channel Enable Register	R/W	12	0x0A0, 20
6	MDC3, CSR2 – Channel Enable Register	R/W	12	0x0C0, 20
7	MDC4, CSR2 – Channel Enable Register	R/W	12	0x0E0, 20
8	MDC5, CSR2 – Channel Enable Register	R/W	12	0x100, 20
9	MDC6, CSR2 – Channel Enable Register	R/W	12	0x120, 20
A	MDC7, CSR2 – Channel Enable Register	R/W	12	0x140, 20
B	MDC8, CSR2 – Channel Enable Register	R/W	12	0x160, 20
C	MDC9, CSR2 – Channel Enable Register	R/W	12	0x180, 20
D	MDC10, CSR2 – Channel Enable Register	R/W	12	0x1A0, 20
E	MDC11, CSR2 – Channel Enable Register	R/W	12	0x1C0, 20
F	MDC12, CSR2 – Channel Enable Register	R/W	12	0x1E0, 20
10	MDC13, CSR2 – Channel Enable Register	R/W	12	0x200, 20
11	MDC14, CSR2 – Channel Enable Register	R/W	12	0x220, 20
12	MDC15, CSR2 – Channel Enable Register	R/W	12	0x240, 20
13	MDC, CSR4 – Test Delay & Test Type Register	R/W	15	0x260, 20
14	MDC, CSR5 – Test & OR Enable Register	R/W	15	0x280, 20
15	MDC, CSR6 – Discriminator Level Register	W	15	0x2A0, 20
16	MDC, CSR7 – Test Pulse Level Register	W	15	0x2C0, 20

17	MDRC – Power Supply & Temperature Monitor	R	6	0x2E0, 20
18	VME Processor –Download Status MDRC – Readout Errors and Status MDC, CSR3 – Error and ADB Status Register	R	1 + 1(2) + 15	0x300, 20
19	MDRC Registers	R/W	32 max	0x320, 20
1A	1553B <-> VME Processor Mail Box	R/W	32 max	0x340, 20
1B	Reserved	R/W	32 max	0x360, 20
1C	Multi-block Mode with Plane Alignment Constants (2 triplets) Alignment constant set ID Calibration constant set ID Tube 001…360 Logical Addresses	R/W	any size 8+ 1+ 1+ 360	0x400, C00
1D	Multi-block Mode for Data Monitoring	R	any size	0x400, C00
1E	Reserved	R/W	32 max	0x3C0, 20

III. MIL-1553B MODE COMMANDS (SUBADDRESS 0)

T/R Bit	Mode Code	Function
1	00001	Reset Multi-block Pointer
1	00100	DSP Reset
1	01000	VME SYSRESET

PRELIMINARY