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Mdc_spec.doc
D0 Note 2988

MINI-DRIFT TUBE DIGITIZING CARD SPECIFICATION

Revision 1.0

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1. Introduction

The Mini-drift tube Digitizing Card (MDC) is a part of the D0 Muon Mini-Drift Tube Chamber Electronics[1]. The Mini-Drift Tube (MDT) Chamber Electronics includes on-chamber Amplifier-Discriminator Boards (ADB)[2] , MDC and Mini-Drift Tube Readout Controller (MDRC). The MDC and MDRC are housed in 9U VME crates located on the detector platform. The primary functions of the MDC modules are Level 1 trigger hit bit generation and coarse time measurements of the drift time within the specified gate width. The design of the MDC implements the following features:

- reception of 192 discriminator signals from the Amplifier-Discriminator Boards;
- digitization of the arrival time of the input signals within a preset gate interval;
- transmission of the latched hit bits to the Level 1 trigger system via high speed serial links;
- fixed event output data format as nine 64-bit words;
- two analog control signals, Discriminator Level and Test Pulse Level, to control on-chamber electronics;
- test signal to fire the ADB's on-board pulser;
- programmable test signal for internal testing;
- mask register for 192 channels to provide selective channel enables;
- front panel 192-channel OR output with an LED indicator for debugging and self-triggering;
- three front panel LEDs to indicate VME access, MDRC readout access and Power OK.

2. Mechanical Specification

The MDT Chamber Electronics is based on VME 9U crates widely used in D0. It is assumed that each MDT crate constitutes a stand-alone readout station within the D0 detector and therefore has to have an individual AC outlet available on the platform. The MDC is implemented as 9U by 280 mm VME card, Fig. 6. The MDC uses three backplane connectors (see 10.3, 10.4, 10.5) for the following functions:

- **J1/J2** connections for standard VME operations
- custom **J3** connections for fast 64-bit wide data readout and for timing & control signals.

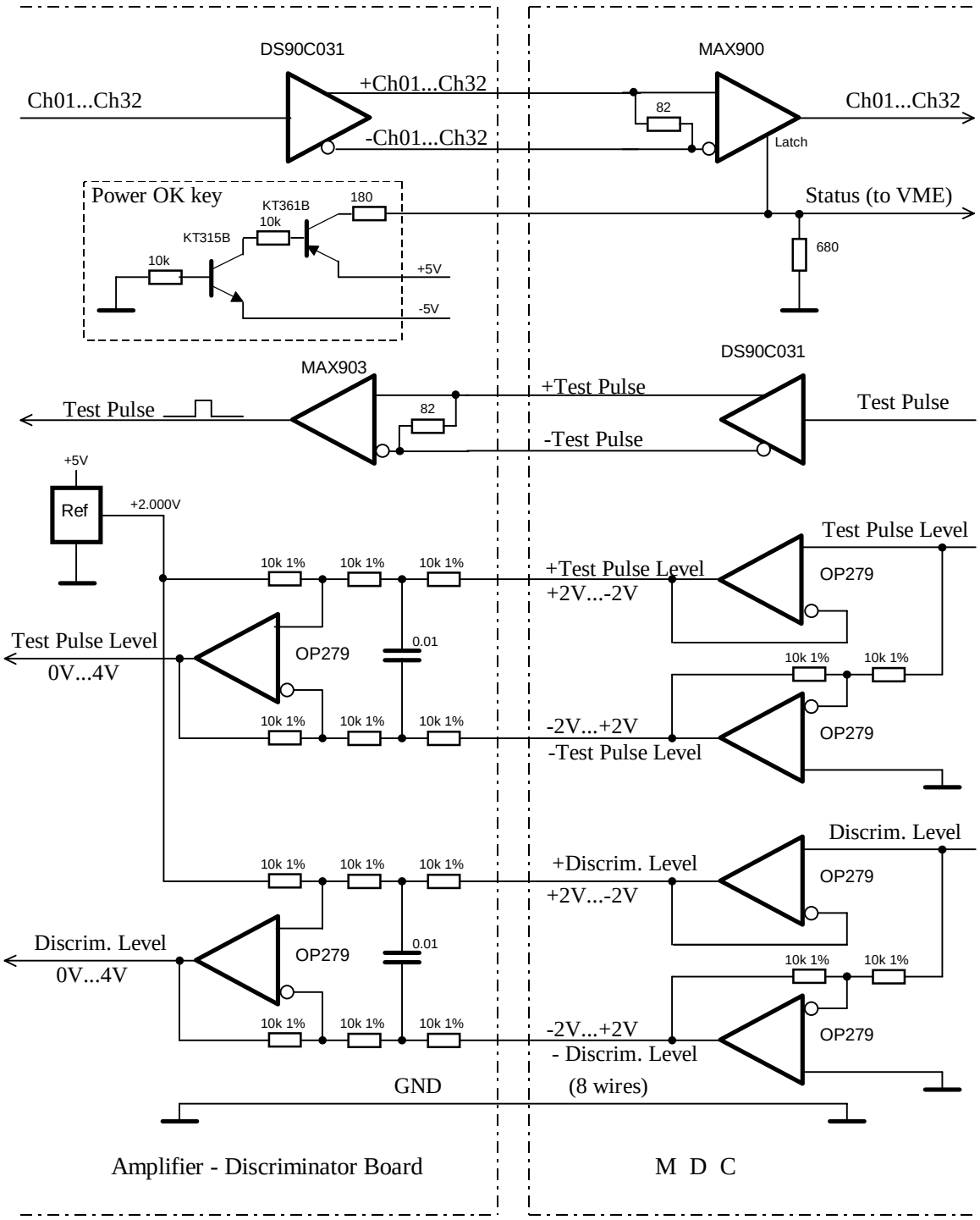


Fig. 1 ADB - MDC connection

There are six 80 pin high density connectors located on the front edge of the MDC to provide connections for the Amplifier-Discriminator Boards (32 channels per connector). Two HF connectors carry out two high-speed serial links emerging from Serial Transmitter Daughter Boards[3] (STDB) designed by Arizona University. An OR output signal uses a LEMO connector

with associated LED indicator. Three more LEDs indicate VME and MDRC readout access to the module as well as Power OK status.

3. ADB/MDC Interconnection

The Amplifier-Discriminator Board transmits data signals using the National DS90C031 LVDS - Low Voltage Differential current line drivers with a +/- 330mV swing . A High density 0.025" pitch 80 conductor cable is used to deliver signals from the ADB to the MDC. Cable pin assignment is shown in Table 3, Section 10.1, and Fig. 1 gives an example of the ADB/MDC connection. It is assumed that all signals on all six cables arrive with equal delays, hence there is no need for individual channel-by-channel delay adjustment within the MDC. Each differential line is terminated with a single 82 Ohm resistor. The MAX900 comparator translates the input differential signal into the TTL level. To prevent oscillations, additional wire brings a TTL level to the latch input of the comparator. When the input cable is disconnected or the ADB power supply is turned off, the output of the comparator is latched making a circuit quiet. In addition two analog differential signals and one logical differential signal are sent to the ADB to control the discriminator thresholds and test pulser.

4. Other Output Signals

Each MDC module uses two STDBs to provide hit information to the Level 1 trigger system. The STDB is arranged as a separate daughter board and has a parallel 16-bit input and HF output coaxial connector. The daughter board is synchronized to the accelerator RF (53 MHz) and is capable to transfer 96 bits of information during a 132 ns interval. A Level 1 trigger bit data format is shown in Table 4.

The front panel Fast OR output provides an OR from all 192 channels, Fig. 4. The Fast OR signal available on the J3 backplane also. Each output pulse is accompanied by a 20 ms flash of the LED indicator. The primary purpose of the output is to provide a simple tool for testing and debugging as well as a signal source for local triggering.

5. Signal Processing

The MDC module is designed to run synchronously with accelerator RF clock frequency of 53.104 MHz. The MDRC receives encoded timing signals from the Geographic Sector (GS), decodes it, and fanouts to the MDCs. Timing signals include RF, First Crossing (FC) and Synchro Gap (SGap). The FC signal marks a bunch crossing in the detector as a relative bunch crossing number one, while SGap controls the transmission of data to the L1 trigger. In fact, the MDRC drives the MDC with a RF/7 reference frequency and the MDC recovers the RF clock of 53.104MHz using the AMCC S4503 Clock Synthesizer circuit. All the rest of the necessary control signals are generated locally, Fig. 2.

All signal processing functions are implemented in the Cypress FPGA CY7C385A IC. Each IC consists of 24 individual channels, Fig. 3. The MDC accepts asynchronous discriminator signals from the ADB and stores them in the input D-type trigger (Trigger Hit) in coincidence with the Gate and Enable signals. The Gate signal is common for all channels of the MDC**.** The Enable signal is individual mask bit for each channel and can be downloaded (10.6). The stored bits are then reloaded into the Serial Link Shift Register and shifted outside the FPGA chip to the Serial Link Daughter Board at the RF clock frequency.

When the Trigger Hit is asserted, the current value of the Drift Time bus is loaded to the Pipeline Register. At the end of the Gate signal the Drift Time value, saved in the Pipeline Register, is reloaded to the Output Shift Register and shifted outside of the FPGA to the Pipeline

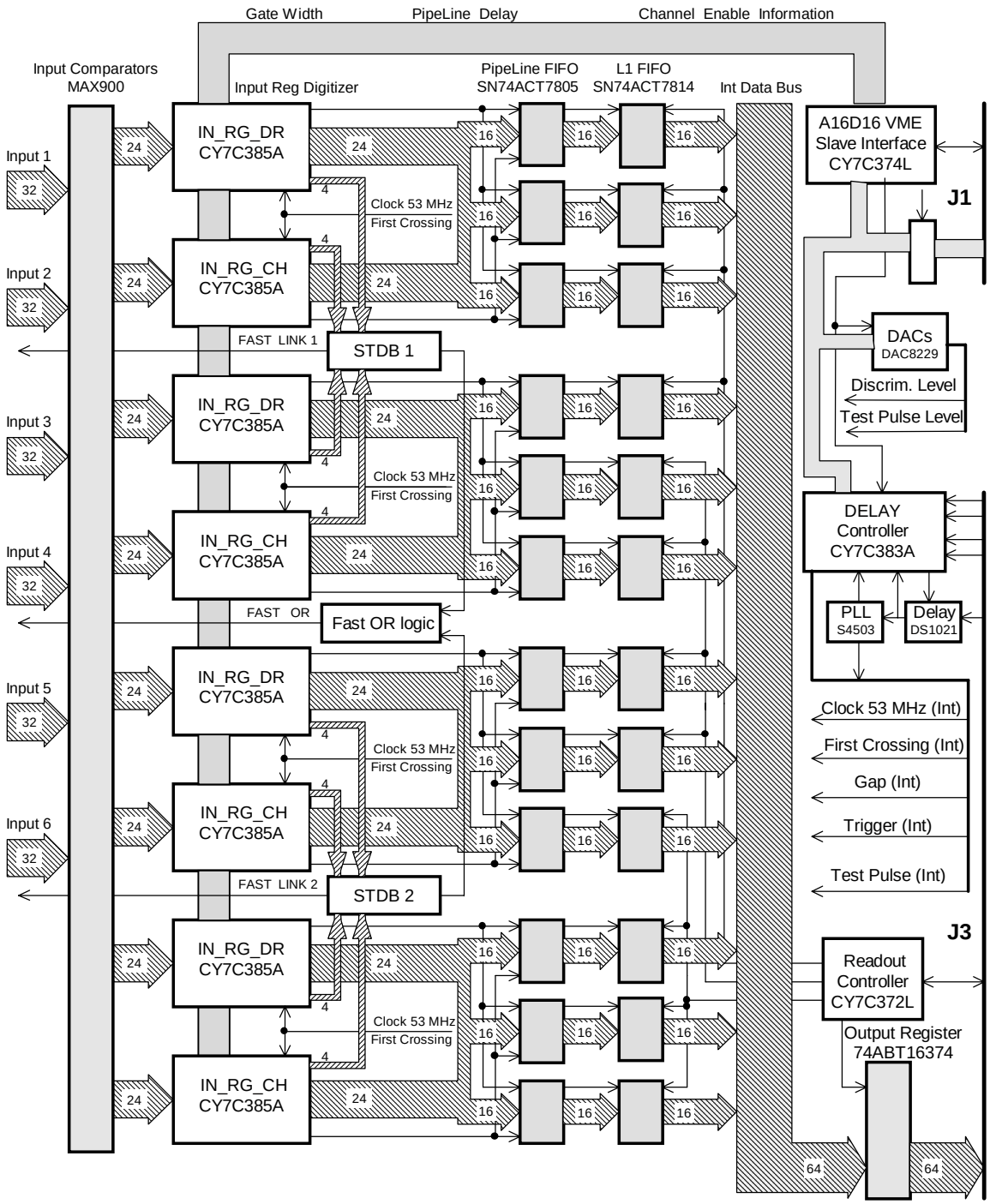


Fig. 2 MDC block diagram

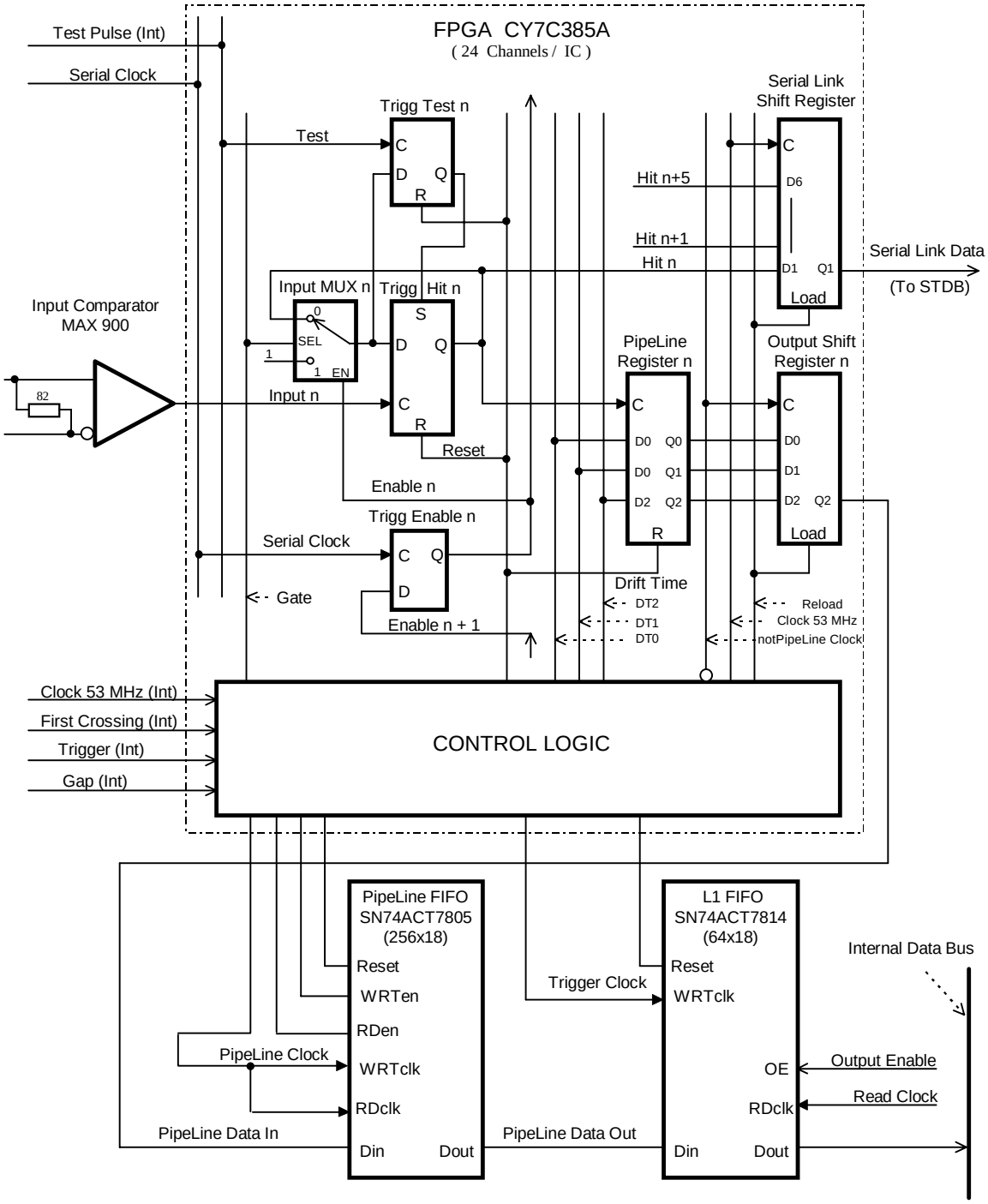


Fig. 3 MDC data channel diagram

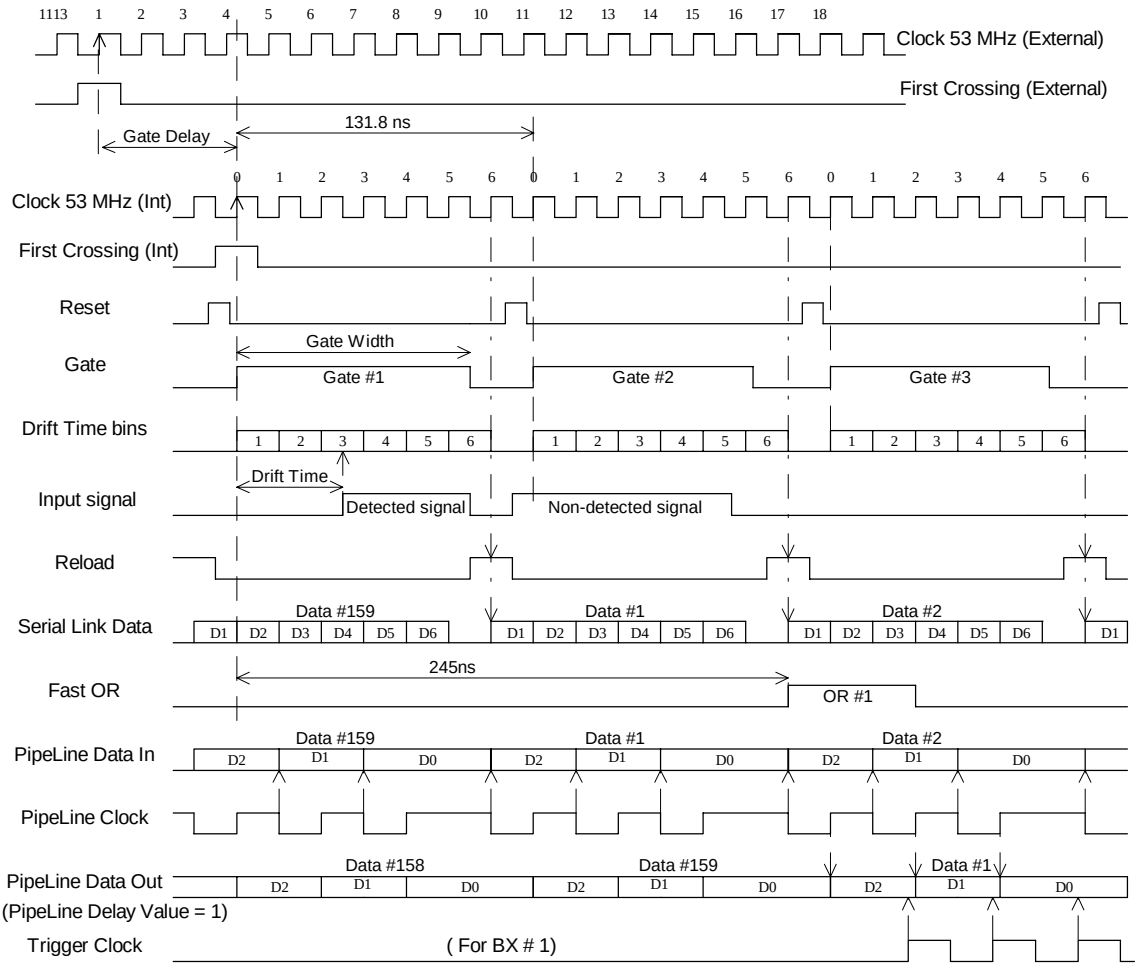


Fig. 4 MDC timing diagram

FIFO. If the Trigger Hit has not been asserted during the gate period, a zero value is stored in the pipeline. If the Trigger Hit was asserted, a corresponding drift time value (1..6) is stored in the pipeline. Gray code is used to eliminate drift time encoding errors. A simplified MDC timing diagram is shown in Fig. 4.[4]

The Pipeline FIFO is used to delay incoming data stream for a fixed period of time, until a corresponding L1 Accept signal is received (about 4.2μs). The Pipeline FIFO is based on a standard clocked Texas Instrument FIFO (SN74ACT7805, 256 x 18 bit). All control signals are generated by the same FPGA IC. The Pipeline Delay (PD) value is programmable (10.6) and has to be downloaded during the initialization procedure.

When an L1 Accept signal arrives, the corresponding data is supposed to be present at the pipeline output. The FPGA generates a Trigger Clock signal to reload data to the L1 FIFO. The data saved in the L1 FIFO is ready to be read out by the Readout Controller. Data path is deadtimeless, as next L1 Accept can be accepted immediately and next data block will be saved in the L1 FIFO. Maximum storage capacity of the FIFO is 21 events. L1 FIFO is based on a standard strobed Texas Instrument FIFO (SN74ACT7814, 64 x 18 bit).

6. Data Readout Interface

A simple pipeline interface is used for data transmission to Readout Controller card. The data is transferred via a 64-bit wide Data Bus at a 10 MHz clock speed which yields 80 Mbytes/s transmission rate, Fig. 5. This assures 100ns * 9 = 900 ns readout time per MDC. Each MDC module is addressable individually using a 4-bit readout Address Bus. (Low-scale part of the VME address DIP switch is used to select up to 15 MDCs per crate.)

Data Readout Interface uses J3 connections and is based on Texas Instruments TTL data transceivers (SN74ABT16374A, SN75ABT16821).

Timing and control signals occupy several lines of the same J3 connector (10.5).

Readout Interface pin assignment is shown in Table 7.

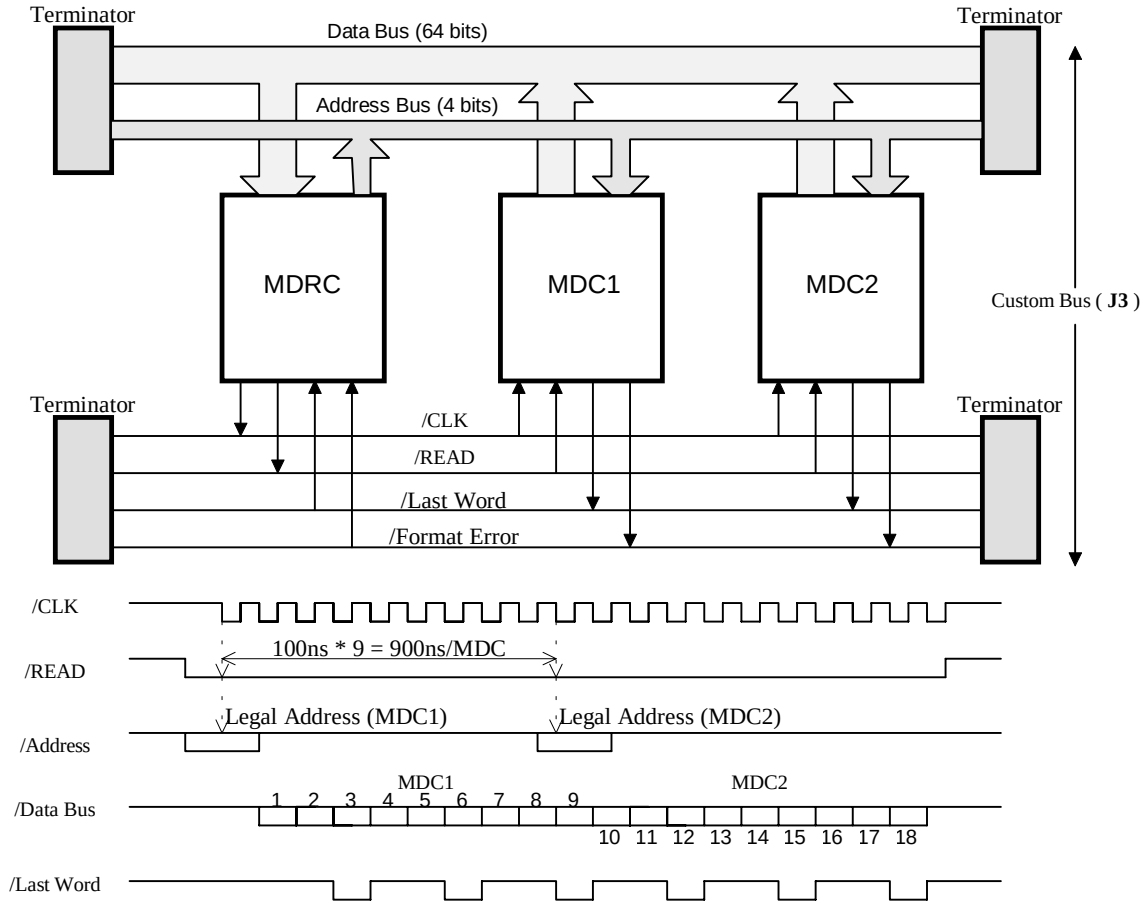


Fig. 5 MDC Data Readout Interface & Timing

Data readout interface output data format is shown below: Table 1

Data Lines: D_xx	64	63	62	61	-		-	02	01
Channel number	064	063	062	061	-		-	002	001
Word 1	D2	D2	D2	D2	-		-	D2	D2
Word 2	D1	D1	D1	D1	-		-	D1	D1
Word 3	D0	D0	D0	D0	-		-	D0	D0
Channel number	128	127	126	125	-		-	066	065
Word 4	D2	D2	D2	D2	-		-	D2	D2
Word 5	D1	D1	D1	D1	-		-	D1	D1
Word 6	D0	D0	D0	D0	-		-	D0	D0
Channel number	192	191	190	189	-		-	130	129
Word 7	D2	D2	D2	D2	-		-	D2	D2
Word 8	D1	D1	D1	D1	-		-	D1	D1
Word 9	D0	D0	D0	D0	-		-	D0	D0

D2, D1, D0 - encoded drift time. Gray code is used: **Table 2**

D2	D1	D0	Time bin
0	0	0	No Hit
0	0	1	Bin 1
0	1	1	Bin 2
0	1	0	Bin 3
1	1	0	Bin 4
1	0	0	Bin 5
1	0	1	Bin 6
1	1	1	Illegal

7. VME Interface

The main purpose of the VME interface is to provide downloading and reading back control and status information. The digitized hit information is unavailable for reading via VME interface and can only be read out by the MDRC. The MDC uses a standard Short I/O A16:D16 Slave Interface. Eight-bit DIP switch allows to select A05..A12 address lines and thus the address space for the particular card. The remaining most significant bits of the address (A13..A15) should be set to zero. One MDC uses 16 contiguous addresses in the address space. The description of the control and status registers is shown in Table 8. Only eight of sixteen addresses are actually used in the current design. The remaining addresses are reserved for future expansion.

VME interface pin assignment is shown in Table 5 and Table 6.

8. MDC Design Parameters [†]

8.1 Input connectors:

Six 80-pin high density connectors,
32 ADB channels per connector
192 differential inputs terminated with 82 Ohm resistors

Minimum differential input voltage	-	100 mV
Nominal differential input voltage	-	250 mV
Minimum input signal width	-	10 ns
Differential Discriminator Level output voltage (8-bit DAC used)	-	-4.0V..+4.0 V / 10 kOhm
Differential Test Pulse Level output voltage (8-bit DAC used)	-	-4.0V..+4.0 V / 10 kOhm
Differential logic Test Pulse (current driver)	-	±3.4 mA

8.2 Output connectors:

Two HF connectors for high speed serial links
Fast OR output with NIM level signal (16mA/50 Ohms)

8.3 Indicators:

Red LED ,	20 ms flash per Fast OR pulse
Green LED	MDC Power OK
Yellow LED	VME access
Yellow LED	MDRC access

8.4 Timing signals:

Reference clock RF/7 (supplied by the MDRC)	-	7.58628 MHz
Internal RF clock frequency (recovered in the MDC)	-	53.103 MHz
Gate Width range (GW) GW = 5 + N*9.41 ns, N=0..10	-	5..100 ns
Gate Delay range (GD) GD=N * 1 ns, N=0..63	-	0..63 ns
Drift time measurement bin width	-	18.83 ns
PipeLine Delay range (PD) PD=N*0.132 μs, N=1..63	-	0.13..8.3 us
Test Pulse Fine Delay range -(TF) TF=N*1 ns, N=0..63	-	0..63 ns
Test Pulse Coarse Delay range (TC) TC=N*18.83 ns, N=0..15	-	0..282.4 ns

[†] *Note: All parameters are subject to change after MDC prototype testing*

9. References

[1] R. Janyanti, K. Johns, et al. The D0 Muon System Upgrade. D0 Note 2780, February 1996.

[2] G. Alexeev, B. Baldin, D. Denisov, S. Hansen, V. Tokmenin. On-Chamber Electronics for Muon Iarocci Mini-Drift Tubes (Technical Specification). D0 Note 2870, 04/02/96.

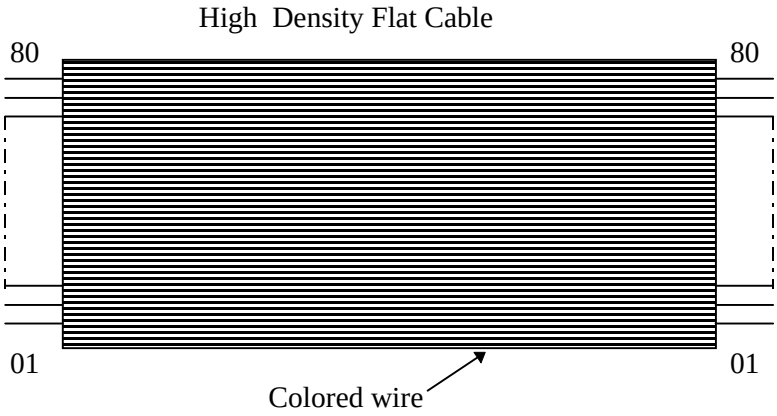
[3] Joel Steinberg. I/O Specification for Serial Transmitter Daughter Board (PCB-0140-XMIT). June 6, 1996.

[4] B. Baldin, S. Hansen. Proposed timing scheme for D0 detectors in RUN II. D0 Note 2705, 07/07/1995.

10. Appendixes

10.1 High Density Flat Cable Wire Assignment

Table 3



80	GND	60	+D09	40	+D19	20	+D29
79	GND	59	- D09	39	- D19	19	- D29
78	GND	58	+D10	38	+D20	18	+D30
77	GND	57	- D10	37	- D20	17	- D30
76	+D01	56	+D11	36	+D21	16	+D31
75	- D01	55	- D11	35	- D21	15	- D31
74	+D02	54	+D12	34	+D22	14	+D32
73	- D02	53	- D12	33	- D22	13	- D32
72	+D03	52	+D13	32	+D23	12	GND
71	- D03	51	- D13	31	- D23	11	GND
70	+D04	50	+D14	30	+D24	10	Status
69	- D04	49	- D14	29	- D24	09	Unassigned
68	+D05	48	+D15	28	+D25	08	+Discrim Level
67	- D05	47	- D15	27	- D25	07	- Discrim Level
66	+D06	46	+D16	26	+D26	06	+Test Pulse Level
65	- D06	45	- D16	25	- D26	05	- Test Pulse Level
64	+D07	44	+D17	24	+D27	04	+Test Pulse
63	- D07	43	- D17	23	- D27	03	- Test Pulse
62	+D08	42	+D18	22	+D28	02	GND
61	- D08	41	- D18	21	- D28	01	GND

10.2 Level 1 Trigger Bit Assignment

Table 4

SERIAL LINK #1

Data bits:

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
word 1	091	085	079	073	067	061	055	049	043	037	031	025	019	013	007	001
word 2	092	086	080	074	068	062	056	050	044	038	032	026	020	014	008	002
word 3	093	087	081	075	069	063	057	051	045	039	033	027	021	015	009	003
word 4	094	088	082	076	070	064	058	052	046	040	034	028	022	016	010	004
word 5	095	089	083	077	071	065	059	053	047	041	035	029	023	017	011	005
word 6	096	090	084	078	072	066	060	054	048	042	036	030	024	018	012	006
	Input connector #3 Channels 065...096						Input connector #2 Channels 033...064					Input connector #1 Channels 001...032				

SERIAL LINK #2

Data bits:

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
word 1	187	181	175	169	163	157	151	145	139	133	127	121	115	109	103	097
word 2	188	182	176	170	164	158	152	146	140	134	128	122	116	110	104	098
word 3	189	183	177	171	165	159	153	147	141	135	129	123	117	111	105	099
word 4	190	184	178	172	166	160	154	148	142	136	130	124	118	112	106	100
word 5	191	185	179	173	167	161	155	149	143	137	131	125	119	113	107	101
word 6	192	186	180	174	168	162	156	150	144	138	132	126	120	114	108	102
	Input connector #6 Channels 161...192						Input connector #5 Channels 129...160					Input connector #4 Channels 97...128				

10.3 J1 Pin Assignment

Table 5

Pin Number	Row A	Row B	Row C
01	D00	*BBSY**	D08
02	D01	*BCLR**	D09
03	D02	*ACFAIL**	D10
04	D03	*BG0IN**	D11
05	D04	*BG0OUT**	D12
06	D05	*BG1IN**	D13
07	D06	*BG1OUT**	D14
08	D07	*BG2IN**	D15
09	GND	*BG2OUT**	GND
10	*SYSCLK*	*BG3IN**	*SYSFAIL**
11	GND	*BG3OUT**	*BERR**
12	DS1*	*BR0**	SYSRESET*
13	DS0*	*BR1**	*LWORD**
14	WRITE*	*BR2**	AM5
15	GND	*BR3**	*A23*
16	DTACK*	AM0	*A22*
17	GND	AM1	*A21*
18	*AS**	*AM2*	*A20*
19	GND	AM3	*A19*
20	IACK*	GND	*A18*
21	*IACKIN**	*SERCLK*	*A17*
22	*IACKOUT**	*SERDAT**	*A16*
23	AM4	GND	A15
24	A07	*IRQ7**	A14
25	A06	*IRQ6**	A13
26	A05	*IRQ5**	A12
27	A04	*IRQ4**	A11
28	A03	*IRQ3**	A10
29	A02	*IRQ2**	A09
30	A01	*IRQ1**	A08
31	-12VDC	+5VDC	+12VDC
32	+5VDC	+5VDC	+5VDC

*BBSY** - not used signals

10.4 J2 Pin Assignment

Table 6

Pin Number	Row A	Row B	Row C
01	-	+5VDC	-
02	-	GND	-
03	-	*Reserved*	-
04	-	*A24*	-
05	-	*A25*	-
06	-	*A26*	-
07	-	*A27*	-
08	-	*A28*	-
09	-	*A29*	-
10	-	*A30*	-
11	-	*A31*	-
12	-	GND	-
13	-	+5VDC	-
14	-	*D16*	-
15	-	*D17*	-
16	-	*D18*	-
17	-	*D19*	-
18	-	*D20*	-
19	-	*D21*	-
20	-	*D22*	-
21	-	*D23*	-
22	-	GND	-
23	-	*D24*	-
24	-	*D25*	-
25	-	*D26*	-
26	-	*D27*	-
27	-	*D28*	-
28	-	*D29*	-
29	-	*D30*	-
30	-	*D31*	-
31	-	GND	-
32	-	+5VDC	-

A24 - not used signals

10.5 J3 Pin Assignment

Table 7

Pin Number	Row A	Row B	Row C
01	GND	GND	GND
02	F/7	/Data_cl	GND
03	GND	/Init	/First_cross
04	/Spare1	/GAP	GND
05	/L1_acc	/CLK	/Test
06	GND	/Fast_OR	/READ
07	/A0	/A1	/A2
08	/A3	/Last_Wd	/F_Err
09	/D_01	/D_02	/D_03
10	/D_04	/D_05	/D_06
11	GND	/D_07	/D_08
12	/D_09	/D_10	/D_11
13	/D_12	/D_13	/D_14
14	/D_15	/D_16	/D_17
15	/D_18	/D_19	/D_20
16	GND	/D_21	/D_22
17	/D_23	/D_24	/D_25
18	/D_26	/D_27	/D_28
19	/D_29	/D_30	/D_31
20	/D_32	/D_33	/D_34
21	GND	/D_35	/D_36
22	/D_37	/D_38	/D_39
23	/D_40	/D_41	/D_42
24	/D_43	/D_44	/D_45
25	/D_46	/D_47	/D_48
26	GND	/D_49	/D_50
27	/D_51	/D_52	/D_53
28	/D_54	/D_55	/D_56
29	/D_57	/D_58	/D_59
30	/D_60	/D_61	/D_62
31	GND	/D_63	/D_64
32	-5VDC	-5VDC	-5VDC

10.6 MDC VME Registers

Table 8

CSR0, Address 0XX0, Read/Write, Pipeline Delay and Gate Width Register,
unused bits read back as zeros

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
		PD5	PD4	PD3	PD2	PD1	PD0					GW3	GW2	GW1	GW0
		Pipeline Delay										Gate Width			

CSR1, Address 0XX1, Write only, Initialization Register
bits 0..15 read back as zeros

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
													IR3 Clear	IR2 Reset	IR1 Init

Clear, **Reset** and **Init** functions are performed by writing logical one to a corresponding bit.

Init - initializes Pipeline FIFO and L1 FIFO.
Must be issued after any access to the register CSR0;

Clear - initializes L1 FIFO;

Reset - loads following default values to the MDC registers:

PD	- Pipeline Delay	= 1
GW	- Gate Width	= 10
E001..E192		= 1
TE1..TE8		= 1
TF	- Test Fine Delay	= 0
TC	- Test Coarse Delay	= 0
GD	- Gate Delay	= 0
TT	- Test Type	= 0

CSR2, Address 0XX2, Read/Write, Channel Enable Register,
bits are accessible by twelve sequential reads or writes to the same address.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
E016	E015	E014	E013	E012	E011	E010	E009	E008	E007	E006	E005	E004	E003	E002	E001
E032	...														E017
E048	...														E033
⋮															⋮
E176	...														E161
E192	...														E177

CSR3, Address 0XX3, Read only, Error Status and ADB Status Register,
unused bits read back as zeros

15	14 11	10	09 06	05 00
ES Σ Err	PE4 PE3 PE2 PE1 Pipeline Error	IE InitE		AS6 AS5 AS4 AS3 AS2 AS1 ADB Status

ASx equals to "1" if a corresponding ADB is powered up and connected to the MDC.
ES - Error Status bit equals to a logical OR of the PE - Pipeline Error and IE - Init Error bits.

CSR4, Address 0XX4, Read/Write, Test Delay & Test Type Register,
unused bits read back as zeros

15 12	11 08	07	06	05 00
	TC3 TC2 TC1 TC0 Test Coarse Delay	TT Type		TF5 TF4 TF3 TF2 TF1 TF0 Test Fine Delay

TT - Test Type: TT=0 - Internal, TT=1 - External

CSR5, Address 0XX5, Read/Write, Gate Delay & Test Enable Register
unused bits read back as zeros

15 08	07	06	05 00
TE8 TE7 TE6 TE5 TE4 TE3 TE2 TE1 Test Enable			GD5 GD4 GD3 GD2 GD1 GD0 Gate Delay

Test Enable bits control test signals depending on the status of the Test Type bit:

Test Type / Test Enable Bit	TT=0 (Internal)	TT=1 (External)
TE1	Ch001..Ch024	ADB1
TE2	Ch025..Ch048	ADB2
TE3	Ch049..Ch072	ADB3
TE4	Ch073..Ch096	ADB4
TE5	Ch097..Ch120	ADB5
TE6	Ch121..Ch144	ADB6
TE7	Ch145..Ch168	
TE8	Ch169..Ch192	

CSR6, Address 0XX6, Write only, Discriminator Level Register

15 08	07 00
	DL7 DL6 DL5 DL4 DL3 DL2 DL1 DL0 Discriminator Level

CSR7, Address 0XX7, Write only, Test Pulse Level Register

15 08	07 00
	TL7 TL6 TL5 TL4 TL3 TL2 TL1 TL0 Test Pulse Level

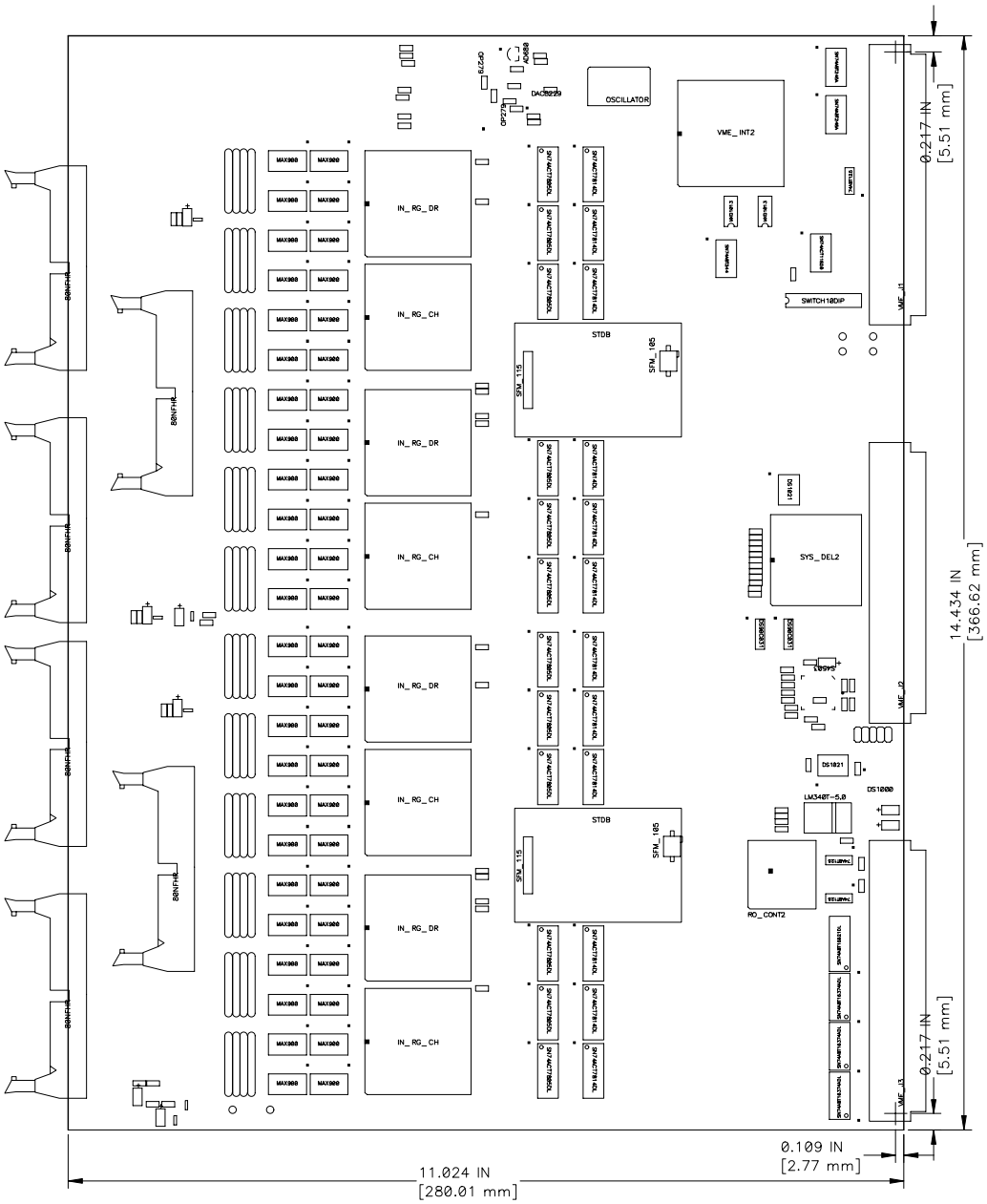


Fig. 6 PCB Layout of the MDC module.