

Suggestions for Level II Interrupt Logic

Dean Schamburger brought up the point during our last Muon Electronics review that it was theoretically possible to have as many as 15 L2 rejects that arrived at the rate of one per crossing. If there was a DSP interrupt for every L2 decision, this string of rejects would confuse the processor, since the L2 interrupt service routine takes a couple of microseconds to run. A possible solution would be to change the L2 interrupt logic. There is a register in the 21csp01 that selects level or edge sensitivity for each external interrupt. If all L2 decisions were written to a FIFO and the empty flag of that FIFO was connected to a level sensitive interrupt pin, then there would be no problem with a burst of L2 rejects. The processor would be re-interrupted as soon as one L2 decision had been handled. Since L1 interrupts have higher priority, the L2 service routine would be preempted when an L1 accept occurred. A diagram of the L2 interrupt logic is shown below:

L2 Interrupt Logic

