

D0 Muon Proportional Drift Tube Electronics Test Results¹

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Abstract

Test results of the Proportional Drift Tube (PDT) electronics for the Muon Upgrade at the D0 experiment at Fermilab are described. Prototypes of two front-end boards and two readout VME modules comprising a deadtimeless readout system have been built and tested. The front-end electronics prototypes include an eight-channel Front-End Board and a Control Board. The Front-End Board is capable of registering PDT anode wire signals with a 1 μ A threshold and two cathode pad charges at a resolution of 5 fC. Control Board features include a sequencer for collecting data from up to four Front-End Boards, two Digital Signal Processors (DSP), and two serial link transmitters. A serial link transports data a 100 meters from the Control Board to the VME based Muon Readout Card. The Muon Readout Card receives timing and control signals from the Muon Fanout Card and re-transmits them to the Control Board. Initial tests with internal pulsers simulating detector signals and further tests with cosmic rays are described. We have tested three data taking modes. The prototype readout system transfers PDT data without deadtime at 16 Mbyte/s with a Level 1 trigger rate of 10 kHz.

I. INTRODUCTION

The D0 Muon Proportional Drift Tube subsystem is a part of the Muon Upgrade project [1]. It includes 7000 PDT wires and twice that number of charge collecting pad electrodes implemented in 94 PDT chambers. The proposed design for the front-end and readout electronics is originally described elsewhere [2], [3]. In this article we describe some details of the PDT Electronics design and first results from prototype testing.

Several tests have been performed with electronics prototypes. After initial bench testing, the front-end boards were connected and raw data from the internal test pulsers were displayed on the terminal. This data were used to finally debug the readout interface and the firmware embedded in the Control Board. In the next step, the readout electronics were connected to the front-end boards, and another set of test pulser data was used to debug the next level of software. Finally, cosmic ray data were taken using different trigger sources, including an external scintillation counter trigger and internal software trigger.

II. SYSTEM ARCHITECTURE AND TESTS

A. PDT Electronics

The PDT front-end electronics includes Front-End Boards (FEB) and a Control Board (CB) mounted on the chamber. The Front-End Board tested was instrumented for eight cells on a full size (60 cm by 36 cm, 24 cell) printed circuit board. Each CB is interfaced with up to four FEBs depending on the PDT chamber type. The CB dimensions are approximately 60 cm by 18 cm. The Control Board reads out information from the FEBs and reformats and process it using one of two on-board DSPs. Processed data is transmitted via high speed serial links to the Level 2 trigger system and to the muon readout crate (Figure 1).

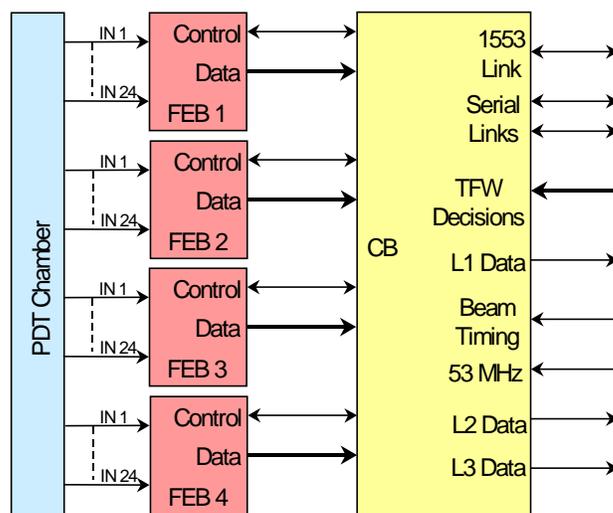


Figure 1: PDT Electronics block-diagram.

The front-end electronics are located in the D0 collision hall and mounted on the aluminum body of the PDT chamber. The connection between the front-end electronics and the Movable Counting House (MCH) is provided by four wide bandwidth coaxial cables, a 25 pair ribbon cable and a 1553 bus cable [4]. The maximum cable length is about 100 meters. Additional active peaking networks are implemented on both the coaxial and ribbon cables to compensate for signal attenuation.

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B. Front- End Board

The final version of the Front-End Board includes 24 Wire Amplifier/Discriminators and 48 Pad Amplifiers and Integrators. Depending on the number of PDT cells, 3 or 4 FEBs can be mounted on each PDT. All the wire discriminators on one FEB have a common threshold voltage controlled by the CB. There are also two test pulsers connected via a resistor network to the wire and pad amplifier inputs. The test pulsers generate signals with a fast rise time and an exponential decay time, approximating the wire and pad signals. The CB also controls the amplitude and timing of these signals. The FEB has a channel enable register, which allows the enabling or disabling of any wire channel on the board. Combined with the test pulsers, this feature allows for remote testing of most of the functions of the FEB. The FEB has six TDC ASICs (TMCTEG3) and 24 10-bit ADCs (ADC875) which continuously digitize the arrival times and induced pad charges whose results are stored in digital pipelines. The pipelines provide about 4 μ s delay for digitized data. That is the specified Level 1 trigger

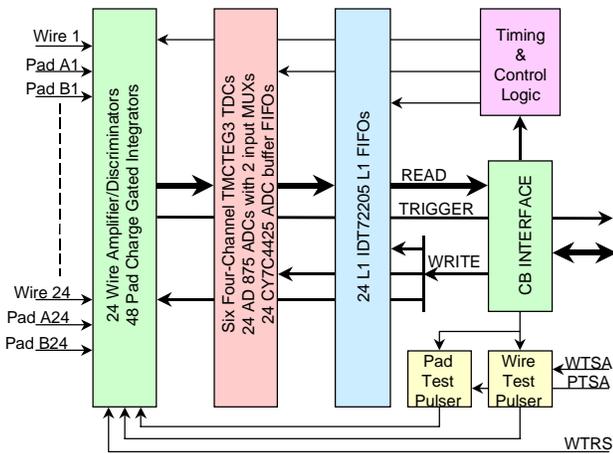


Figure 2: Front-End Board block-diagram.

decision time. If a trigger accept is generated, the appropriate portion of the time history from the pipelines is transferred to the Level 1 FIFOs. From there information is readout under control of the CB. The FEB also receives its timing signals via the CB interface.

C. Control Board

The Proportional Drift Tube (PDT) Control Board (CB) is connected to as many as four Front-End Boards (FEBs). It is the interface between these boards and the Muon Readout Card (MRC) and monitoring systems. A block diagram is shown in Figure 3. When in data taking mode, a new set of hit bits received from the FEBs is sent to the L1 trigger system every 132 ns by means of a 1 Gbit/s serial link mounted on a daughter board designed by Arizona University. In response

to an L1 accept trigger, data is read from the FEBs and stored in CB memory pending the outcome of an L2 decision. Data from each L1 accept is also processed and then transmitted on a 160 Mbit/s serial links to the L2 trigger system.

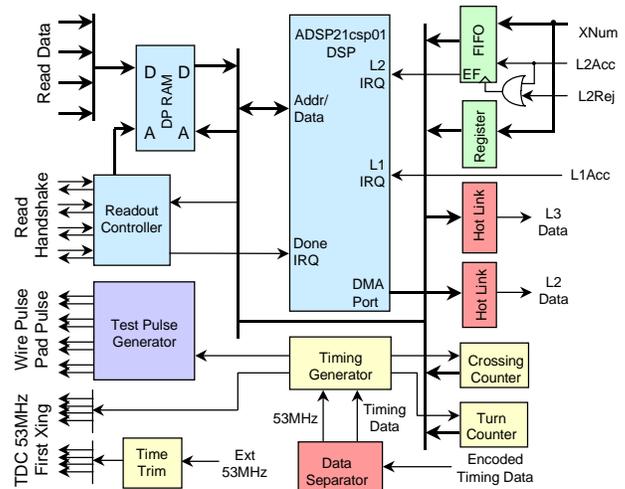


Figure 3: Control Board block-diagram (main data path).

An L2 accept initiates the transmission of an event (also on a 160 Mbit/s serial link) to the DAQ system in the Movable Counting House. An L2 Reject causes the data stored for that event to be discarded. An on-board timing generator can delay all the arriving timing signals a programmable amount as a means of synchronizing the operation of all FEBs in the muon system. For test pulsing, a programmable test pulse generator is fitted.

The board uses two DSP microprocessors, one as the data acquisition processor, the other as the control interface. This control processor handles the serial ports, 1553 interface, FEB control functions, the on board test pulse generator, the timing generator settings, DACs for setting test pulse amplitudes and wire discriminator thresholds, and a multi-channel ADC measuring power supply voltages and the PDT chamber differential gas pressure.

D. Readout Electronics

The readout electronics includes the Muon Readout Card (MRC) and Muon Fanout Card (MFC) prototypes [3]. Both modules are located in a muon readout crate (MCH) and controlled by an MVME162 Motorola embedded controller. The MVME162 also has an Ethernet interface, which allows access to a Unix host (See Figure 4). In the final version of the D0 DAQ system a VME Buffer Driver (VBD) module will also be used in this crate to provide D0 DAQ interface functions.

E. Levels of Testing

Four levels of testing are incorporated in the front-end and readout electronics, allowing data taking independent of the D0 DAQ. In each of the testing levels a trigger can be generated either by the internal test pulser or by logical OR of the wire discriminator signals. The following is a list of available test modes.

1) Front-end DSP level

The on-board DSP can run diagnostic sequences when it is not in data taking mode. These diagnostics can involve the pulsers, or self-triggering on noise or cosmics. The DSP can accumulate statistics on each channel and later pass the results up through the readout system. The RS-232 port can be used to display data on the terminal screen.

2) Muon readout crate VME processor level

VME processor in the crate could run programs to accumulate data from any of the MRC's. The RS-232 port on the VME processor can be connected to a terminal to provide a control interface and display results.

3) D0 host plus Ethernet interface level

The VME processor will still manage the accumulation of data, but instead of analyzing the data itself, it will pass it on through the Ethernet to the host computer for more sophisticated analysis and optional recording of events.

4) D0 host plus Trigger Fanout Card crate synchronization level (planned)

A deficiency of test triggering in Run I was the inability to coordinate the data taking from multiple muon crates without using the D0 DAQ system. A special Trigger Fanout Card (TFC) will be used to synchronize multiple crates. It distributes a specific sub-set of the D0 Trigger Framework (TFW) timing and control signals that can originate from any of the MFCs. This module must be connected to all the MFCs included in a particular local configuration.

5) Standard D0 DAQ level (planned)

Here, the triggers will be managed by the TFW and the data will be read out in the normal way through the VBD into the data cables. This requires the resources of essentially the whole D0 data acquisition system. This is the mode in which calibration was done in Run I.

F. Test Setup

After assembly, the FEB and CB were tested independently using their respective internal test features. The FEB has two on-board pulsers generating wire and pad simulated detector pulses. Both pulsers have independent control bits, but are triggered by the same external pulse supplied by the CB. They also have independent control of the test pulse amplitude supplied in the form of analog levels set

by the CB. The outputs of the pulsers are connected via a resistor network to each wire and pad amplifier respectively. There is a channel enable register on the FEB that allows a pre-selected number of channels to be triggered by the test pulse. Each wire discriminator on the FEB triggers the corresponding pad sequencer which stores the ADC information in the ADC pipeline delay [2]. Thus, individual testing of any channel is provided.

An intrinsic resolution obtained with internal FEB pulsers was at the level of 0.3 r.m.s. (1.2 ns TMC bin width) for the time measurements and about 1.5 r.m.s. (3 fC ADC bin width) for charge measurements.

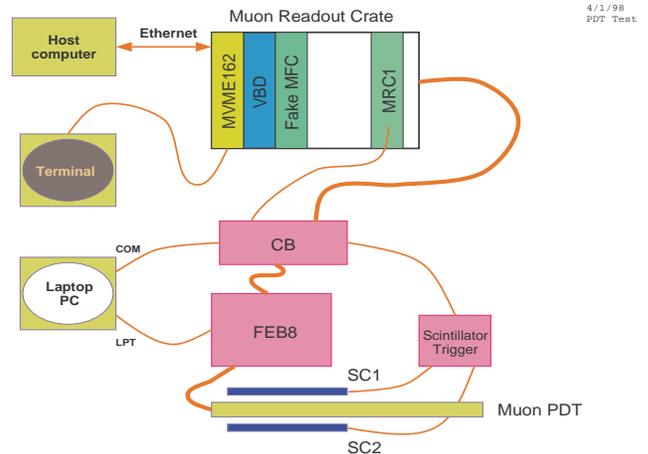


Figure 4: PDT comic ray test stand.

The Control Board includes two serial terminal interfaces. One interface is used to communicate to an on-board auxiliary DSP processor (ADSP-2111), which provides remote and local control of the CB's peripheral devices. Using a laptop PC serial port, the readout DSP and peripheral devices can be monitored and controlled a small resident debugger. The readout processor (ADSP-21csp01) does event data processing at different trigger levels. A Level 1 accept signal causes the readout DSP to retrieve data from the readout controller dual-port memory. The readout controller is triggered either by a Level 1 external trigger or internally by a trigger "OR" supplied from the FEB. It performs data driven readout from the FEB's Level 1 FIFO memories, which contain event data. After data is placed into FIFO, the readout DSP processor retrieves and formats it for Level 2 and Level 3 transfers [4]. It is possible to use a software trigger to analyze event data before data transfers. The processed and formatted data is sent to a serial transmitter (Cypress HOTLink CY7B923) and transferred at 16 Mbyte/s via a coaxial cable to the MRC. At this level data could be displayed by the VME processor on a terminal screen or stored in a file on the host machine.

G. Cosmic Ray Tests

A series of preliminary PDT Electronics tests with cosmic rays was performed using a six foot standard muon PDT filled

with fast gas mixture (Ar + 10%CH₄ + 10%CF₄). Prototypes of the Front-End Board, Control Board, Muon Readout Card and a hand wired minimally functioning Muon Fanout Card were used in the test setup (Figure 4). A Motorola MVME162 processor was used as a VME master in a muon readout crate to control the MRC and MFC modules and as an interface with a host Unix machine via Ethernet. Two scintillation counters SC1 and SC2 are used in coincidence to generate an external trigger signal. An eight-channel FEB prototype was connected to the PDT by twist-n-flat 34 wire 3M cables.

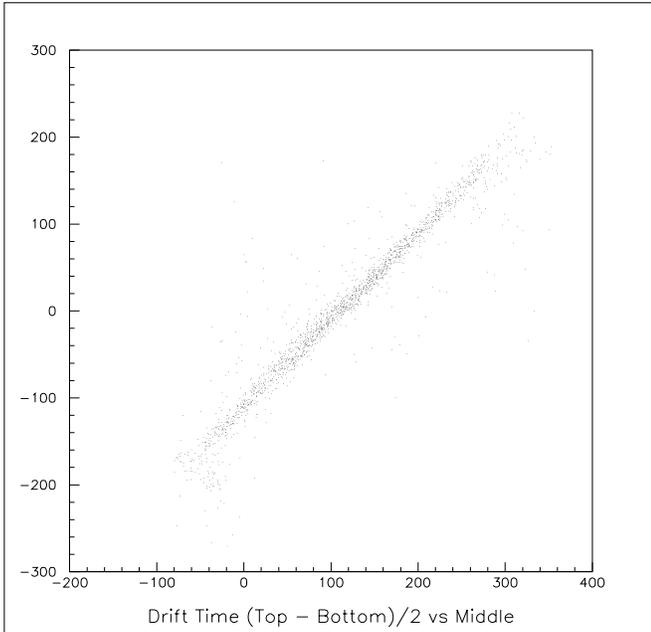


Figure 5: Drift time correlation.

The laptop PC also was used to download and communicate with the Control Board processors. The debugger program resident in the control DSP has a basic set of operations that includes downloading of Intel hex formatted object files. Terminal emulator software running on the laptop was used to send code for a startup routine over the RS-232 port of the CB that configures both the FEB and the appropriate registers of the CB when run. The startup routine is menu driven and allows user to initialize both boards and setup hardware parameters.

The readout processor software was implemented in a PROM. The code running the readout processor responds to requests by the auxiliary DSP thus enabling at least indirect control of both processors from the terminal port attached to the auxiliary DSP.

When triggered, a hardware sequencer reads wire and pad data and does an initial set of reformatting steps. For the time being, the readout processor copies this data unaltered to the serial link transmitter with the addition of beam orbit and crossing numbers and global word count. The HOTLink receiver in the MRC receives the data and stores it in a buffer memory. The MRC data buffer is read out by an MVME162 processor and is displayed in hex format on the terminal screen or stored in a file on the host.

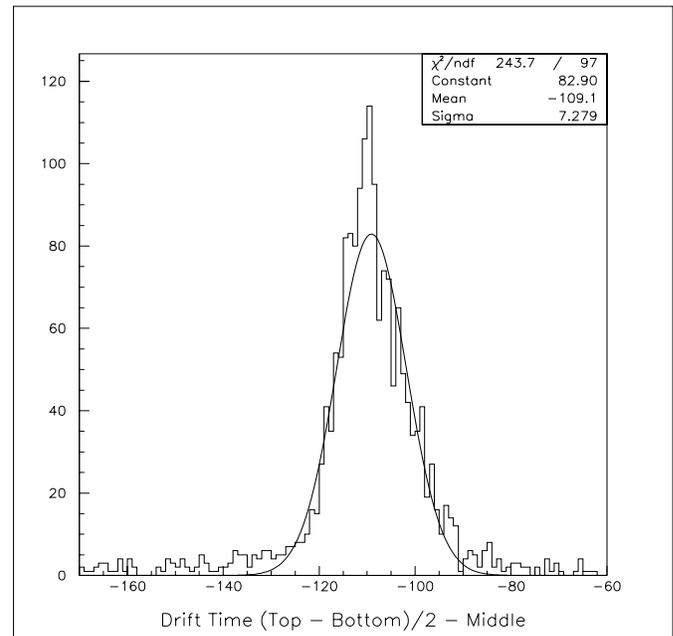


Figure 6: Drift time resolution projected from Figure 5.

A typical coincidence trigger rate for the scintillation counters of 20cm x 60cm size was about 10 Hz. Drift time and pad transfer gates were set to approximately 800 ns and 1500 ns respectively. The pipeline delay was adjusted to an arbitrary value of 1800 ns. The whole setup was carefully tested using the internal FEB test pulsers. A typical threshold value for cosmic ray measurements was about 1 μ A. Three types of measurements [5] have been made:

- 1) Drift time of track ionization perpendicular to the chamber wire
- 2) Transit time of the wire pulse longitudinally along the wire, and
- 3) Charge ratio of the induced pulses on the shaped cathode pads.

In order to measure the drift time resolution, the drift times in the top and bottom cells are combined and plotted versus the middle cell drift time. This procedure compensates for tracks at different angles. Figure 5 shows such a two-dimensional plot. A one-dimensional projection of this plot is shown in Figure 6. The calculated drift time resolution is about 7 ns, which corresponds to approximately 0.7 mm spatial resolution.

For the transit time measurements, a software trigger was generated at the CB using an “AND” of the three decks. The scintillation counters were not used in this case. In order to compensate for tracks at different angles, the top and bottom decks were combined and compared to the middle deck. Figure 7 shows the transition time scatter plot. Recall that the wires are connected at the “simple” end of each cell pair by a 20 ns delay. Figure 8 shows the transit time resolution, gotten by comparing the average of the top and bottom decks to the middle deck. The time resolution of about 1.5 ns corresponds

to a spatial resolution of approximately 20 cm. The transit time determines the tracks longitudinal position roughly;

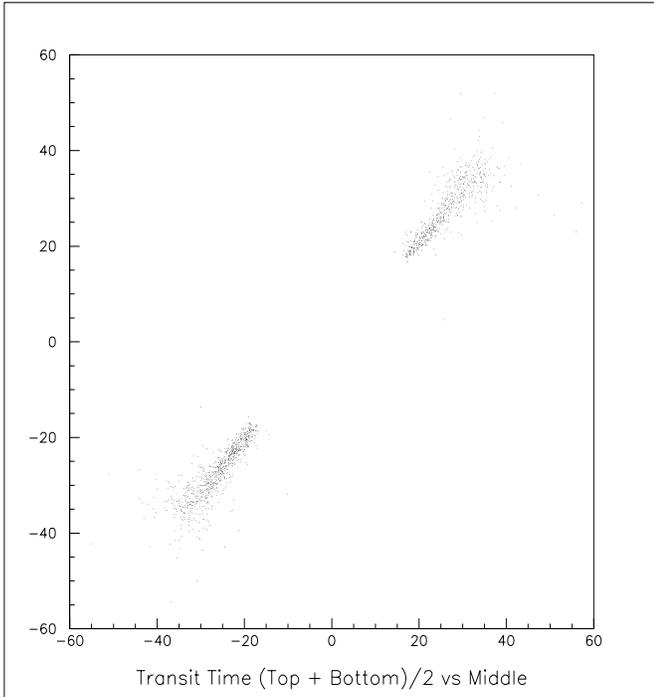


Figure 7: Transit time correlation.

the charge ratio of the signal induced on the cathode pads gives the fine position. Again, by comparing the sum of top and bottom signals to the middle signal, Figure 9 shows

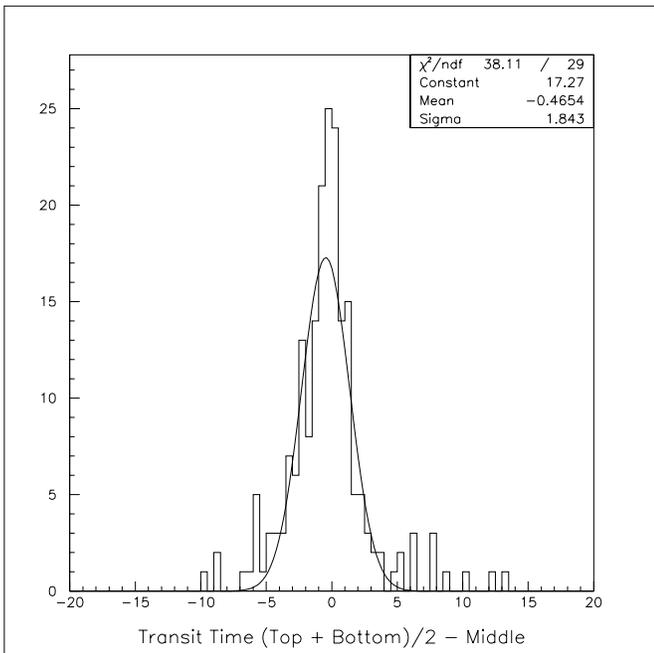


Figure 8: Transit time resolution projected from Figure 7.

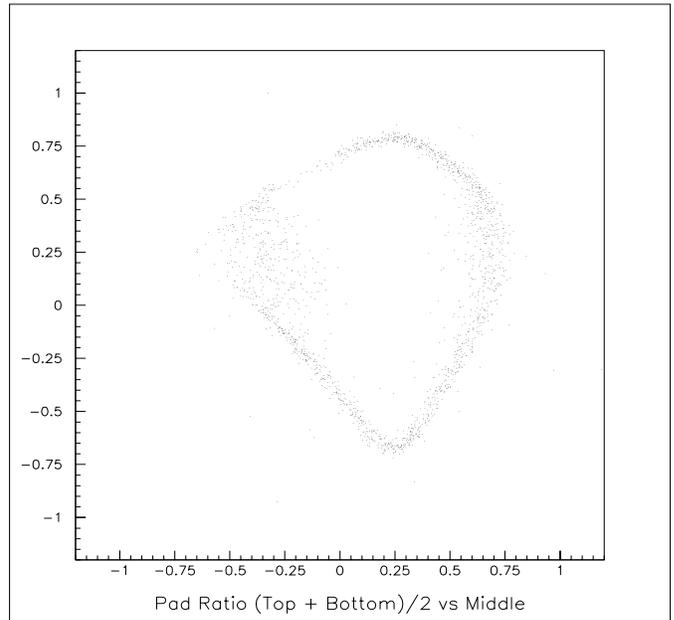


Figure 9: Pad ratio correlation.

scatter plot for charge pad ratios. Each ratio is defined by the following equation:

$$R = \frac{Q_a - Q_b}{Q_a + Q_b} \quad (1)$$

In the equation (1) Q_a and Q_b are the charges on the pads with the pedestals subtracted.

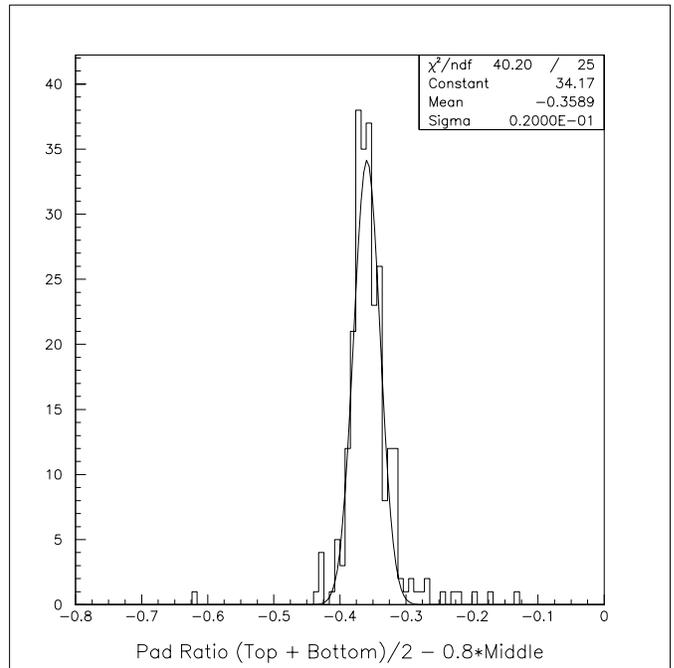


Figure 10: Pad resolution from selected projection of the plot in Figure 9.

Figure 10 shows the fine resolution obtained by selecting a segment of Figure 9 that is independent of the track angle. The pad resolution measured by this method is about 0.5 cm.

H. Conclusion

We conclude that the prototype PDT electronics generally complies with the original specification. It provides deadtimeless operations for trigger rates up to 10 kHz. Minor modifications and improvements are necessary before mass production of the PDT electronics begins.

III. REFERENCES

- [1] D0 Collaboration. "The D0 Upgrade. The detector and its physics," Fermilab preprint, FERMILAB-PUB-96-357-E, October 1996.
- [2] B.Baldin, et al. "D0 Upgrade Muon Electronics Design," *IEEE Trans. on Nuclear Science*, Vol.42, No.4, pp. 736-742, August 1995.
- [3] B.Baldin, et al. "D0 Muon Readout Electronics Design," *IEEE Trans. on Nuclear Science*, Vol.44, No.3, pp. 363-369, June 1997.
- [4] A.Khohlov et al., "Muon System Electronics Upgrade", Technical Design Report, D0 Note 3299, July 22, 1997.
- [5] D.Green et al., "Accurate 2 Dimensional Drift Tube Readout Using Time Division And Vernier Pads", *Nucl. Instr. & Meth.*, vol. A256, pp. 305-312, 1987.