

B.Baldin  
S.Hansen  
7/24/97

## PDT Front-End Board Specification

Front-End Board (FEB) is designed to process wire and pad signals generated by the WAMUS Proportional Drift Tubes (PDT) described earlier. The wire is a negative current source in the range of 0.5..50  $\mu\text{A}$ . The pad is a positive current source in a range of 0.2..20  $\mu\text{A}$ . The wire signals travel within the aluminum body of the PDT which with the wire constitutes a wave guide of about 330  $\Omega$  impedance. Two neighboring cells in one layer of the PDT have a lumped delay jumper connecting the two far ends of the wires. A signal originating at the near of one tube will take about 60 ns to propagate to the near end of the other (Fig. 1). Induced charge from the wire signal is collected on two pad electrodes with about 700 pF capacitance each.

Each cell has a service board to bring high voltage to the wire and pads and to pick up the signals. Single ended wire signals are converted to differential by a broadband coupling transformer. Each cell has two pad electrodes, A and B connected to the FEB separately. According to the current naming convention, pad electrode connected to the pin closest to the wire pin is pad B. Though arbitrary, this convention is used to distinguish the two pad signals.

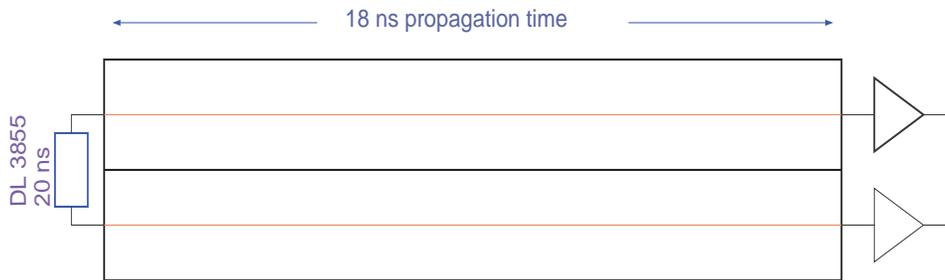


Fig. 1. PDT delay jumper.

A block diagram of the Front-End Board is shown in Fig. 2. Each board includes 24 Wire Amplifier/Discriminators and 48 Pad Amplifiers and Integrators. Depending on the number of PDT cells, 3 or 4 FEBs and one Control Board (CB) can be mounted on each PDT. All the wire discriminators on one FEB have a common threshold voltage controlled by the CB. There are also two test pulsers connected via a resistor network to the wire and pad amplifier inputs. The test pulsers generate exponential signals approximating the wire and pad signals. The amplitude and synchronization of these signals is also controlled by the CB. The FEB has a channel enable register which allows the enabling or disabling of any wire channel on the board. Combined with the test pulsers, this feature allows for remote testing of most of the functions of the FEB. The FEB has six TDC ASICs (TMCTEG3) and 24 10-bit ADCs (ADC875) which continuously digitize the arrival times and induced pad charges whose results are stored in digital pipelines. The digitized data is

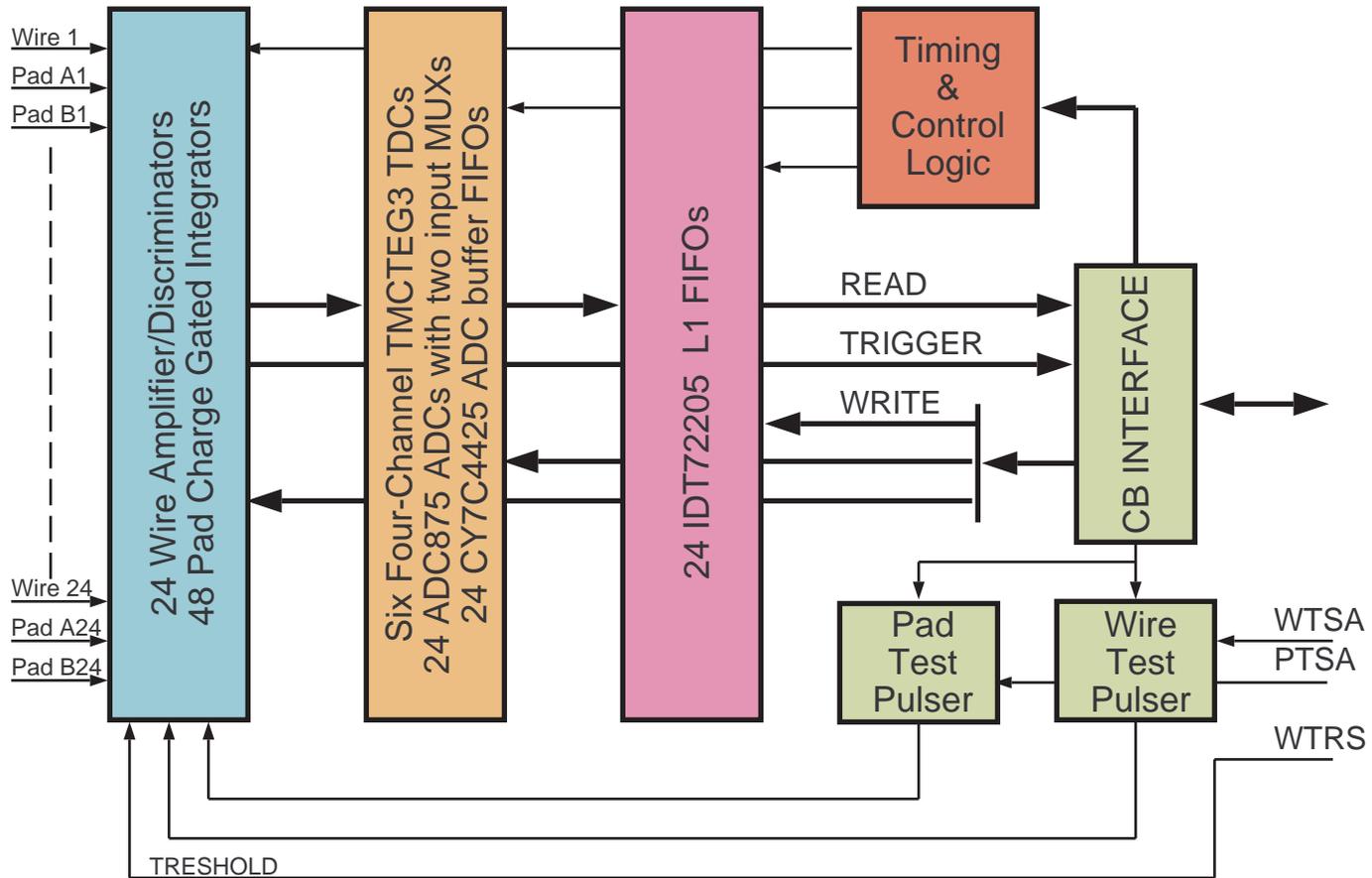


Fig. 2. Block diagram of 24-channel muon PDT Front-End Board.

delayed by the pipelines for about 4  $\mu\text{s}$  which is the Level 1 trigger decision time. If a trigger accept is generated, the appropriate portion of the time history from the pipelines is transferred to the Level 1 FIFOs. From there information is readout under control of the CB. The FEB also receives its timing signals via the CB interface. A detailed specification of the FEB is provided in the Appendix A. The following sections describe different aspects of the proposed FEB design.

#### A1. Wire Amplifier and Discriminator

Wire signal discrimination is performed by the Wire Amplifier and Discriminator (WAD). A two stage amplifier (UPC1663G and HFA1135) provides a gain of 1  $\mu\text{A}/\text{mV}$  at the discriminator input. A schematic diagram of the wire channel is shown in Fig. 3. The amplifier has a differential input which rejects common mode signals. The transformer coupling also rejects low frequency noise. The amplifier has a rise time of 8 ns and an input noise level of 85 nA (RMS) for the bandwidth of interest. This allows us to operate with a discriminator threshold as low as 0.5  $\mu\text{A}$ . Additional measurements are necessary to determine the level of a synchronous noise produced by the digital part of the board. It is likely that this noise level will define the actual minimum threshold achievable. L101 and C109 will be used to adjust the bandwidth of the amplifier to optimize  $\Delta t$  resolution (discussed later). An HFA1135 has an internal limiting feature which is used to reduce the recovery time of the amplifier when overdriven by high level input signals. These limits are set to +3V and to -1V respectively.

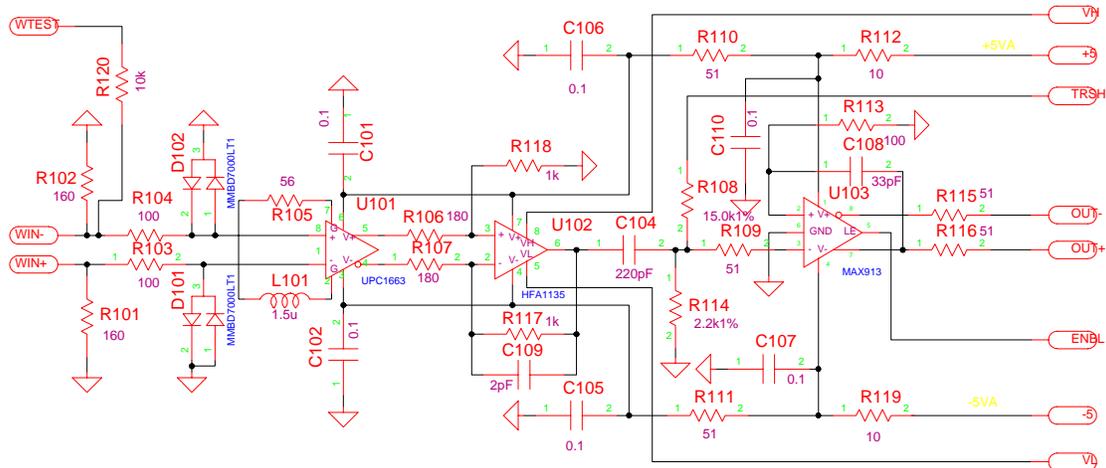


Fig. 3. Wire amplifier and discriminator.

A discriminator using the Maxim MAX913 comparator with capacitive feedback to set the output pulse width at 40 ns is used. The 40 ns minimum width is required by the time-to-digital converter chip to prevent false interpolator codes. This comparator has excellent input overdrive versus delay characteristics. The 2x to 20x over threshold propagation delay difference is less than 2 ns. The comparator has complementary outputs to match the differential inputs of the TDC chip we have selected. This arrangement has the additional

benefit of less feedback to the amplifier input than single ended outputs. The power consumption is less than 15 mA from  $\pm 5$  V supplies.

### A2. Wire Signal Triggering.

The WAMUS pads have 700 pF of capacitance which limits the noise performance and bandwidth of their preamplifiers. Because the pad signals are unique to one tube while the wire signals are not, due to its jumper wire, the old triggering scheme was based on the discrimination of a differentiated pad signal integrator output. The 400 ns width of this signal is not a problem at a crossing time of 3.2  $\mu$ s, but is too long for one of 132 ns. The wire signal is much faster than the pad signal, but the tube pair ambiguity problem must first be resolved in order to use it as a trigger. The signals coming from two adjacent wires need to be separated in order to determine which of the drift cells is hit.

A wire signal will always arrive first at the near end of the tube in which it occurred before crossing the jumper and traveling the full length of the adjacent tube and appearing at its near end. To determine first arrival, a simple two D-type flip-flop separator circuit clocked by the wire signals with cross-connected Q-bar outputs to D inputs is used. Both flip-flops are reset 60 ns after the output signal is generated. Fig. 4 shows this arrangement. When the difference in arrival time is less than the propagation delay and setup time of the flip-flop this scheme breaks down. Replacing the existing far end jumper with a delay line of 20 ns solves this problem. The custom delay line, a DL3855 from Datatronics, is matched to the 330 ohm tube impedance and is referenced to ground with HV capacitors. The rise time of the delay line is about 7 ns. A prototype separator circuit based on ALTERA EPX740 PLD chip has been tested and the resolution time of the circuit is shown in the Fig. 5. It is clear that selected delay line provides enough time for such a circuit to separate two signals.

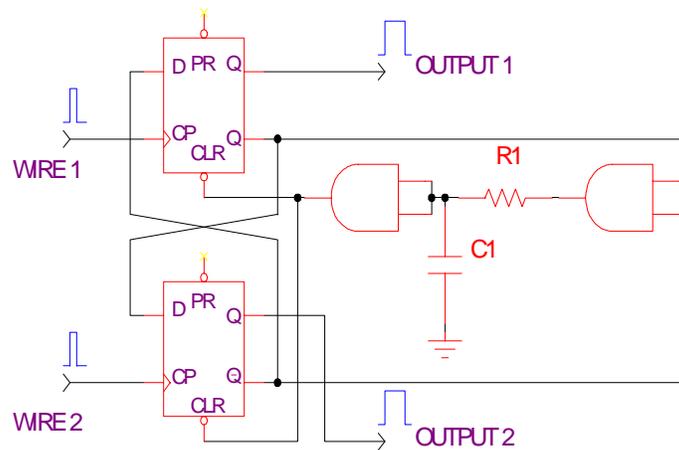


Fig. 4. Wire signal separator.

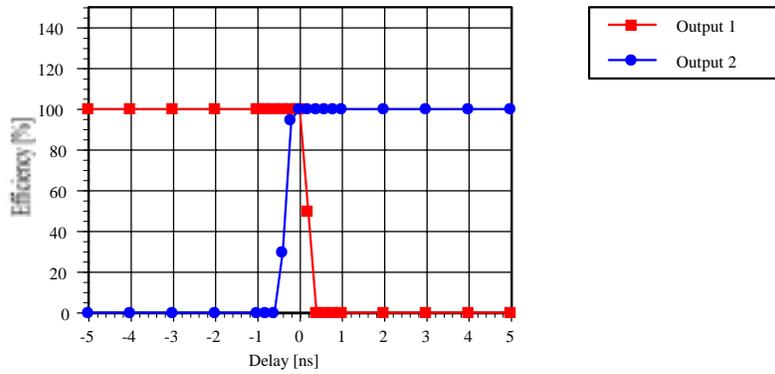


Fig. 5. Wire signal separator time resolution.

Fig. 6 shows the response of the wire signal separator with this delay installed on a pair of test tubes measured using the old analog  $\Delta$ TVCs on cosmic rays. Scintillation counters were located at the far end of the drift tubes which guarantees the minimum time difference between two wire signals. Fig. 6a shows the  $\Delta t$  distribution without regard to the separator output. Fig. 6b and Fig. 6c show the same data qualified by the separator outputs. There is clean separation between the two tubes. The proposed circuit will produce valid result only with one track crossing two paired PDT cells. In the rare case of two particles crossing paired cells and generating wire signals within time resolution of the separator (60 ns), the latest signal will be suppressed and no trigger signal will be generated for this wire. An off-line analysis can identify and flag such events after track reconstruction.

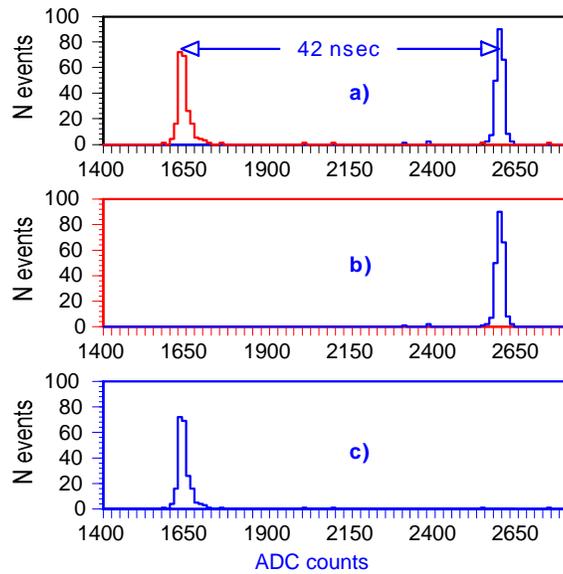


Fig. 6.  $\Delta t$  distribution with a  $10 \times 10 \text{ cm}^2$  trigger scintillator at one end. a - all signals, b - wire 1 tag, c - wire 2 tag.

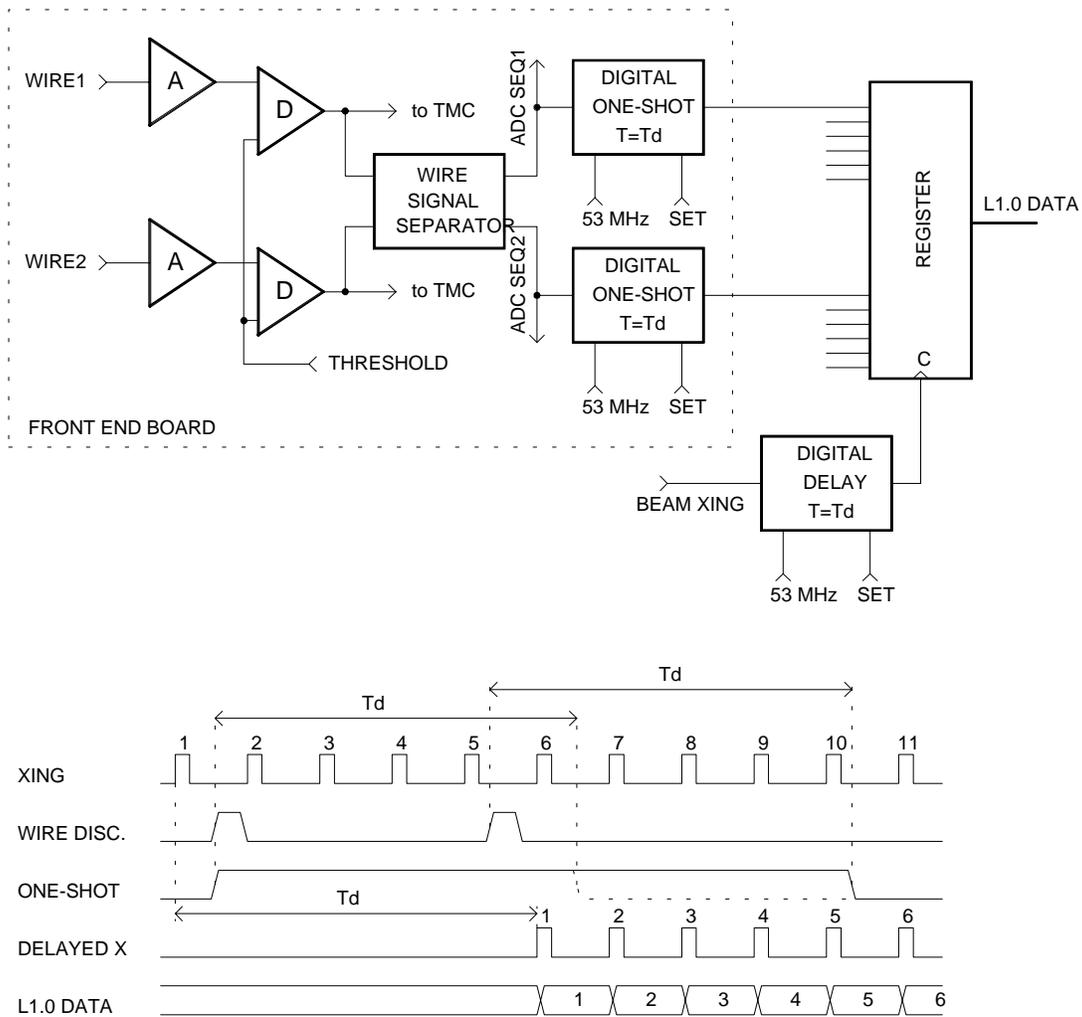


Fig. 7. Wire signal trigger logic block diagram and timing.

A block diagram of the logic used to form hit maps for the first level trigger system is shown in Fig. 7. The amplifiers (A) and discriminators (D) generate logic pulses from the wire signals. The complete hit map for a particular collision cannot be determined until the maximum drift time has elapsed because the tube signals are delayed by an unknown amount up to the maximum drift time. The strobe for the trigger logic must then be a copy of the crossing frequency delayed by this amount. The separator outputs fire retriggerable digital one-shots clocked by the 53 MHz accelerator RF, whose output widths are set equal to the maximum drift time of the detectors. The purpose of the one-shots is to lengthen the discriminator signals to such an extent that the earliest arrivals from a particular collision persist until the sampling time. The sampling of the one-shot outputs is performed at the Control Board (CB) which is a readout controller for all FEBs located on one PDT.

Since the storage time of the tubes is greater than one crossing interval, it is impossible to correlate hits and crossings at the CB level. It can only produce a list of trigger candidates. Additional high time resolution detectors have to be included in the Level 1

trigger system in order to determine the crossing from which the hits originated. A wire signal can originate from any crossing within the maximum drift time before its arrival. If the PDT drift time is about 800 ns, this covers up to six crossings at the 132 ns interval. This means that the trigger output has to be six crossings wide to cover all possible origins. The timing of three possible wire hits are shown in Fig. 8. This includes a depiction of two hits within one maximum drift interval to illustrate the need for retriggerability of the one-shots. One hit produces up to six trigger candidates whose validity can only be ascertained by applying the times constraints of other fast detectors, specifically scintillator counters. The trigger candidates correspond to wire signals delayed by as much as the maximum drift interval. Therefore it is necessary to delay the scintillator counter signals by the same amount before a coincidence can be formed. This is shown in the bottom portion of the figure.

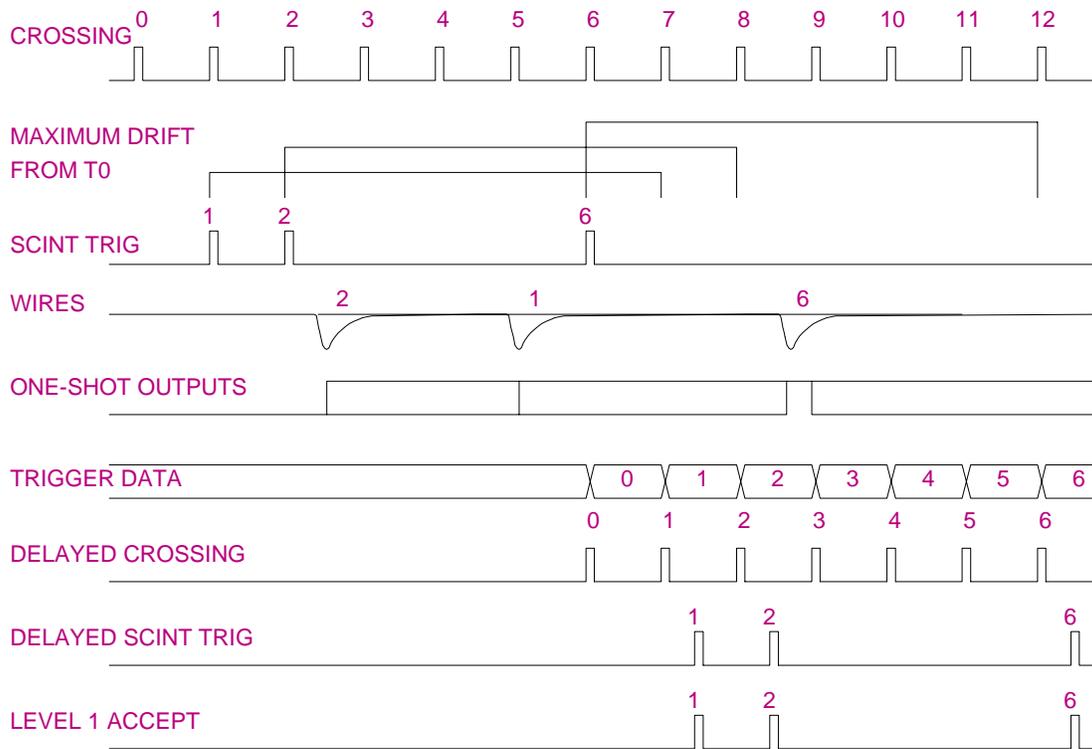


Fig. 8. Drift time tube ambiguities.

### A3. Digital Time Measurements

The requirement on time resolution of the muon system is driven by the  $\Delta t$  measurement. The wire signal traverses one 60 cm vernier pad in about 3 ns. We would like to have a resolution of at least 30 cm or about 1.5 ns. Time measurements are made by a four channel TDC chip (TMCTEG3) developed for the SSC by a group at KEK [7]. The TMC chip has a bin width of 0.78 ns at its nominal clock frequency of 40 MHz. The chip provides five bits of interpolator data and a hit flag bit for each channel. The data is stored in an internal 128-deep memory with independently settable read and write pointers. We are going to operate the chip at a frequency of 53/2 MHz which will give us ample

resolution (1.2 ns binning) and sufficient storage time for the Level 1 decision time. At this frequency, the data can be stored for as long as 4.8  $\mu$ s before it is overwritten, which is less than the Level 1 decision time of 4.1  $\mu$ s. This makes possible a deadtimeless synchronous data readout which is very attractive. The block-diagram of the digital time measurements is shown in the Fig. 9.

The  $\Delta t$  measurement is done indirectly by subtracting the two drift times for adjacent tubes as opposed to the old system, which performs the  $\Delta t$  measurement in hardware. Our studies using the existing analog electronics show that there is no significant difference between the two methods for determining  $\Delta t$ . Another result of these studies is that reduction of the bandwidth of the wire amplifier improves  $\Delta t$  resolution and slightly worsens drift time resolution. There should be an optimum rise time for the wire amplifier which will provide desired performance for  $\Delta t$  and drift time measurements. Further tests with the final gas mixture and FEB prototype are necessary to determine optimum component values for the wire amplifier.

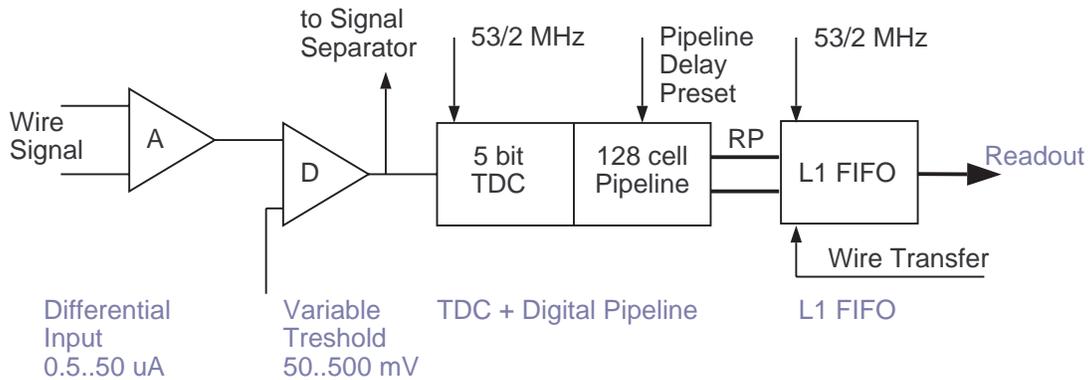


Fig. 9. Digital time measurements.

#### A4. Pad Signal Amplifier and Integrator.

The old pad electronics is the commonly used charge sensitive preamplifier followed by a dual base line subtractor. The decay time constant of the preamplifier is very long (40  $\mu$ s) and limits the counting rate of the channel to a few kHz. This scheme only works when the beam crossing intervals are greater than the drift time, and the likelihood of multiple hits within this interval is small, which is clearly not the case for the upgrade collider mode.

A schematic diagram of the new pad channel is shown in Fig. 10. The charge amplifier used in an old design has an FET input stage which gives very good noise performance but, at the expense of bandwidth. The time required to collect charge from the large capacitance of the pads is now a much more critical parameter in Run II. Charge collection time is partially a function of input impedance which is in turn a function of bandwidth. We have measured the input impedance of the old charge amplifier to be on the order of

65Ω. The new preamplifier uses RF bipolar transistors (NEC NE856) and has an input impedance of about 20Ω. It has a gain of 300 mV/pC, the same as the current design. The average charge collected from the pads is about 2 pC. The recovery time of the integrator is the most critical parameter in Run II. In Run Ib, nearly half of the channels saturated their charge integrators, and it was necessary to modify their integration time constant. The expected rates for Run II are even higher. The integrator has a CMOS switch (74LV4066) externally connected in parallel to the capacitor. The discharge time of the integrator

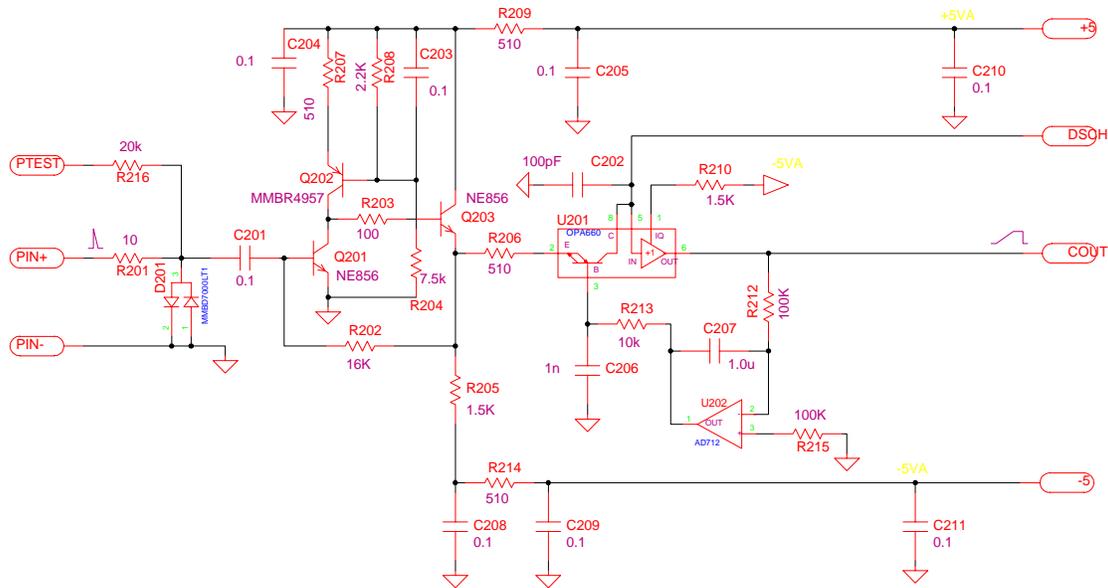


Fig. 10. Pad preamplifier and gated integrator.

capacitor is less than 20 ns which allows us to use a reset pulse 50 ns wide. A high impedance BiFET input amplifier (AD712) provides DC zeroing at the integrator output.

#### A5. Pad Signal Processing.

In the new design, each pad channel is triggered by its corresponding separator output.

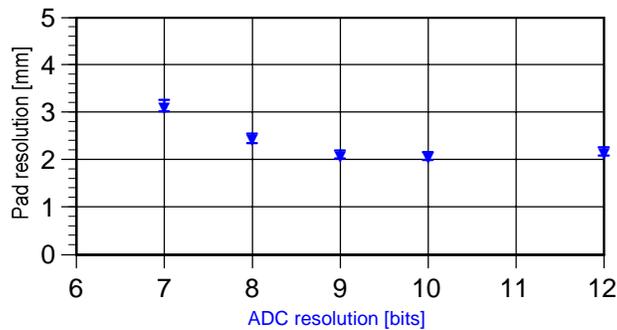


Fig. 11. Pad coordinate resolution versus ADC resolution.

This results in a sampling interval that is fixed with respect to the pad signal. The pad data from Run I which has 12 bits of precision, was truncated one bit a time and plotted. The results are shown in Fig. 11. and clearly demonstrate that 10 bits of ADC resolution is sufficient. This allows us to use a newly available low cost pipelined ADC followed by a more reliable digital buffer instead of the analog buffers used in the old design. The delay between the sampling point and valid data out of the Analog Devices AD875 is three clock cycles, which allows baseline sampling without any external delays. The ADC and memory buffer are continuously clocked at 53/4 MHz. Signals synchronous with the ADC clock are generated by the ADC sequencer which is triggered by the asynchronous separator output. Fig. 12 shows the simplified block diagram of the pad signal processing. The sequencer

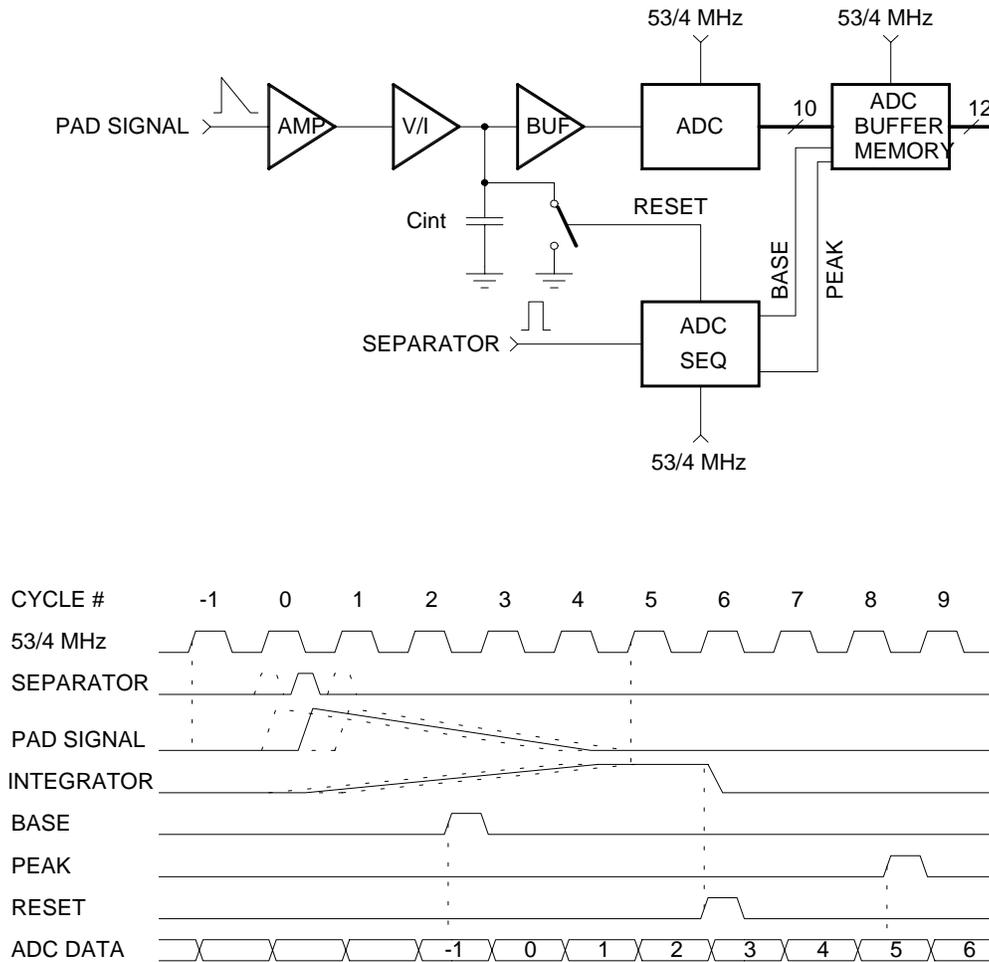


Fig. 12. Pad signal processing block diagram and timing.

generates BASE and PEAK bits which are flag bits appended to the data stream to facilitate zero suppression at the time when data is transferred from the ADC buffer memory to the next level of buffering. The integrator is reset after its signal has been sampled by the ADC, thus reducing the recovery time of the integrator to 50 ns. The ADC buffer memory is a FIFO with external logic that allows the difference between the read and write pointers to be programmable. Level 1 triggers are formed while the data is

clocking through the buffer. The length of the buffer is adjusted so that the data emerges approximately in time with the arrival of the L1 trigger accept.

#### A6. Pad Signal Multiplexing.

Instead of using two independent ADCs and FIFO memories per single wire as it is shown in the Fig. 12, one can implement an analog multiplexer at the ADC input which will reduce number of ADCs per tube to one. The multiplexer runs at a  $53/8$  MHz clock frequency synchronously with the ADC clock. The drawback of such a solution is an increased duration of the sequencer cycle which is mainly determined by the integrator rise time of about 150 ns. Additional time required for multiplexing is one half of a  $53/8$  MHz clock period or 75 ns. The multiplexer is based on the same type of CMOS analog switch (74LV4066) used to discharge the integrator capacitor. Since TMC chip and corresponding L1 FIFO are running at  $53/2$  MHz which is twice higher than the ADC clock, it is possible to implement the next stage of multiplexing on the digital level thus further reducing the cost of the pad electronics. Two ADC buffer memories are multiplexed at the L1 FIFO input shown in Fig. 13.

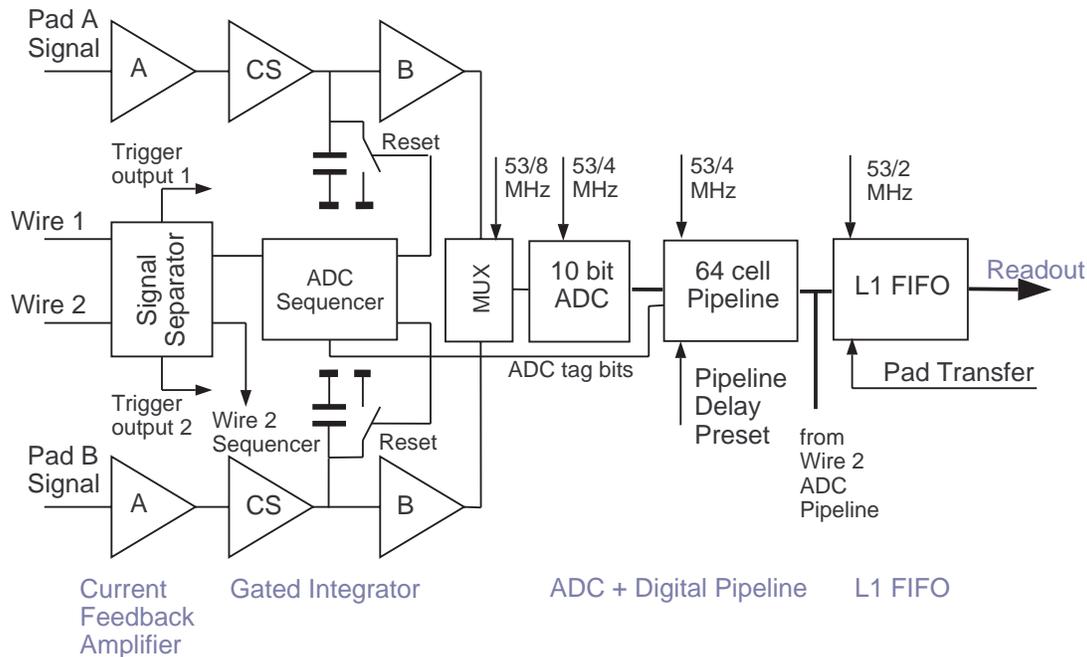


Fig. 13. Pad signal multiplexing.

#### A7. Deadtimeless Readout and Event Synchronization

The principle advantage of the new system is its storage of digitized data in circular buffers pending a trigger decision, with no data loss. For the sake of simplicity, all the components of the Front-End Board and Control Board are synchronized to subharmonics of 53 MHz. The TMC chip has its own 128 deep buffer controlled by its read and write pointers. The difference in the pointer settings allows the data to be delayed for the necessary trigger decision time. Five bits of data from the read pointer output are

combined with five TMC output bits in order to extend its range to span the full drift time. The bunch spacing occurs at an uneven subharmonic ( $1/7$ ) of 53 MHz which makes it necessary to make corrections to the TMC data in order to resolve the ambiguities between bunches occurring at the beginning or the middle of a TMC clock cycle.

For ADC data an external memory buffer is used which runs in a manner similar to the TMC internal buffer. Because of the lower bandwidth of the pad channel, a  $53/4$  MHz frequency is used for its synchronization. During multiplexing at the L1 FIFO input ADC data is written into FIFO at  $53/2$  MHz clock frequency. Pad information is not time correlated and doesn't require the correction for uneven subharmonics. Because pad information is multiplexed at the ADC input, there is a possibility of transferring only a portion of the background event pad data to the L1 FIFO. This problem is discussed in the following section describing FEB data formats. Because of the specified minimum interval between two L1 accepts of  $2.6 \mu\text{s}$ , data transfers to L1 FIFOs are invisible to the DAQ system and do not generate any dead time.

Level 1 and Level 2 decisions come from the D0 trigger framework down to the front ends located in the collision hall. In order to reduce the likelihood of synchronization problems and correctly identify the crossing at which a trigger has occurred, the trigger framework provides an eight bit crossing number to the front-end electronics. This number is compared to a local crossing counter value, which is stored in a buffer memory of the same type as those used within the TMCs and attached to the ADCs. The data appearing at the output of the memory buffers must be directed to the L1 FIFOs used to store Level 1 accepts at the point exactly correspondent to the crossing generating the accept. This could be done by performing timing adjustments on all the trigger signals however, achieving a timing uniformity of 18 ns over the entire muon system is a daunting prospect.

By comparing the values of the local counter and the Level 1 crossing number, the time of arrival of the trigger is no longer critical. However, the buffer delay setting must be greater than or equal to the Level 1 decision time. The excess delay should be as small as practical, due to the limited range of the pipeline depth. The duration of the data transfer to the Level 1 FIFOs is programmed within the Level 1 logic and is equal to the maximum drift time for TMC data. For the ADC data, because of the rise time of the integrator signal, and a one clock cycle uncertainty in the arrival time of the asynchronous pad signal, the transfer takes about  $0.5 \mu\text{s}$  longer. Based on the flag bits previously appended to the data stream, only valid hits are stored. There are event boundary marker words embedded in the data written to the Level 1 FIFOs, so several events can be stored in a buffer.

#### A8. Front-End Board Data Formats.

Pad and wire information is transferred from the L1 FIFO memories located on the FEBs via an 18 bit data bus. The number of words transferred depends on the number of hits digitized for the particular event and thus varies. Each FIFO memory has to be read out for each event. The FEB readout logic transfers data words from the TMC and ADC pipelines upon receiving wire transfer and pad transfer signals from the Control Board. Only valid hit data is transferred to the L1 FIFOs. An event separator word is added at the end of the each transfer indicating end of the event data. If there is no hit data present



the particular event from the FIFO, only one data word with EF=0 will be available for the readout.

During the readout, event data is converted to a 16 bit data format by the CB readout controller. Because of the asynchronous nature of the wire signals and a finite drift time interval, there is a non-zero probability of reading out a portion of the pad information instead of the full event. This happens when background tracks originating from other interactions before the one that caused the trigger decision are present. It is necessary to identify such events and appropriately handle them. The typical good pad event will look like one of these two examples:

1	1	1	1	0
1	1	1	1	
B	B	P	P	I
A	A	E	E	N
S	S	A	A	V
E	E	K	K	A
				L
				I
A	B	B	A	D

17 Event separator  
Even/odd wire  
0

1	1	1	1	0
2	2	2	2	
B	B	P	P	I
A	A	E	E	N
S	S	A	A	V
E	E	K	K	A
				L
				I
B	A	A	B	D

17 Event separator  
Even/odd wire  
0

Unfortunately, all partial combinations of the two are possible for background events. The other rare situation when two paired wires are hit by separate tracks overlapping within drift time interval will generate the following picture:

1	1	1	1	1	1	1	1	0
1	1	1	2	1	2	2	2	
B	B	P	B	P	B	P	P	I
A	A	E	A	E	A	E	E	N
S	S	A	S	A	S	A	A	V
E	E	K	E	K	E	K	K	A
								L
								I
A	B	B	B	A	A	A	B	D

17 Event separator  
Even/odd wire  
0

Of course, the overlap of the pad information is completely arbitrary and cannot be predicted. The DSP software has to be able to recognize such events and flag them. This operation only needs to be performed at the Level 3 event rate (1 KHz) and thus is not considered to be an undue burden on the DSP.

#### A9. Input Connectors and Data Ordering.

Each FEB has six 34 pin connectors (see Appendix B) bringing in 24 differential wire signals and 48 single ended pad signals. The proposed FEB design uses IDT 72205 256 x 18 bit FIFO memories as the L1 FIFO. Two five bit TMC channels and one five bit read pointer are connected to one FIFO chip according to the data format description in section

A8. Therefore, two TMC channels are paired within an FEB to reduce the number of FIFO chips used. The channels are numbered on the FEB from left to right starting from the input connector located in the leftmost corner of the board. This puts some limitations on the input connections to the detector. The other problem is related to the 72/96 cell varieties of the PDTs. In order to make just one version of the FEB, the input connector is compatible with a 96 cell (four deck) PDT. For 72 cell (three deck) PDT, a special cable is required to make use of all FEB channels. The Fig. 14 shows the proposed design for such a cable. Since the order of channel numbers is not changed in this arrangement, it is called a natural (i.e. following the natural FEB channel ordering) scheme.

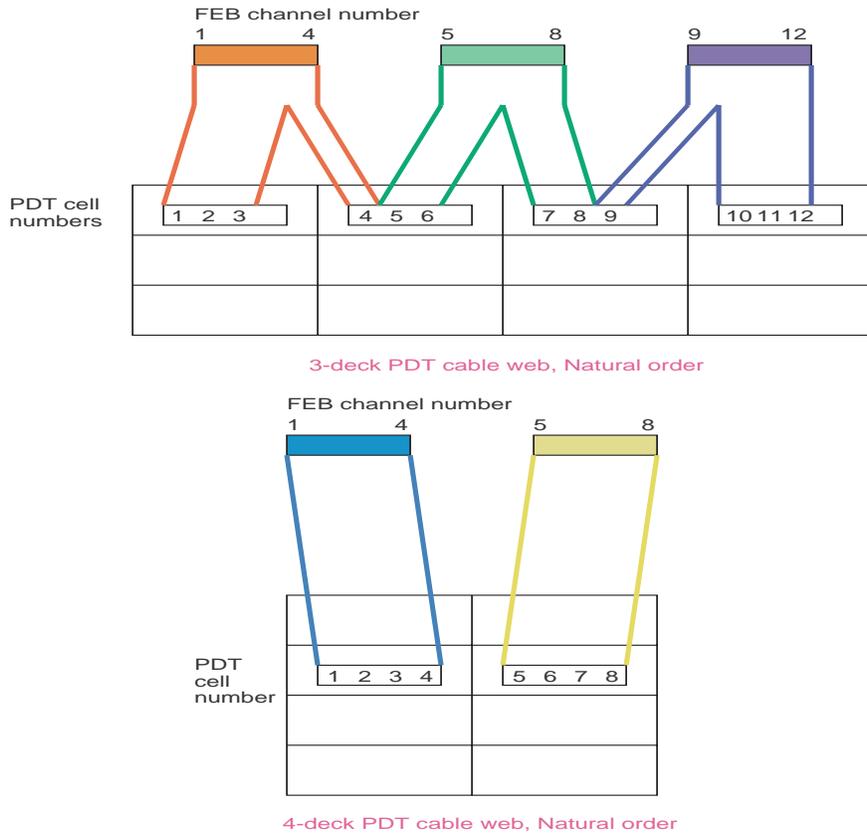


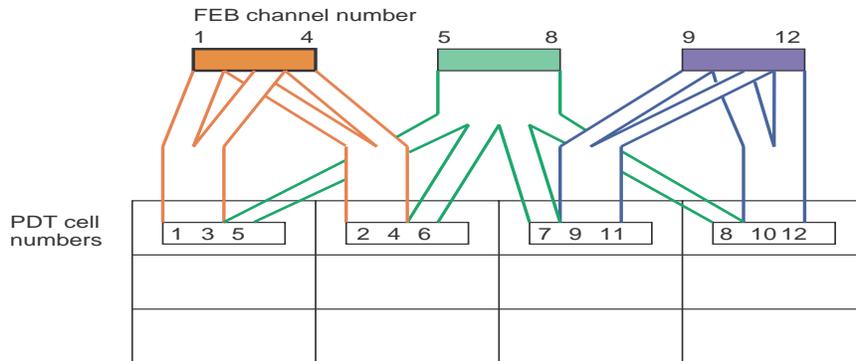
Fig. 14. FEB input connections, natural order.

Other options can be implemented, if different numbering schemes are required. In this case all the necessary changes have to be done externally by modifying the cable connection. A possible example of specific channel numbering implementation is shown in the Fig. 15. The cable web looks more complicated, but it makes the necessary connections without layout changes to the FEB.

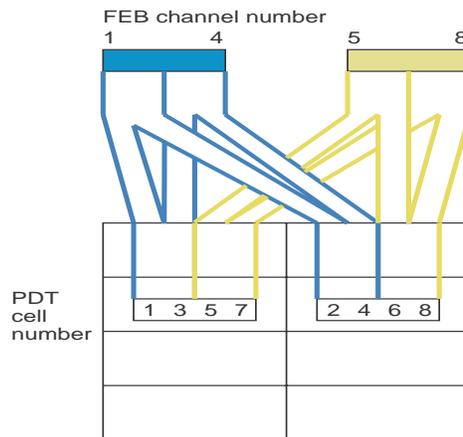
A10. Front-End Board Control and Trigger Connections.

Each FEB has one 100 pin high density connector with signals for fast data readout, a control data bus and other specific timing and control lines (see Appendix B). All readout and timing signals use LVDS differential drivers and receivers to minimize feedback to the FEB inputs. The control bus uses series-terminated TTL signals. The readout clock

frequency is 12.5 MHz and the control bus data rate is 10 Mbytes/s. One 50 pin high density connector is used for 24 trigger output signals generated by the digital one-shots. These signals use also LVDS levels. The Control Board provides also three analog levels to control a common threshold of all wire discriminators and amplitudes of wire and pad test pulses. There is one trigger OR signal on the data & control connector which is generated by the FEB logic. This signal is a 24 fold OR of all the trigger outputs and can be used by the CB to form an internal trigger simulating a L1 Accept. The power supply connector uses



3-deck PDT cable web, Data specific order



4-deck PDT cable web, Data specific order

Fig. 15. FEB input connections, data specific order.

the same pinouts as the existing PDT cables. This will allow the use of the same DC distribution printed boards as in the existing system. The FEB uses separate +/- 5 V power supplies for analog and digital portions of the board. The pinouts for the FEB connectors are listed in the Appendix B.

There are several registers in the FEB which control the mode and parameters of the FEB components (see Appendix C).

- Three 8 bit Channel Enable registers. Each bit of these registers turns on and off the corresponding wire discriminator and associated pad channels.

- 8 bit Run Control register. One of four bits of this register enables or disables the wire or pad information digitization and wire or pad transfer signal.
- The ADC pipeline register. This register sets the pipeline delay for pad information.
- Three 8 bit ADC FIFO Empty Flag registers. These registers are used for on-line testing of the board.
- Three 8 bit ADC Test registers. These registers enable a fixed bit pattern to be generated at the selected ADC output. They are used for on-line testing of the board.
- There are also six groups of four 8 bit registers which control six TMCs. These registers set the pipeline delay and perform some on-line testing of the TMC.

Appendix A.

FRONT-END BOARD MAIN PARAMETERS.

1. Wire signal amplifier & discriminator (WAD)

- differential input impedance	320 ohms
- minimum threshold	0.5 $\mu$ A
- input signal dynamic range	0.5..50 $\mu$ A
- double pulse resolution	40 ns
- rise time	8..20 ns *
- variable threshold range	0.5..5.0 $\mu$ A

2. Pad signal preamplifier & integrator (PAI)

- input impedance	20 ohms
- integrator rise time	<150 ns
- integrator reset time	50 ns
- minimum S/N ratio	1:200 *
- sensitivity	300 mV/pC *

3. Time digitizer

- bin width (@ 53/2 MHz)	1.18 ns
- time resolution (RMS @40 MHz)	250 ps *
- integral non-linearity	<80 ps *
- differential non-linearity	<60 ps *

4. Charge digitizer

- ADC resolution	10 bit
- sampling frequency	53/4 MHz

- integral non-linearity  $\pm 1$  LSB
- differential nonlinearity  $\pm 0.4$  LSB
- pad charge dynamic range  $0..3$  pC \*

#### 5. Trigger logic & data buffering

- maximum drift time readout interval (@53/2 MHz) 1186 ns
- trigger pulse duration range (@53 MHz)  $19..1186$  ns \*
- wire signal separator resolution  $< 1$  ns
- separator double pulse resolution  $< 80$  ns
- digital pipeline depth (ADC and TMC)  $4.8$   $\mu$ s
- ADC pipeline step ( @53/4 MHz) 75 ns
- TMC pipeline step (@53/2 MHz ) 37.7 ns

#### 6. Data readout and Control

- number of wire channels 24
- number of pad channels 48
- Level 1 FIFO depth  $> 16$
- data readout signal levels LVDS
- control signal levels TTL
- readout frequency 12.5 MHz
- readout algorithm fixed address seq.

#### 7. Physical dimensions

21.6" x 14" x 1"

#### 8. Estimated power consumption

+5V digital	8 A <sup>*</sup>
+5V analog	2.5 A <sup>*</sup>
-5V analog	1.6 A <sup>*</sup>

Notes: <sup>\*</sup>) indicates a parameter to be measured

Appendix B.

## FRONT-END BOARD CONNECTORS.

## 1. Input connectors

Type: Right angle, 34 pin, 3M p/n 3431-5303

Table 1. Input signals.

Pin	Signal name	Description	Comment
1,2	GND	Shield	
3	GND	Return path	GND in 3 deck board
4	P41B	Pad 4B	GND in 3 deck board
5	W41+	Wire 4 positive	GND in 3 deck board
6	W41-	Wire 4 negative	GND in 3 deck board
7	GND	Return path	GND in 3 deck board
8	P41A	Pad 4A	GND in 3 deck board
9,10	GND	Shield	
11	GND	Return path	
12	P31B	Pad 3B	
13	W31+	Wire 3 positive	
14	W31-	Wire 3 negative	
15	GND	Return path	
16	P31A	Pad 3A	
17,18	GND	Shield	
19	GND	Return path	
20	P21B	Pad 2B	
21	W21+	Wire 2 positive	
22	W21-	Wire 2 negative	
23	GND	Return path	
24	P21A	Pad 2A	
25,26	GND	Shield	
27	GND	Return path	
28	P11B	Pad 1B	
29	W11+	Wire 1 positive	
30	W11-	Wire 1 negative	
31	GND	Return path	
32	P11A	Pad 1A	
33,34	GND	Shield	

## 2. FEB to CB data &amp; control connector

Type: right angle, 100 pin, Circuit Assembly p/n CA-100NFHR-12GT-20

Table 2. Differential LVDS signals.

Pin number	Number of wires	Signal name	Description	Direction
1 to 36	36	DB00 to DB17	Readout Data (18 bits)	FEB => CB
69,70	2	TrgOR	24 channel Trigger OR	FEB => CB
71,72	2	Read/Write	Data Direction Control	CB => FEB

73,74	2	RdClk	Read Clock	CB => FEB
75,76	2	BdSel	Board Select	CB => FEB
Pin Number	Number of wires	Signal name	Description	Direction
77,78	2	Strb	Control Bus Data Strobe	CB => FEB
79,80	2	CBClk	Return Read Clock for CB	FEB => CB
81,82	2	Wire/Pad	Wire/Pad Data Indicator	CB => FEB
83,84	2	IRST	Initial Reset (INIT)	CB => FEB
85,86	2	WEVT	Wire event transfer signal	CB => FEB
87,88	2	PEVT	Pad event transfer signal	CB => FEB
89,90	2	53 MHz	Tevatron Clock	CB => FEB
91,92	2	TRST	Timing Reset (FC) Signal	CB => FEB
93,94	2	TEST	Test Signal	CB => FEB

Note: All odd pins are positive true signals.

Table 3. Single ended CMOS/TTL signals

Pin number	Number of wires	Signal name	Description	Direction
37	1	ERR1	Error 1 signal	FEB => CB
38	1	GND	Return path	
39	1	CB00	Control Data bit 0	CB <=> FEB
40	1	GND	Return path	
41	1	CB01	Control Data bit 1	CB <=> FEB
42	1	GND	Return path	
43	1	CB02	Control Data bit 2	CB <=> FEB
44	1	GND	Return path	
45	1	CB03	Control Data bit 3	CB <=> FEB
46	1	GND	Return path	
47	1	CB04	Control Data bit 4	CB <=> FEB
48	1	GND	Return path	
49	1	CB05	Control Data bit 5	CB <=> FEB
50	1	GND	Return path	
51	1	CB06	Control Data bit 6	CB <=> FEB
52	1	GND	Return path	
53	1	CB07	Control Data bit 7	CB <=> FEB
54	1	GND	Return path	
55	1	AD00	Control Address Line 00	CB => FEB
56	1	GND	Return path	
57	1	AD01	Control Address Line 01	CB => FEB
58	1	GND	Return path	
59	1	AD02	Control Address Line 02	CB => FEB
60	1	GND	Return path	
61	1	AD03	Control Address Line 03	CB => FEB
62	1	GND	Return path	
63	1	AD04	Control Address Line 04	CB => FEB
64	1	GND	Return path	
65	1	AD05	Control Address Line 05	CB => FEB
66	1	GND	Return path	
67	1	AD06	Control Address Line 06	CB => FEB
68	1	GND	Return path	

Note: All TTL signals are of positive true logic.

Table 4. Single ended analog signals

Pin number	Number of wires	Signal name	Description	Direction
95	1	WTRS	Wire Threshold (analog)	CB => FEB
96	1	GND	Signal return path	
97	1	WTSA	Wire Test Signal Amplitude	CB => FEB
98	1	GND	Signal return path	
99	1	PTSA	Pad Test Signal Amplitude	CB => FEB
100	1	GND	Signal return path	

Note: All analog signals are 0 to + 4096 mV @ 1 K load.

### 3. FEB to CB trigger data connector

Type: right angle, 50 pin, Circuit Assembly p/n CA-50NFHR-12GT-20

Table 5. Differential LVDS signals.

Pin Number	Number of wires	Signal name	Description	Direction
1,2	2	Trg01	Trigger Output 1	FEB => CB
3,4	2	Trg02	Trigger Output 2	FEB => CB
5,6	2	Trg03	Trigger Output 3	FEB => CB
7,8	2	Trg04	Trigger Output 4	FEB => CB
9,10	2	Trg05	Trigger Output 5	FEB => CB
11,12	2	Trg06	Trigger Output 6	FEB => CB
13,14	2	Trg07	Trigger Output 7	FEB => CB
15,16	2	Trg08	Trigger Output 8	FEB => CB
17,18	2	Trg09	Trigger Output 9	FEB => CB
19,20	2	Trg10	Trigger Output 10	FEB => CB
21,22	2	Trg11	Trigger Output 11	FEB => CB
23,24	2	Trg12	Trigger Output 12	FEB => CB
25,26	2	Trg13	Trigger Output 13	FEB => CB
27,28	2	Trg14	Trigger Output 14	FEB => CB
29,30	2	Trg15	Trigger Output 15	FEB => CB
31,32	2	Trg16	Trigger Output 16	FEB => CB
33,34	2	Trg17	Trigger Output 17	FEB => CB
35,36	2	Trg18	Trigger Output 18	FEB => CB
37,38	2	Trg19	Trigger Output 19	FEB => CB
39,40	2	Trg20	Trigger Output 20	FEB => CB
41,42	2	Trg21	Trigger Output 21	FEB => CB
43,44	2	Trg22	Trigger Output 22	FEB => CB
45,46	2	Trg23	Trigger Output 23	FEB => CB
47,48	2	Trg24	Trigger Output 24	FEB => CB
49,50	2	GND	Return path	

Note: All odd pins are positive true signals.

#### 4. Power supply connector

Type: right angle, 12 pin, Panduit p/n MPAS156-12-L

Table 6. Power supply cable.

Pin number	Number of wires	Signal name	Comment
1,2	2	+5V	Digital
3,4	2	GND	
5,6	2	-5V	Digital
7,8	2	GND	
9	1	+5VA	Analog
10	1	GND	
11	1	-5VA	Analog
12	1	GND	

Appendix C.

## FRONT-END BOARD ADDRESS MAP

Table 7. Address values are in hexadecimal notation.

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment
01	PTEN	WTEN	TGT5	TGT4	TGT3	TGT2	TGT1	TGT0	Trigger Gate
02	CE8	CE7	CE6	CE5	CE4	CE3	CE2	CE1	Channel ENBL
03	CE16	CE15	CE14	CE13	CE12	CE11	CE10	CE9	Channel ENBL
04	CE24	CE23	CE22	CE21	CE20	CE19	CE18	CE17	Channel ENBL
05	WF8	WF7	WF6	WF5	WF4	WF3	WF2	WF1	Wire FIFO EFs
06	WF16	WF15	WF14	WF13	WF12	WF11	WF10	WF9	Wire FIFO EFs
07	WF24	WF23	WF22	WF21	WF20	WF19	WF18	WF17	Wire FIFO EFs
08	BF8	BF7	BF6	BF5	BF4	BF3	BF2	BF1	ADC FIFO EFs
09	BF16	BF15	BF14	BF13	BF12	BF11	BF10	BF9	ADC FIFO EFs
0A	BF24	BF23	BF22	BF21	BF20	BF19	BF18	BF17	ADC FIFO EFs
0B	X	X	X	X	PEN	WEN	PRUN	TRUN	RUN Control
0C	AT8	AT7	AT6	AT5	AT4	AT3	AT2	AT1	ADC Test
0D	AT16	AT15	AT14	AT13	AT12	AT11	AT10	AT9	ADC Test
0E	AT24	AT23	AT22	AT21	AT20	AT19	AT18	AT17	ADC Test
0F	X	X	AD5	AD4	AD3	AD2	AD1	AD0	ADC Pipeline
10	Shift	MTS	NRPS	ENRP	X	TCH	TCH0	F/R*	TMC1 CRS0
11	X	RP6	RP5	RP4	RP3	RP2	RP1	RP0	TMC1 CSR1
12	X	WP6	WP5	WP4	WP3	WP2	WP1	WP0	TMC1 CSR2
13	SOUT	SIN	TD5	TD4	TD3	TD2	TD1	TD0	TMC1 CSR3
20	Shift	MTS	NRPS	ENRP	X	TCH	TCH0	F/R*	TMC2 CRS0
21	X	RP6	RP5	RP4	RP3	RP2	RP1	RP0	TMC2 CSR1
22	X	WP6	WP5	WP4	WP3	WP2	WP1	WP0	TMC2 CSR2
23	SOUT	SIN	TD5	TD4	TD3	TD2	TD1	TD0	TMC2 CSR3
30	Shift	MTS	NRPS	ENRP	X	TCH	TCH0	F/R*	TMC3 CRS0
31	X	RP6	RP5	RP4	RP3	RP2	RP1	RP0	TMC3 CSR1
32	X	WP6	WP5	WP4	WP3	WP2	WP1	WP0	TMC3 CSR2
33	SOUT	SIN	TD5	TD4	TD3	TD2	TD1	TD0	TMC3 CSR3
40	Shift	MTS	NRPS	ENRP	X	TCH	TCH0	F/R*	TMC4 CRS0
41	X	RP6	RP5	RP4	RP3	RP2	RP1	RP0	TMC4 CSR1
42	X	WP6	WP5	WP4	WP3	WP2	WP1	WP0	TMC4 CSR2
43	SOUT	SIN	TD5	TD4	TD3	TD2	TD1	TD0	TMC4 CSR3
50	Shift	MTS	NRPS	ENRP	X	TCH	TCH0	F/R*	TMC5 CRS0
51	X	RP6	RP5	RP4	RP3	RP2	RP1	RP0	TMC5 CSR1
52	X	WP6	WP5	WP4	WP3	WP2	WP1	WP0	TMC5 CSR2
53	SOUT	SIN	TD5	TD4	TD3	TD2	TD1	TD0	TMC5 CSR3
60	Shift	MTS	NRPS	ENRP	X	TCH	TCH0	F/R*	TMC6 CRS0
61	X	RP6	RP5	RP4	RP3	RP2	RP1	RP0	TMC6 CSR1
62	X	WP6	WP5	WP4	WP3	WP2	WP1	WP0	TMC6 CSR2
63	SOUT	SIN	TD5	TD4	TD3	TD2	TD1	TD0	TMC6 CSR3