12/11/97
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FEB8 Test Results with Muon PDT

Preliminary testing was performed with 8-channel PDT Front-end Board prototype connected to the muon PDT six feet long. The PDT was filled with Ar + 10% CF_4 + 10% CH_4 gas mixture and outfitted with new design service and delay boards. The FEB8 was powered and supplied with 53 MHz clock and INIT and TEST signals using HP8130A and HP8110A programmable pulsers respectively. The ALTERA FLASHlogic chips on the board were not configured. The threshold on wire channels was set to ~ 1 µA, which corresponds to ~150 mV amplifier output signal. All the measurements are performed with the clock signal turned off on the board and the scope triggered by telescope of two counters. The following is a list of performed measurements.

1. Wire amplifier measurements.

Instant pulse shape, average pulse shape, and drift time measurements have been made. See the following figures.

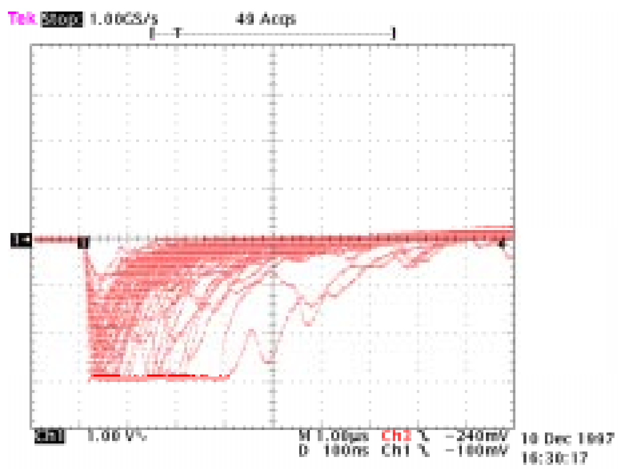

Figure 1. Wire amplifier (HFA1135) output with infinite persistence @ 4800 V.

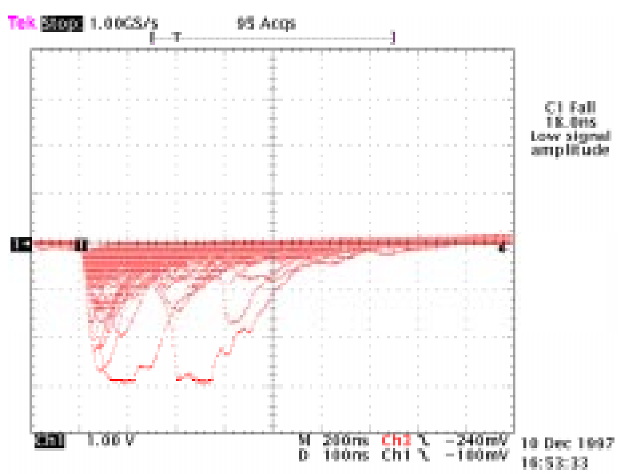

Figure 2. Same as in Figure 1, but @ 4600 V.

The wire amplifier has internal limiter set at 3.0 volts. This setting affects average amplitude measurements. As one can see from the Figure 1, the gas gain is more then adequate at 4800 V, so portion of the signals is cut by the limiter. The average pulse height is well above the threshold level (~150 mV). The average signal shape at the same high voltage is shown in Figure 3. The average value includes overflow pulses as well.

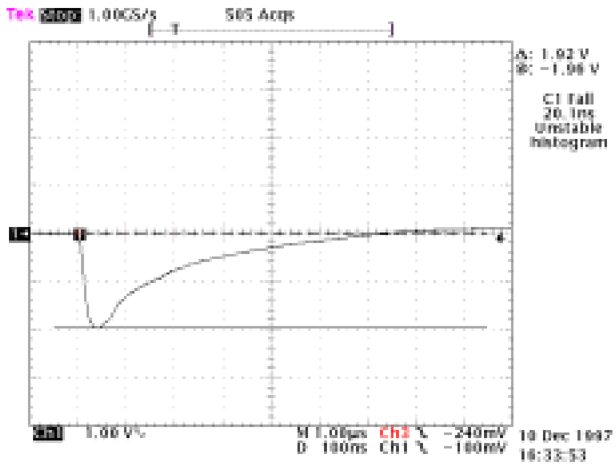

Figure 3. Average wire signal at HFA135 output (200 events, @ 4800 V).

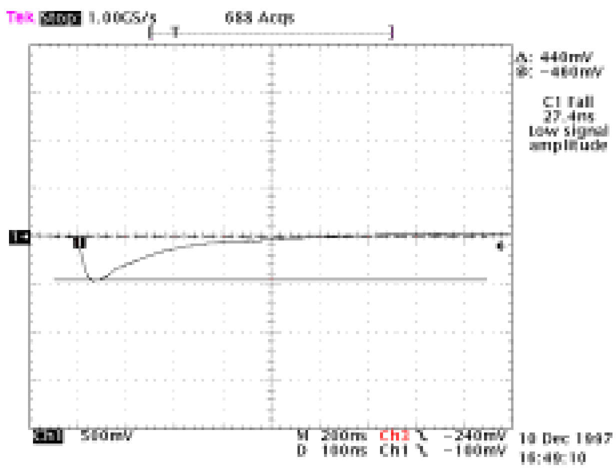

Figure 4. Same as in Figure 3, but @ 4600 V.

The average pulse height at 4600 volts is still about 500 mV, which is five times above the threshold. One can think of reducing the amplifier gain and, therefore, noise and crosstalk levels. This statement has to be verified by measurements with the longest PDT in the muon system.

The single wire pulse is shown in Figure 5. As one can see it is about 200 ns long at the threshold level and requires about that time to integrate the pulse charge. Overlapping discriminator pulses provides the coarse drift time measurement as it is shown in the Figure 6.

As we look at the discriminator input signal, we can make a conclusion regarding possible dead time associated with the shape of the wire pulse. It is obvious that input pulses have to be separated at the discriminator threshold level. One can see that the dead time of the PDT-Amplifier-Discriminator system is about 120 ns for the pulse shown in Figure 7. As per Figure 4, for cosmic events the dead time could be as big as 600..700 ns. For the beam events it will be around 100..200ns depending on gas multiplication. This makes possible to register up to three hits during one drift interval.

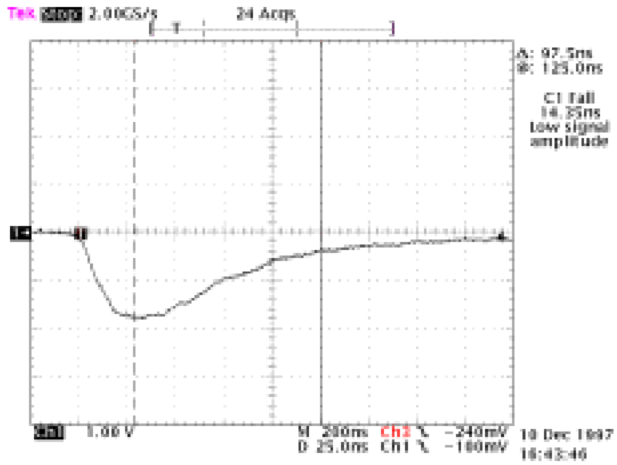

Figure 5. Single wire pulse output @ 4800 V.

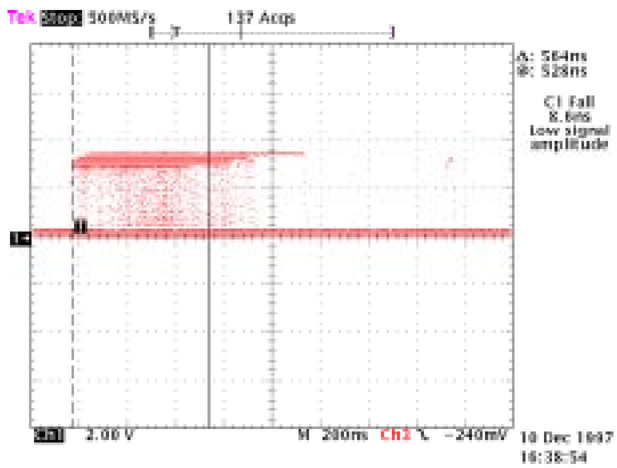

Figure 6. Drift time measurement.

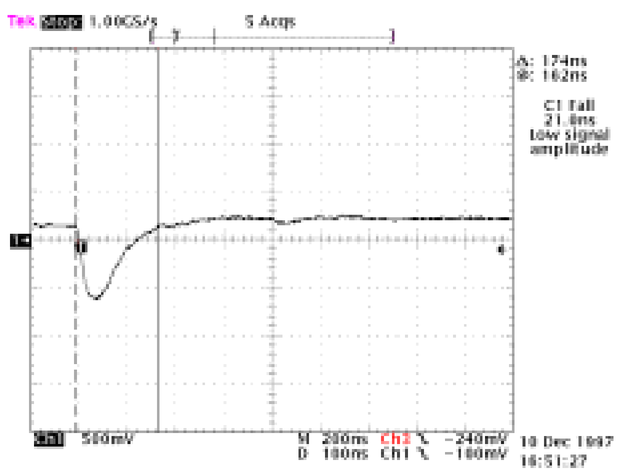

Figure 7. Wire pulse at discriminator input @ 4600 V.

2. Pad integrator measurements.

Instant and average pulse shapes have been measured for pad signal. See the following figures.

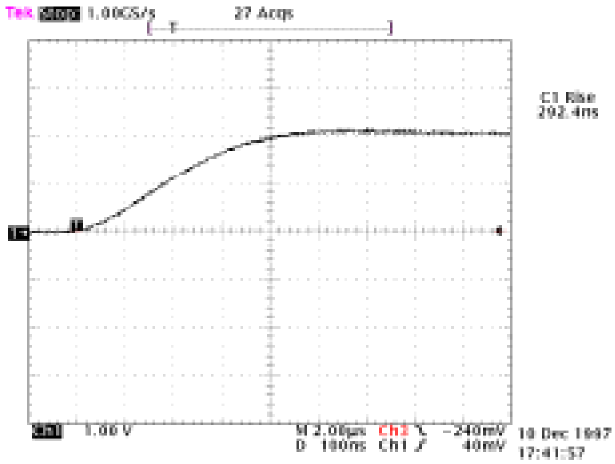

Figure 8. Pad A integrator single pulse @ 4800 V.

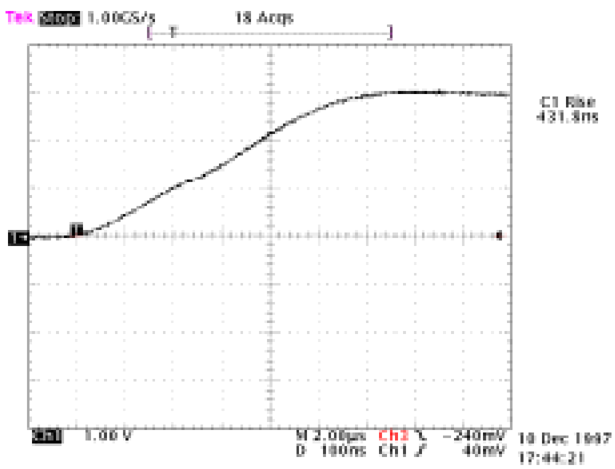

Figure 9. Pad B integrator single pulse @ 4800 V.

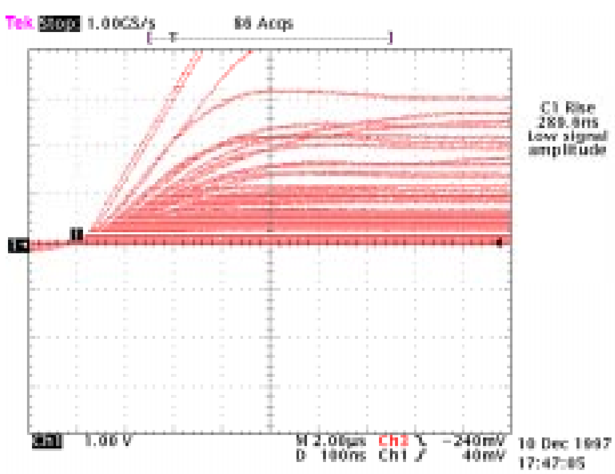

Figure 10. Pad A integrator pulse with infinite persistence @ 4800 V.

The most important conclusion one can make from the Figure 8, Figure 9 and Figure 10 is that pad pulse integration takes about 250..300 ns, but sometimes is as long as 600 ns. The sampling at the flat top of the pulse is required to achieve reasonable charge measurement accuracy. This has to be compared to the bench test measurements of the delay between separator output and first ADC signal sample. Right now this delay is about 440 ns, which should be satisfactory for most cases. As we said at the beginning, the FLASHlogic chips were not configured and, therefore, no integrator discharge and digitization occurred. The full timing scale pad pulses are shown in Figure 11.

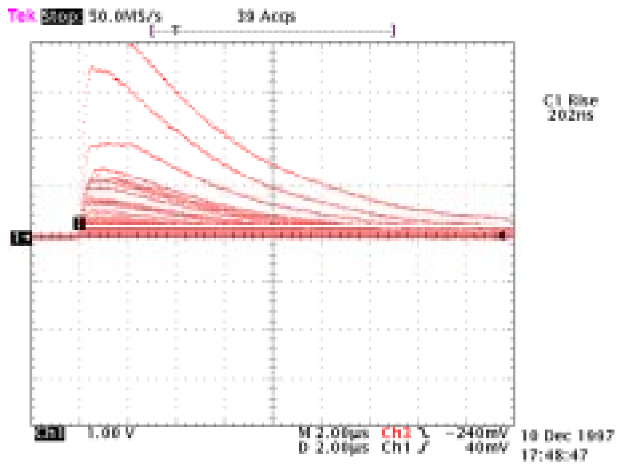

Figure 11. Pad A integrator pulse with infinite persistence @ 4800 V.

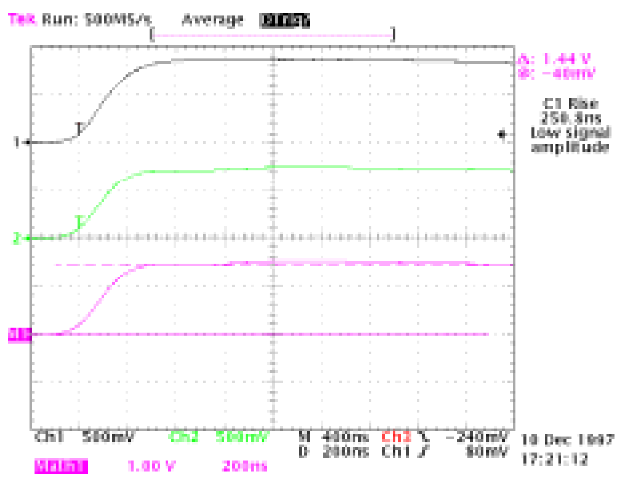

Figure 12. Average pad integrator pulses @ 4800 V (Pad A = Ch1, Pad B = Ch2, Math = Ch1 + Ch2).

Figure 12 shows average pad signals and also a sum of two (i.e. pad A and pad B). It was expected that pad A + pad B sum would represent gas multiplication factor and could be used to characterize it. We observed relatively big deviations in this value (30% and more) for several measurements. We explain that by wide dynamic range of the pad integrator (~5V) and contribution to the average from sparks and externally induced noise. The gain or conversion factor for pad integrator seems to be too high because corresponding ADC overflow limit is 1V. It might be necessary to reduce pad integrator gain in order to adjust signal dynamic range to the ADC limits.

3. Conclusion.

Final measurements with Control Board and local data acquisition system will allow to make fine adjustments for wire amplifier and pad integrator gain. Initial setting for wire amplifier looks adequate. Pad integrator may need reduction of the gain by some factor.