

PRELIMINARY TESTS OF THE FEB8

Preliminary testing was performed with 8-channel PDT Front-end Board prototype. The FEB8 was powered and supplied with 53 MHz clock and INIT and TEST signals using HP8130A and HP8110A programmable pulsers respectively. Special adapters have been used to apply high impedance source (current) signals to the FEB8 inputs. The following is a list of performed measurements and comparison to the original specification.

1. Power consumption. The estimated values for 24-channel FEB are ~8A on +5VD (digital), ~2.5A on +5VA (analog) and ~1.6A on -5A (analog) power supply. For the 8-channel prototype the following values have been measured with the clock signal applied: 0.66A on +5VD, 0.75A on +5VA and 0.45A on -5VA power supply. For full 24-channel board one can expect about 2.5 times higher value on +5VD and about 3.0 times higher values on +5VA and -5VA. Table 1 is a comparison of estimated and measured values.

Table 1. Power consumption estimates.

Power Supply	+5VD	+5VA	-5VA
Estimated (calculated) current [A]	8.0	2.5	1.6
Estimated for 24 channel current [A]	1.65	2.25	1.35

As one can see, the main error is in +5VD power supply current which can be explained by big uncertainties in FIFO memories power consumption.

2. Noise level and crosstalk. With 53 MHz clock and its sub-harmonics distributed over the PCB the level of crosstalks has to be noticeable. We have measured noise level of the

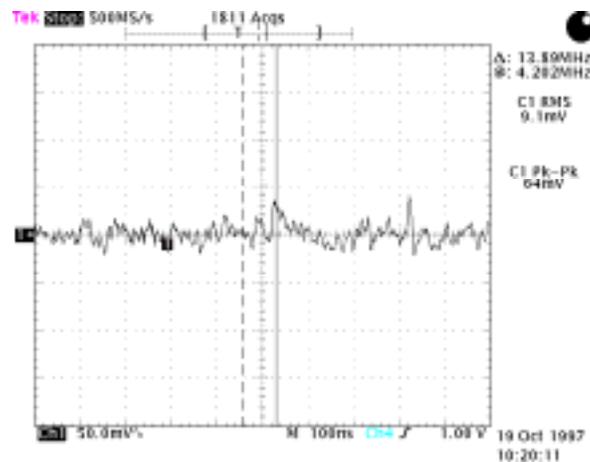


Figure 1. Wire amplifier noise level without clock signal.

wire amplifiers and pad integrators with and without the clock signal applied. Additional noise level due to the clock distribution is 7.8 mV RMS for WAD and 8..10 mV for PAI. Since no shielding was used in these measurements, the results are very preliminary (See **Figure 1** to **Figure 4**).

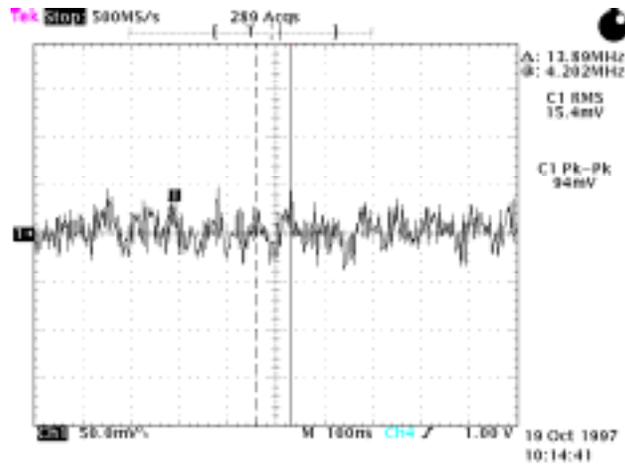


Figure 2. Wire amplifier noise level with clock signal.

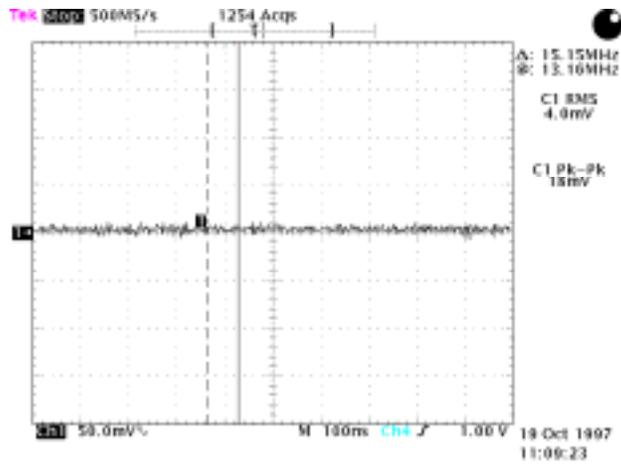


Figure 3. Pad integrator noise level without clock signal.

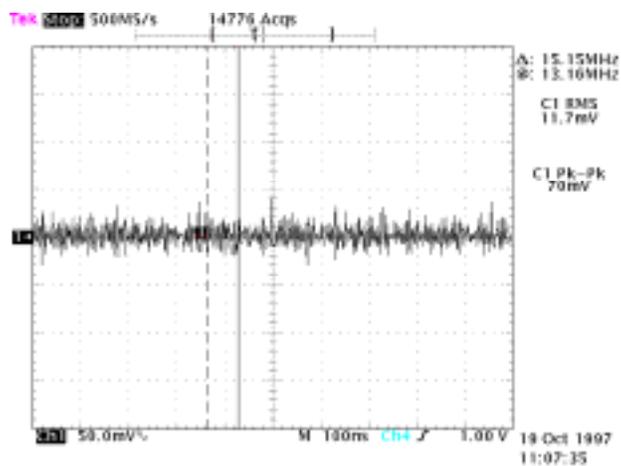


Figure 4. Pad integrator noise level with clock signal.

Additional measurements have been performed to check correlated noise from 3.3V switching converter. No correlation has been found (See Figure 5 and Figure 6).

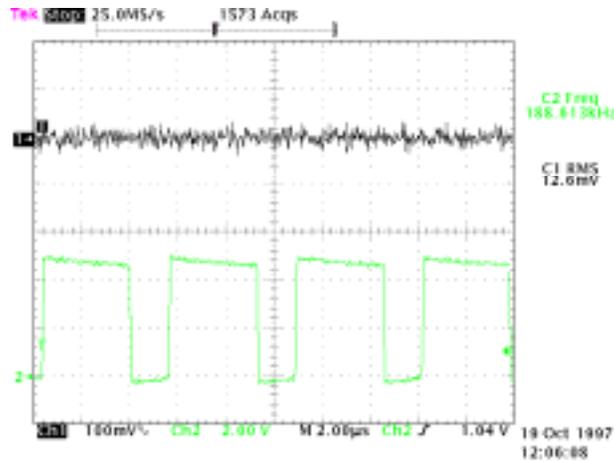


Figure 5. Wire amplifier noise correlated with 3.3V converter (Ch1 – pin 6 of HFA1135, Ch2 – pin 7 of MAX763A).

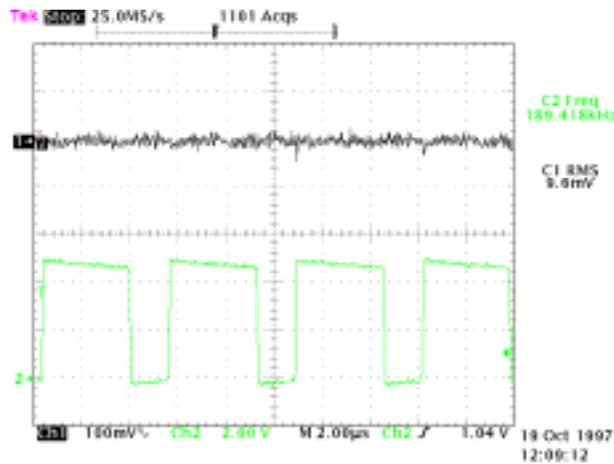


Figure 6. Pad integrator noise correlated with 3.3V converter (Ch1 – pin 6 of OPA660, Ch2 – pin 7 of MAX763A).

3. Wire Amplifier and Discriminator parameters. A 100 mV minimum discriminator threshold and a 100mV/ μ A amplifier gain was originally specified. The measured amplifier gain is 150 mV/ μ A. The gain and minimum discriminator threshold will be adjusted during PDT test with selected gas mixture. Right now the measured noise level is below 1 μ A threshold and can only contribute to the time resolution (15 mV RMS noise vs 100 mV threshold). A minimum discriminator pulse width has to be longer than 18.8 ns in order to allow synchronization of the wire separator circuit clocked at 53MHz. Also minimum interval between two same direction transitions of the discriminator output has to be greater than 37.7 ns which is required by the TMC spec. MAX903 positive feedback naturally provides these conditions. FEB threshold was set at \sim 1 μ A. The bandwidth of the amplifier is limited by the external LC network and can be adjusted (See Figure 7). Results of the double pulse resolution measurement with 1.5 μ A and 10 μ A input signals are shown in the Figure 8 and Figure 9. The on-board test pulser provides exponential pulse for all the channels using 50 ohm stripline and 10 k source resistors. The test pulse (at 2.0V analog voltage applied to the pulser) and amplifier output are shown in the Figure 10.

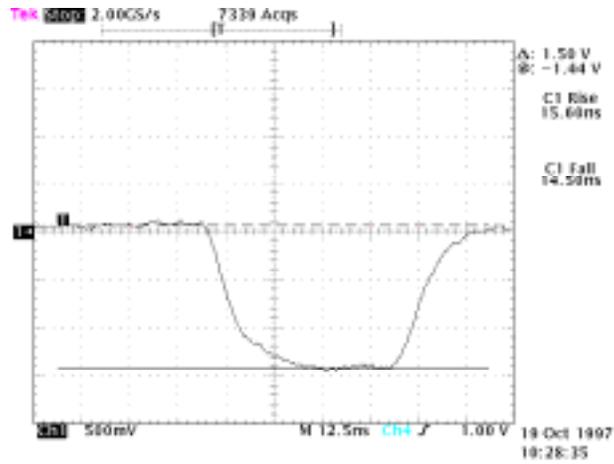


Figure 7. Wire amplifier output with 50 ns 10 μ A input signal.

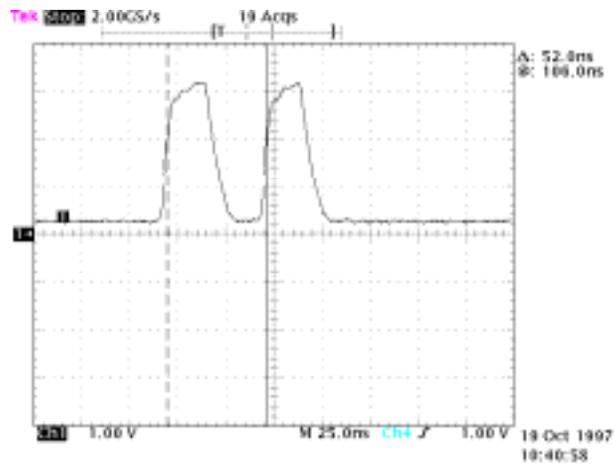


Figure 8. Double pulse resolution with 20 ns 1.5 μ A input signals.

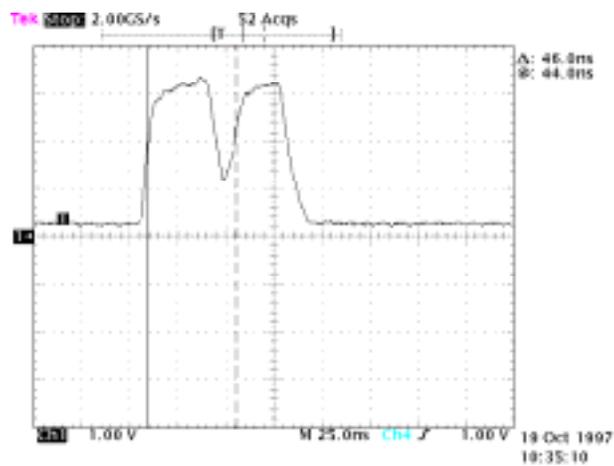


Figure 9. Double pulse resolution with 20 ns 10 μ A input signals.

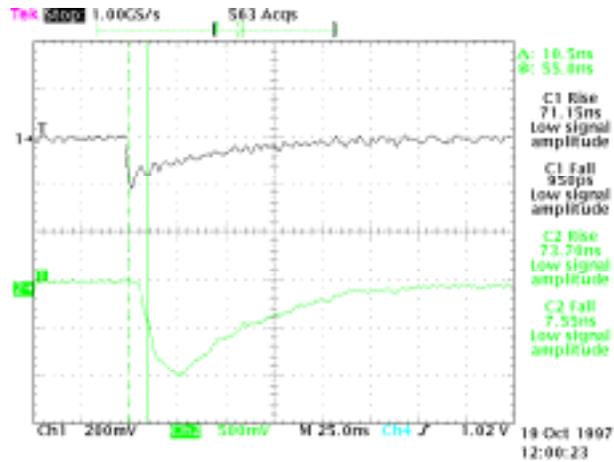


Figure 10. Test pulse @ 2.0V analog voltage (Ch1) and amplifier output (Ch2).

4. Pad Amplifier and Integrator parameters. The specified integrator gain is 300 mV/pC. The measured value is 220 mV/pC. Again, this parameter has to be adjusted after PDT test. The clock induced noise in the integrator is about 3.4 times higher than intrinsic integrator noise, and provides only 133:1 signal-to-noise ratio as to compare to the specified 200:1 value. There are certain things to improve in the board design besides measurements with the standard shields that can reduce the correlated noise level as well. Figure 11 shows integrator output with 2 pC input signal. If no wire signal detected, the integrator discharges with the time constant of about 5 μ s (See Figure 12). When wire signal at appropriate channel is detected the integrator is reset by RESET signal generated by ADC sequencer (Figure 13). Two integrator outputs are multiplexed at the ADC input at 53/8 MHz frequency (See Figure 14). Pad test signal (at 2.0V analog voltage) and corresponding integrator output are shown in the Figure 15.

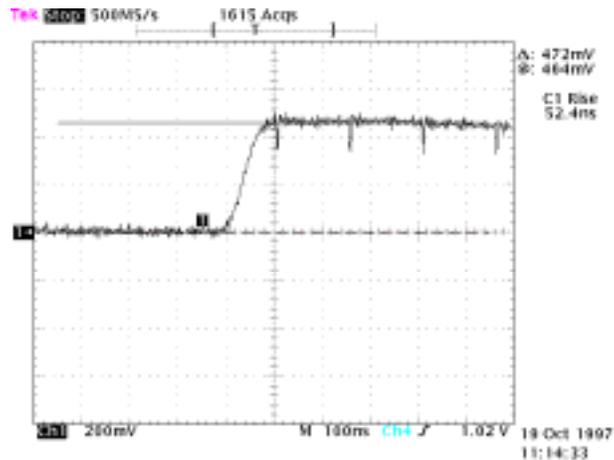


Figure 11. Pad integrator output at pin 6 of OPA660 with the input signal of 50 ns, 2 pC.

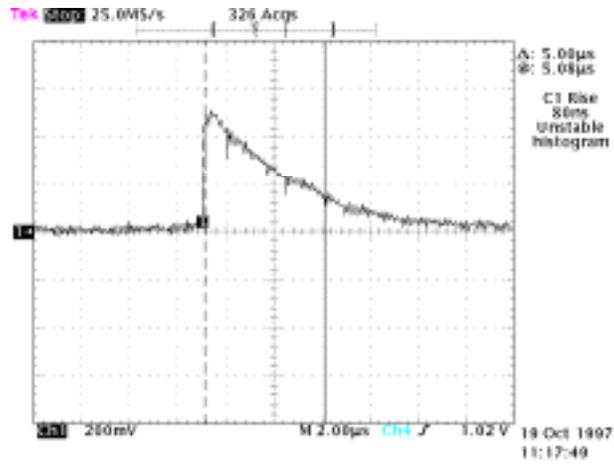


Figure 12. Pad integrator output at pin 6 of OPA660 with the input signal 50 ns, 2 pC (no wire signal applied).

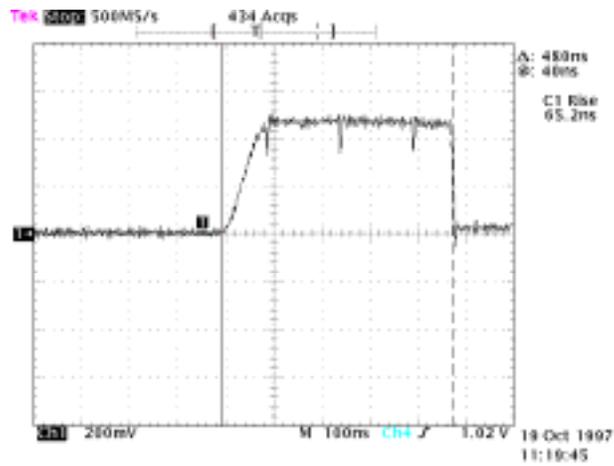


Figure 13. Pad integrator output with wire signal applied.

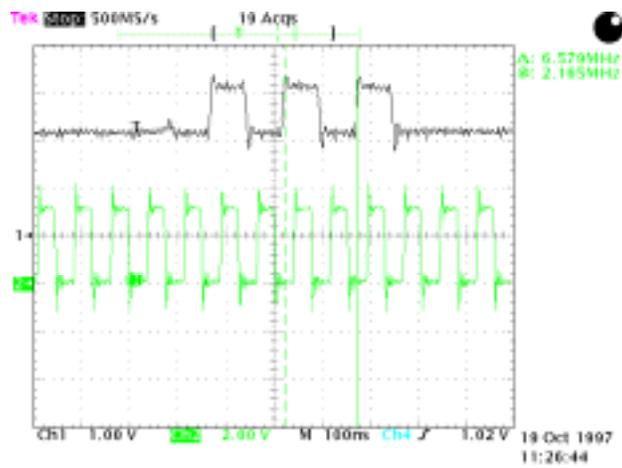


Figure 14. Ch1 – ADC input, Ch2 – ADC clock frequency.

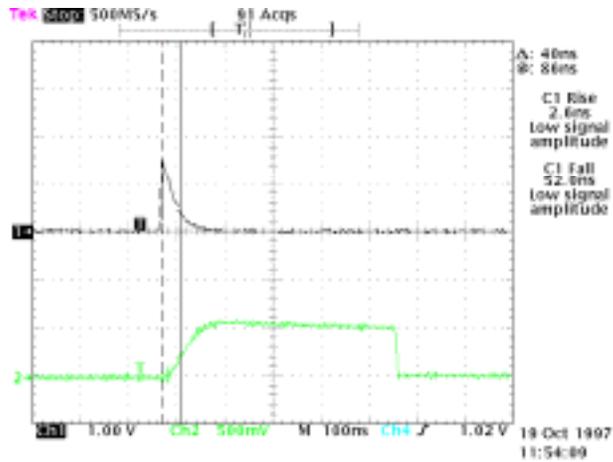


Figure 15. Pad test signal – Ch1 and integrator output – Ch2

5. ADC and Buffer timing. As one can see from the Figure 14, both ADC clock transitions are centered relative to the multiplexer output. This provides maximum margin for temperature and voltage deviations. The ADC sequencer generates flag bits to be stored along with

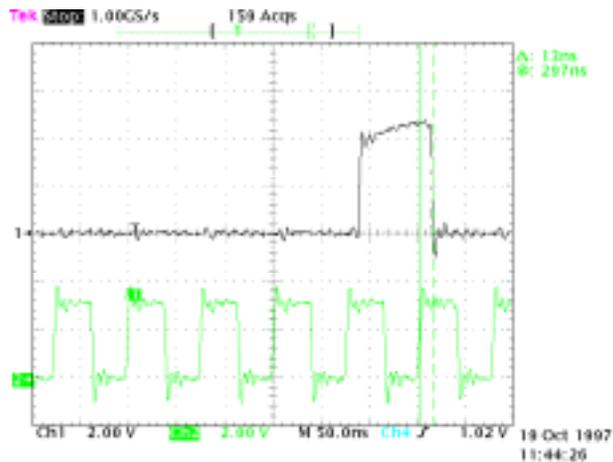


Figure 16. PAB flag bit – Ch1, FIFO WCLK signal – Ch2.

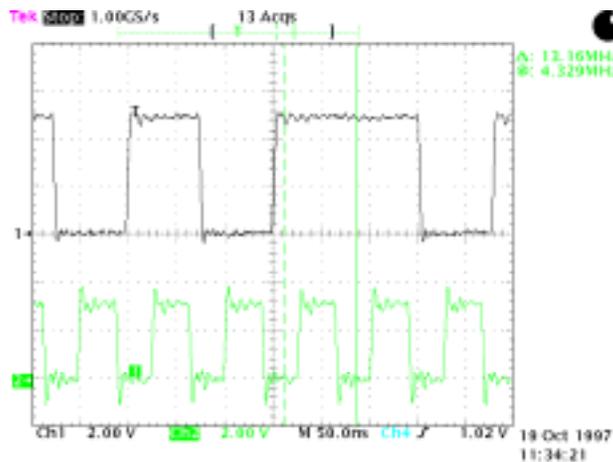


Figure 17. Buffer FIFO data input – Ch1, FIFO WCLK signal – Ch2.

ADC data in the buffer FIFO (CY7C4425). PAB flag signal is shown in the Figure 16 for example. ADC data relative to the buffer FIFO clock signal are shown in the Figure 17. Two ADC outputs are digitally multiplexed at the Level 1 FIFO inputs @ 53/2 frequency. One FIFO data input and clock signal are shown in the Figure 18.

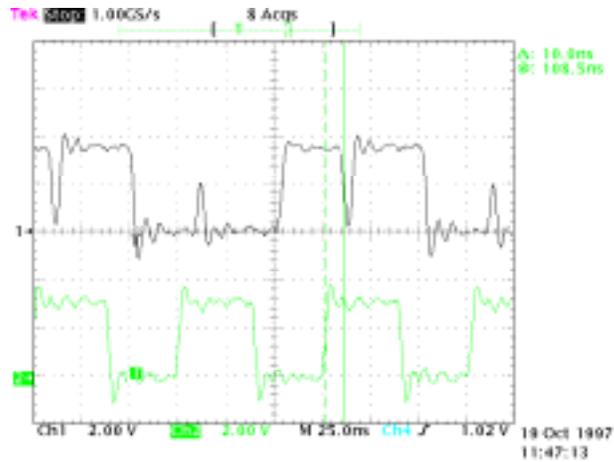


Figure 18. Level 1 FIFO data input – Ch1, FIFO WCLK signal – Ch2.

6. **TMC timing.** TMC chips are set to the maximum pipeline depth by INIT signal. There is no way to program CSR registers of the TMC without Control Board connection. In default state the TMC is running as shown in the Figure 19 and Figure 20. The cursor shows the position of the discriminator output pulse. To our surprise, we found very big deviation in the phase shift of the PLL clock relative to the external 53/2 MHz clock (31.5 ns). It was necessary to reverse both clock signals at the TMC inputs in order to satisfy setup and hold requirements of the Level 1 FIFO.

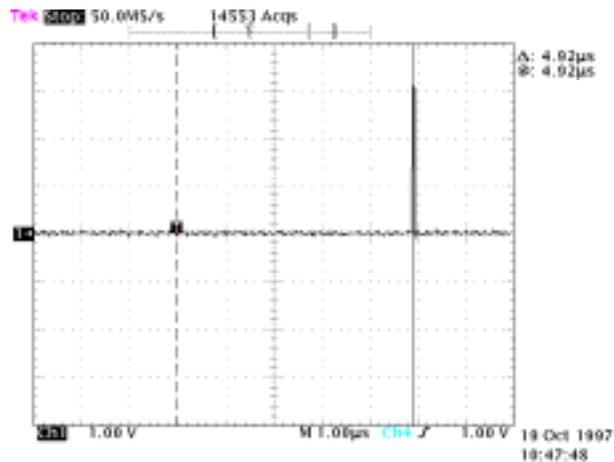


Figure 19. TMC hit bit vs discriminator output.

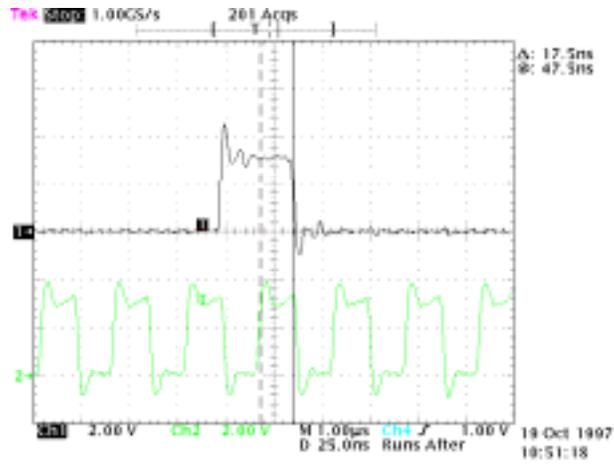


Figure 20. TMC hit bit sampling and hold condition.

7. Conclusion. Preliminary tests of the FEB8 show good agreement with the original specification. Further measurements with PDT and Control Board are necessary to adjust FEB parameters and study the nose performance.

References:

1. A. Khohlov et al., "MUON SYSTEM ELECTRONICS UPGRADE", D0 Note #3299, July 22, 1997, Fermilab.