

**TECHNICAL REPORT**  
**R&D "Tok"**  
**DOM Ampl-8 & Disc-8 ICs**

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**CONTENTS**

<b>1. INTRODUCTION</b>	<b>3</b>
<b>2. THE BJT-JFET TECHNOLOGY</b>	<b>3</b>
<b>3. THE FIRST ITERATION DESIGN</b>	<b>3</b>
<b>3.1 The current amplifier</b>	<b>3</b>
3.1.1 The amplifier circuit	3
3.1.2 The amplifier layout	5
3.1.3 The measurement results	6
<b>3.2 The discriminator</b>	<b>11</b>
3.2.1 The discriminator circuit	11
3.2.2 The discriminator layout	11
<b>3.3 Testing and Results</b>	<b>13</b>
<b>4. THE SECOND ITERATION OF DESIGN</b>	<b>15</b>
4.1 Contents of the second iteration	15
4.2 Current amplifier version 2 AMPL-8 v.2 (common-base)	15
4.3 The current amplifier version 3 AMPL-8 v.3 (cascode)	16
4.4 The discriminator version 2 DISC-8 v.3	16
<b>5. THE PACKAGE</b>	<b>19</b>
5.1 Present industry practicality	20
5.2 Testing	20
5.3 Resistance to mechanical action exposure	21
5.4 Climatic resistance:	22
5.5 Glue	22
5.6 The aim of the package design	23
<b>6. THE AMPLIFIER-DISCRIMINATOR MULTILAYER PCB (VERSION 1.0)</b>	<b>23</b>

## *INTRODUCTION*

Two IS's having common designation DOM ("Dubna+D0+Minsk") have been designed in the frame of the R&D:

- 8-channel current amplifier/shaper IC named Ampl-8;
- 8-channel discriminator IC named Disc-8.

The pilot batch (10 wafers) have been produced in February, 1997. The chips were packaged and measured. On the base of the first iteration measurement results obtained the second iteration has been started. The discriminator circuit has been subjected to negligible correction (outputs have been made slightly more powerful). In the current amplifier chip the bases of reference common base amplifier stages were connected to separate pins to permit compensation of output level shifts by external OpAmps. In addition, a new cascode-based current amplifier version has been designed and put in production.

A special aluminium package has been designed and produced for the ICs.

32-channel PCB has been designed and put in production.

## *THE BJT-JFET TECHNOLOGY*

The element base used in this design carried out in the BJT-JFET technology [1] has the next features:

- Only npn BJTs and pJFETs are used as active devices.
- Presence of two buried layers  $n^+$  and  $p^+$  in n-type epitaxial structures.
- Combined isoplanar oxide isolation.
- Self-alignment of  $n^+$  gate and  $n^+$  emitter areas.

The BJT-JFET technology has the following features:

- Application of ion doping only.
- Boron doping through a preliminary grown thermal oxide.
- Simultaneous forming of different conductivity type regions.
- The technological process includes 14 photolithography operations, 8 ion doping ones and has a block structure.
- Two-level metallization.

The technology permits to have the input npn with a transition frequency  $f_T = 3\text{GHz}$  and common emitter current gain  $\beta \approx 80$ . Low power pJFETs have  $f_T = 300\text{MHz}$ . and can be placed in any part of a chip. The technology proves to possess good radiation hardness to neutrons [2].

## *THE FIRST ITERATION DESIGN*

### The current amplifier

The amplifier circuit

One channel of the 8-channel current amplifier AMPL-8 (Fig.3-1) consists of an input stage of common base/common collector configuration ( $Q28, R23, Q29, Q30, R10$ ) (Fig.1), two voltage amplifier differential stages ( $Q32, Q31, R34, R35, Q33,$



$R26$  and  $Q38$ ,  $Q40$ ,  $R36$ ,  $R37$ ,  $Q39$ ,  $R28$ , respectively), two output emitter followers  $Q45$ ,  $Q47$ ,  $R30$  and  $Q46$ ,  $Q48$ ,  $R31$ , respectively), and a stage to stabilise amplifier constant current operation conditions and to compensate crosstalks ( $Q51$ ,  $R42$ ,  $R41$ ,  $Q52$ ,  $Q53$ ,  $R40$ ).

The common-base input circuit  $Q28$ ,  $R24$  is made of a low-noise UHF npn transistor ( $R_{bb'} \leq 300\Omega$ ,  $f_T > 3\text{GHz}$ ). It operates at large collector current, the common-base configuration provides low input impedance in wide frequency band. The amplifier input is protected from positive ( $Q38$ ) and negative (a chain of two large-area diodes,  $Q2001$ ,  $Q3001$ ) overvoltage pulses.

The common base stage provides low input impedance and converts of input current pulse into voltage on the resistor  $R23$ . Differential stages provide voltage gain required. The emitter followers  $Q34$ ,  $Q37$  and  $Q41$ ,  $Q44$  with diode chains match constant current levels between the stages, and the emitter followers  $Q45$ ,  $Q47$  and  $Q46$ ,  $Q48$  provide required output capacity.

The amplifier circuitry feature is the method to establish  $Q31$  base potential. For this purpose the common base/common collector stage ( $Q51$ ,  $R42$ ,  $R41$ ,  $Q52$ ,  $Q53$ ,  $R40$ ) is used, which is similar to the input stage but having collector currents exactly 10 times smaller.

Signal shaping is carried out on the differential stage transistors' ( $Q31$ ,  $Q32$ ,  $Q38$ ,  $Q40$ ) collector capacitances and their loading resistors ( $R34 - R36$ ).

The amplifier layout

The layouts of one channel of AMPL-8 (fig.2) has following features:

- The channel has width  $320\ \mu$ . It is determined by dimensions of two contact pads and minimum gap between them ( $100\ \mu + 100\ \mu + 60\ \mu + 60\ \mu = 320\ \mu$ ).
- Each channel is shielded by a contact to a substrate connected by metal lead to a separate contact pad (SUB) having no contact with a voltage supply line.
- Each Ampl-8 channel has diode voltage protection against positive and negative overvoltage pulses by diodes introducing  $8.52\text{pF}$  stray capacitance. All protective diodes of both polarities consist of two sections, what makes it possible to reduce the stray capacitance by half at the cost of 50% reduction of the diode area with correspondent decrease of current passed. Similar test protective elements are formed separately to investigate their characteristics.
- Each input of the Ampl-8 channel has separate ground line PGND beginning from the input transistor base, these lines are not connected inside the chip.
- The eight channels have common ground line VGND which ties collectors of transistors  $Q50$ . Varying the value of an external resistor  $R_{ext}$  connected to this point and/or the positive supply voltage one can regulate operation mode of all the Ampl-8 transistors except the input transistors  $Q28$ ,  $Q51$ .

- There are separate contact pads tied to a substrate in the Ampl-8 and Disc-8 which have no connections to negative voltage supply source. Applying large negative potential limited by breakdown voltage to the substrate, one can substantially decrease stray capacitances between IC devices and the substrate, i.e. interelement and interchannel couplings.

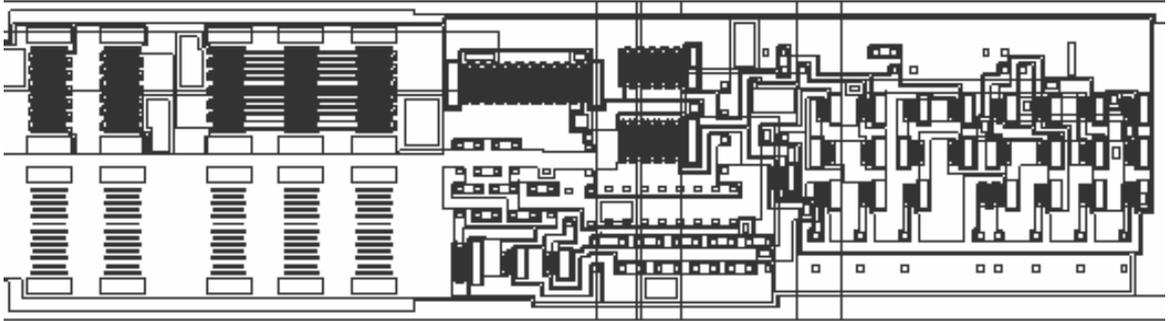


Fig. 3-2. The single channel current amplifier layout

#### The measurement results

The Ampl-8 amplifiers were tested on a test bench. The detector was simulated by a cut of  $50\Omega$  cable 60cm long having capacitance 60pF. The input signal (Fig.3-3) was simulated by RC-circuit shown in Fig. 3-1 at the input of the amplifier between a pulse generator and a long line..

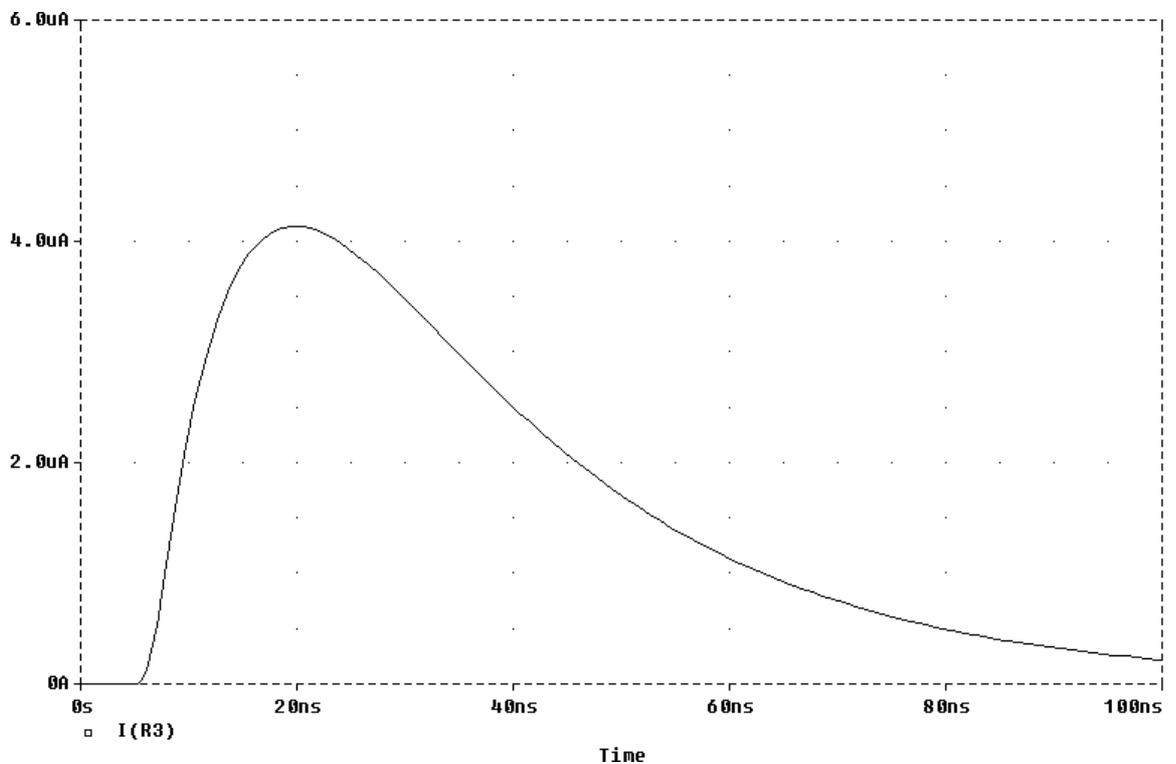


Fig.3-3. The test signal

Supposed and measured characteristics of the current amplifier AMPL-8 are shown in Table 3-1.

Table 3-1. The current amplifier specification

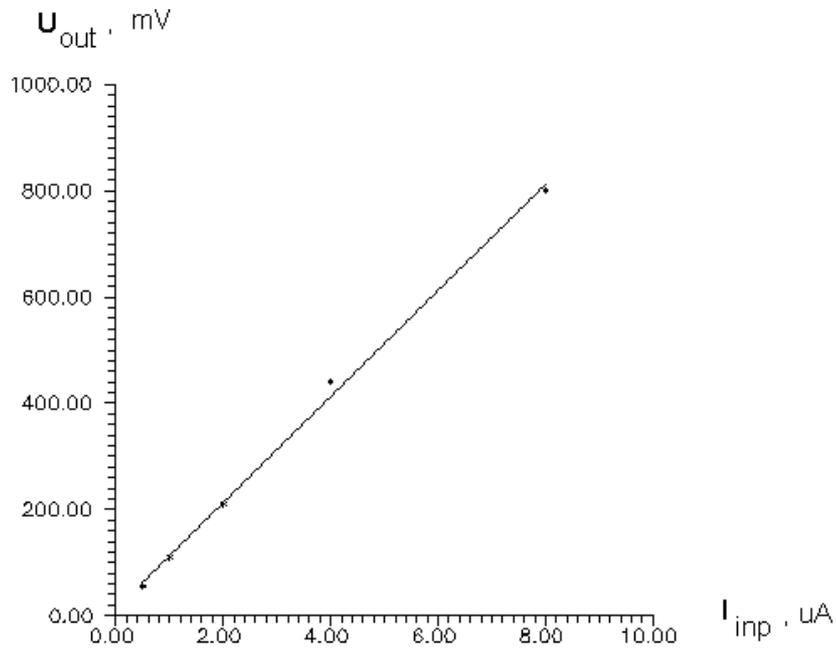
Parameters	Supposed value	Measured value
Current gain	100 mV/ $\mu\text{A}$ (50 mV/ $\mu\text{A}$ per arm) <sup>*1</sup>	
ENC for detector capacitance:	4000	not measured
$\tilde{N}^{el} = 0$ , r.m.s. electrons,	8000	$\leq 13800$
$\tilde{N}_s = 60$ pF, r.m.s. electrons,		
Output signal leading edge	5-7	8
Input dynamical range, dB	60	
Input signal polarity	$\pm$	$\pm$
Input impedance, $\Omega$	10	$\leq 10$
$\pm$ overvoltage protection	Yes	Yes
Channel number	8	8
Input linear range	40	
Differential output	Yes	Yes
Available output load, $\Omega$	50-2000	
Cross-talks, dB	-46	$< -25$
Voltage supply, V	$\pm 5$	$\pm 5$
Dissipated power, mW/channel	<sup>*2</sup> -	75
Package	To be chosen	Custom QFP-48-1.27

The dependence of amplifier output voltage on input current for different resistor load is shown in Figs. 3-5 - 3-8.

From Figs. 3-6, 3-8 it is seen that the negative arm can not provide sufficient current. To increase the output current the output stage current mirrors were shunted by external resistors. The output signals for the case of shunting by 2.4k $\Omega$  resistors are shown in Figs. 3-9, 3-10.

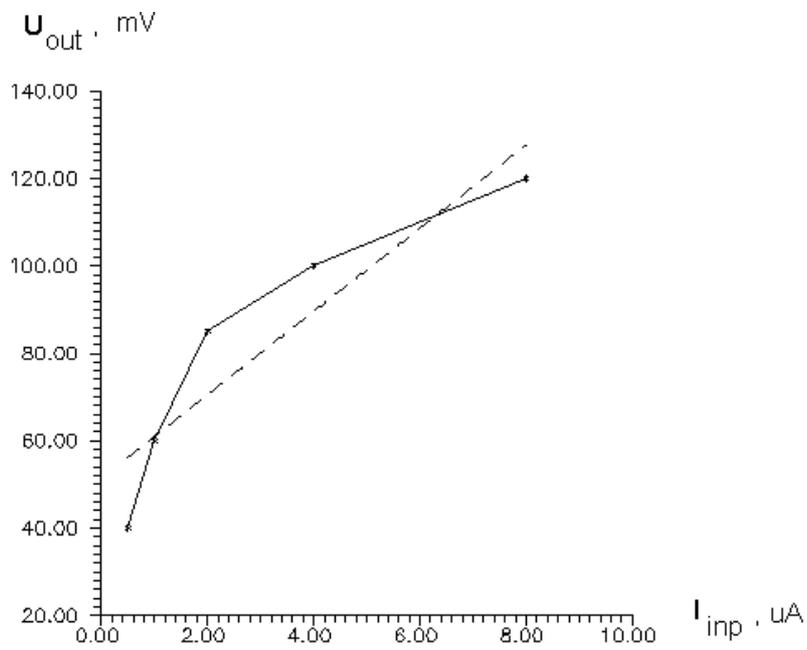
<sup>1</sup>When loading by comparator at 1 k $\Omega$

<sup>2</sup> To be minimized.



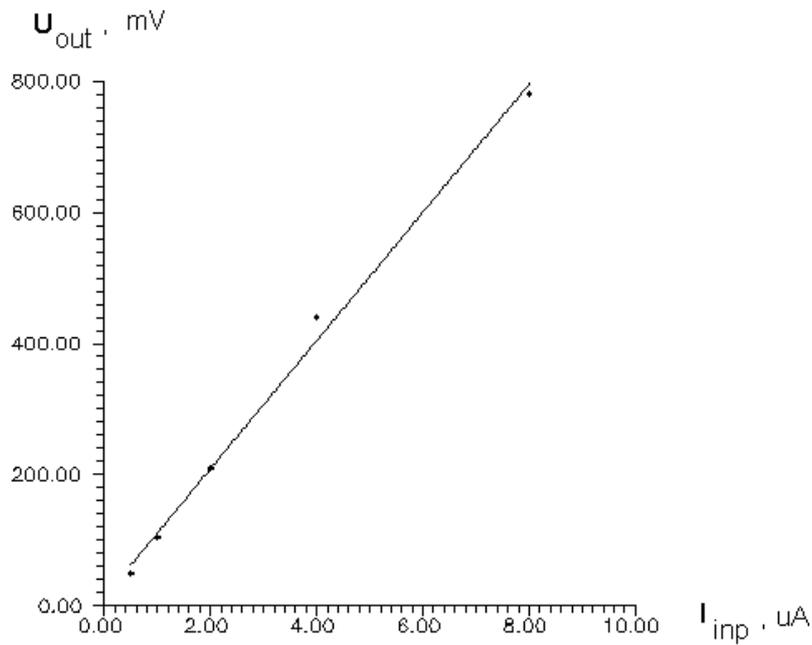
Best Fit:  $Y = 99.7581X + 13.75$

Fig.3-5. Output voltage versus input current (positive arm, 51 k $\Omega$  load)



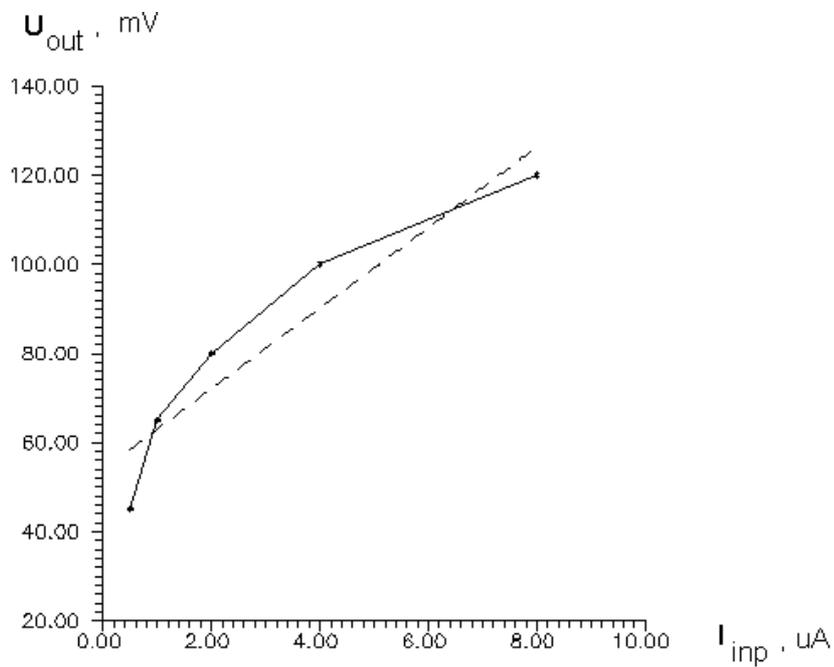
Best Fit:  $Y = 9.52957X + 51.4583$

Fig.3-6. Output voltage versus input current (negative arm, 51 k $\Omega$  load)



Best Fit:  $Y = 97.7554X + 13.9583$

Fig.3-7. Output voltage versus input current (positive arm, 1 k $\Omega$  load)



Best Fit:  $Y = 9.0457X + 53.9583$

Fig.3-8. Output voltage versus input current (negative arm, 1 k $\Omega$  load)

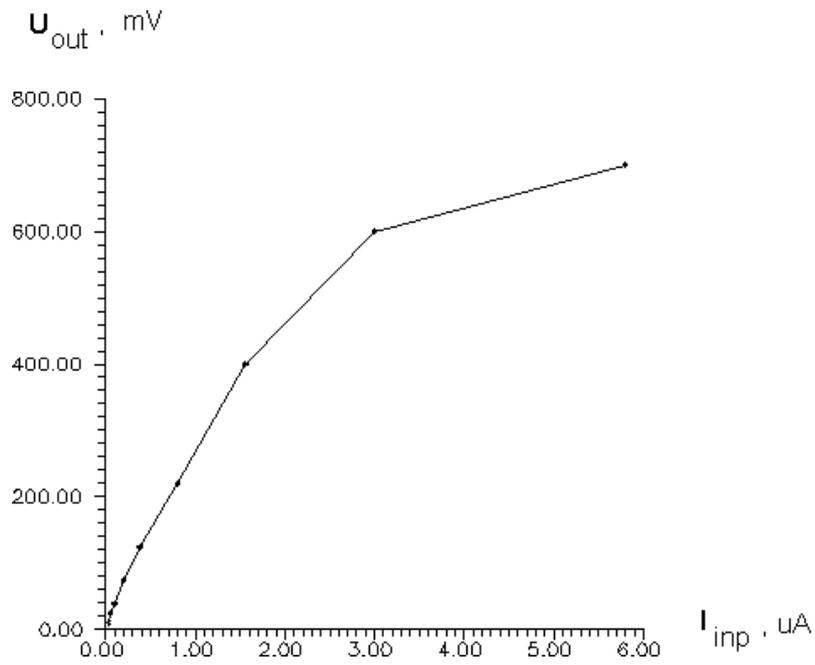


Fig.3-9. Output voltage versus input current (positive arm, 51 k $\Omega$  load, 2.4 k $\Omega$  shunting)

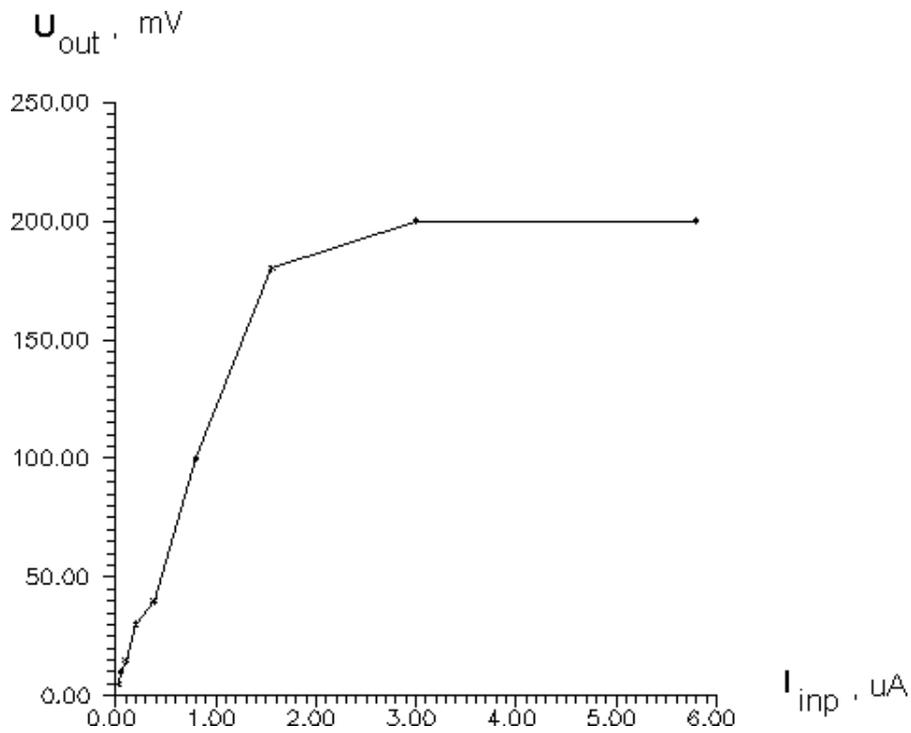


Fig.3-10. Output voltage versus input current (negative arm, 51 k $\Omega$  load, 2.4 k $\Omega$  shunting)

## The discriminator

### The discriminator circuit

The discriminator consists of eight parallel channels having common voltage supply lines and maximum load current control. To extend the discriminator's application capabilities we have taken a decision to make no built-in threshold control circuits inside the IS. Implementation of open collector output stages makes it possible to obtain various output signal amplitudes with dc level in the range from 0 V to 5 V (ECL, NIM, TTL).

A circuitry of a single channel is shown on Fig.3-11. The discriminator has three differential stages, the first and the second one (with resistor load) provide voltage amplification required, the third one (with open collector) is intended to feed an internal load. The comparator has a differential input and a complementary current output. The first differential stage Q1, Q2 is loaded by the common base stages Q4, Q5 to decrease Miller's effect and influence of input capacitance. The second differential stage has similar construction. The oppositely connected diodes Q19, Q20 clip maximum voltage amplitude between the collectors of Q9, Q10 providing an increase of speed. The emitter followers Q6, Q7, Q12, and Q13 with Zener's diodes D1-D4 match constant voltage levels between the differential stages. The second differential stage is lapped by the frequency independent feedbacks coming through the resistors  $R23=R24=1.2\text{ k}\Omega$ ,  $R25=R26=7\text{ k}\Omega$ ,  $C1=C2=2.1\text{ pF}$ , which forms pulses 60 ns

long at the output of the comparator. Leads of the resistor R8 of each channel are combined together and outputted to the separate ground pin VGND, permitting to control the output current by changing potential at this pin or by increasing R8.

### The discriminator layout

Layout of one channel of the discriminator is presented on Fig.3-12.

Dimensions of one discriminator channel without contact pads equals  $320\mu \times 770\mu$ , and the area of the 8-channel discriminator die with contact pads is  $1.1 \times 2.9\text{ mm}$ . The channel width is determined by minimum sizes of the contact pads ( $100\mu$ ) and admissible gaps between them ( $60\mu$ ). It should be noted that channels of both Ampl-8 and Disc-8 have the same width, what makes it possible in future to joint them into single amplifier/discriminator chip with dimensions  $3.3\text{mm} \times 2.3\text{ mm}$  (together with test elements, marks and so on).

The layout of the comparator has following features:

- Each channel is shielded by a contact to a substrate, which is connected by metal lead to a separate contact pad (SUB) having no contact with a voltage supply line.
- The zero potential line (GND) has two contact pads connected in parallel.
- The Zener's diodes are comprised of a reverse biased emitter junction of a npn transistor with the collector being connected to positive voltage supply line.

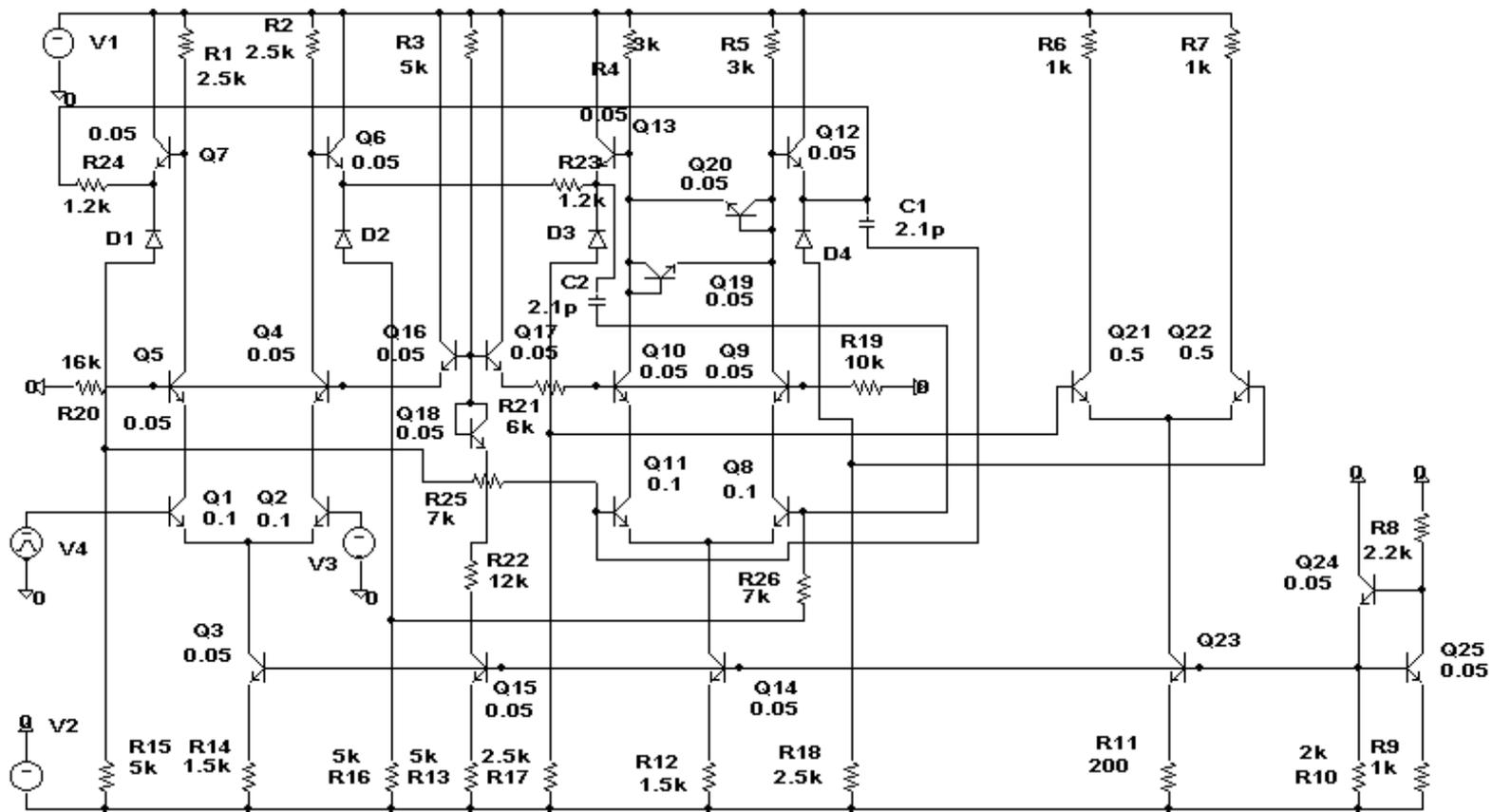


Fig 3-11. The circuit of the discriminator DISC-8 version

1

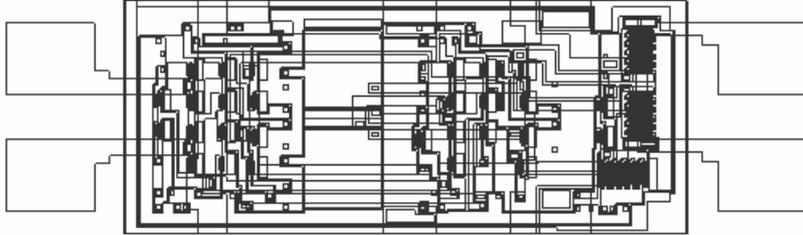


Fig.3-12. The discriminator v.1 single channel layout

- To decrease the stray capacitances of collectors of the Q9/Q10 collectors the oppositely connected diodes Q19, Q20 have been made by means of additional p-area formed in the epitaxial well of the npn transistor.

### Testing and Results

To test the chip the probe card was designed which contained eight channel zero-crossing discriminator. The discriminator's parameters measured are presented in Table 3-2.. The chip has good speed: the 1/0 and 0/1 edges are 1.8 ns and 2.2 ns when operating on 110  $\Omega$  load (twisted pair wire). Identity of propagation delay from channel to channel is less than 4 ns. The output was designed to provide operation on differential line driver DS90C031 with 20 m twisted pair line 20 m long. Dissipated power is 84 mW/channel.

Table 3-2: Specifications of the eight-channel comparator IC

Parameter	Value
Supply voltage, V	+5, -5
Supply current $I^+$ , $I^-$ , mA	$\leq 65$ ,
	$\leq 69$
Supply current $I^+$ , $I^-$ /chan, mA	$\leq 8.2$ ,
	$\leq 8.6$
Channel number	8
Offset, mV	$\leq$
Output current, mA	$\leq 4$
Input current difference, $\mu\text{A}$	$\leq 0.01$
Input current, $\mu\text{A}$	$\leq 1$
Propagation delay at 10 mV/60 mV, ns	$\leq 36$ ,
	14
Output signal edge 01/10, ns	2.2 /
	1.8
Maximum propagation delay difference, ns	$\leq 4$ , $< 1$

The dependence of propagation delay on overdrive is shown in Fig.3-13.

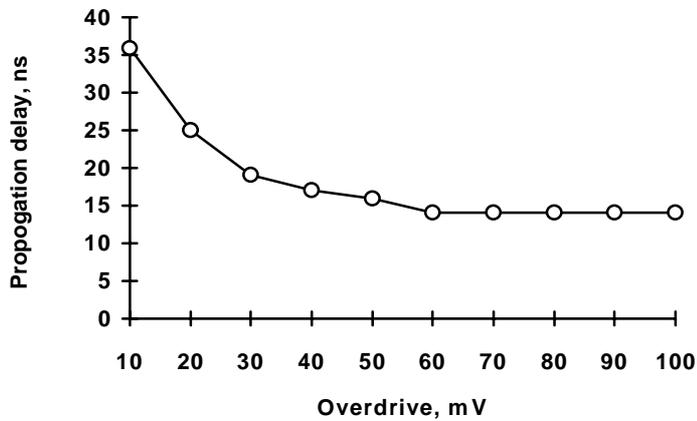


Fig.3-13. The dependence of propagation delay on overdrive.

Time walk was measured to be 3.8 ns for two input pulse amplitudes 20 mV and 100 mV ( $2Q_{th}$  and  $10 Q_{th}$ ) at the threshold corresponding to the amplifier input current 0.5  $\mu\text{A}$ .

## *THE SECOND ITERATION OF DESIGN*

### Contents of the second iteration

Simultaneously with fabrication of wafers for the first iteration design another batch of wafers was started which had been stopped before formation of metal wiring layers. During the second iteration we have made new photomasks for metal layers, thereby changing circuits of amplifier and discriminator according to the test results for the first iteration ICs. In such a manner we have put in production two new versions of the current amplifier, AMPL-8 version 2 with common base input stages and AMPL-8 version 3 with cascode input stages, and one new version of the discriminator, DISC-8 v.2.

### Current amplifier version 2 AMPL-8 v.2 (common-base)

In basic configuration of AMPL-8 v. 1 (Fig.3-1) with the common-base input stage an additional input has been added connected to the reference-stage input-transistor base to provide balance of the amplifier differential outputs by an external OpAmp separately in each channel. Pspice simulation has confirmed the possibility of such adjustment. When this idea will be confirmed on physical chips those OpAmps will be embedded into the chip. Moreover, the base of input common-base transistor is connected to the collector of Q7 (these points of all channels are jointed and outputted to the VGND pin) inside the chip hereby providing possibility to connect the amplifier's inputs directly to the detectors' outputs by separate two-wire lines without joining together their ground lines to diminish possible cross-talks. The AMPL-8 v.2 layout is shown on Fig.4-1.

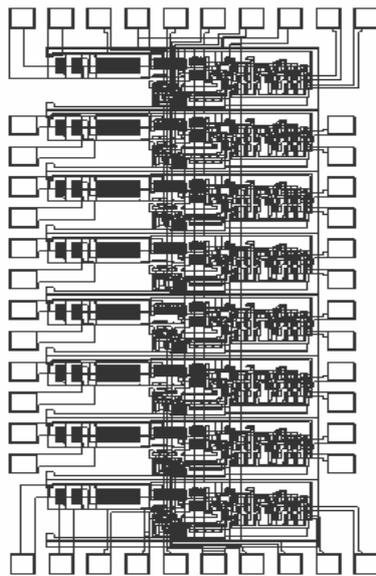


Fig 4-1. The layout of AMPL-8 v.2 (common base)

### The current amplifier version 3 AMPL-8 v.3 (cascode)

On the base of transistors and resistors formed on the production of the AMPL-8 v.1 another current amplifier circuit has been designed having input cascode stage instead of common base one (Fig. 4-2). Greater amplification of this cascode input stage make it possible to exclude the second differential amplifier stage providing more advantageous conditions to balance the outputs for DC. The free devices of this eliminated stage were used to increase available output current of the amplifier and to build an additional separate output-stage current mirror with possibility to program the steady state current to operate with different loads. DC balance is provided by choice of an external feedback resistor in the reference stage (Pspice simulation shows proper operation of the amplifier with deviation of the resistor in the range of  $\pm 20\%$  relative the nominal value  $110\text{ k}\Omega$ ). Experimental check of this approach will be carried out after fabrication of the chip ( the number of AMPL-8 v.3 chips will be 1/3 of total number of amplifier chips in the second iteration).

The input impedance should be equal to  $150\Omega$ . The circuit will be stable without an input load.

The layout of the chip is shown in Fig.4-3.

### The discriminator version 2 DISC-8 v.3

In the basic discriminator circuit (Fig.3-11) an additional output from the resistor R8 has been made for separate control of the current mirror, permitting to vary output stage current in the range of  $\pm 20\%$ . Another parts of the circuit have not changed. The layout of the chip is shown in Fig. 4-4.

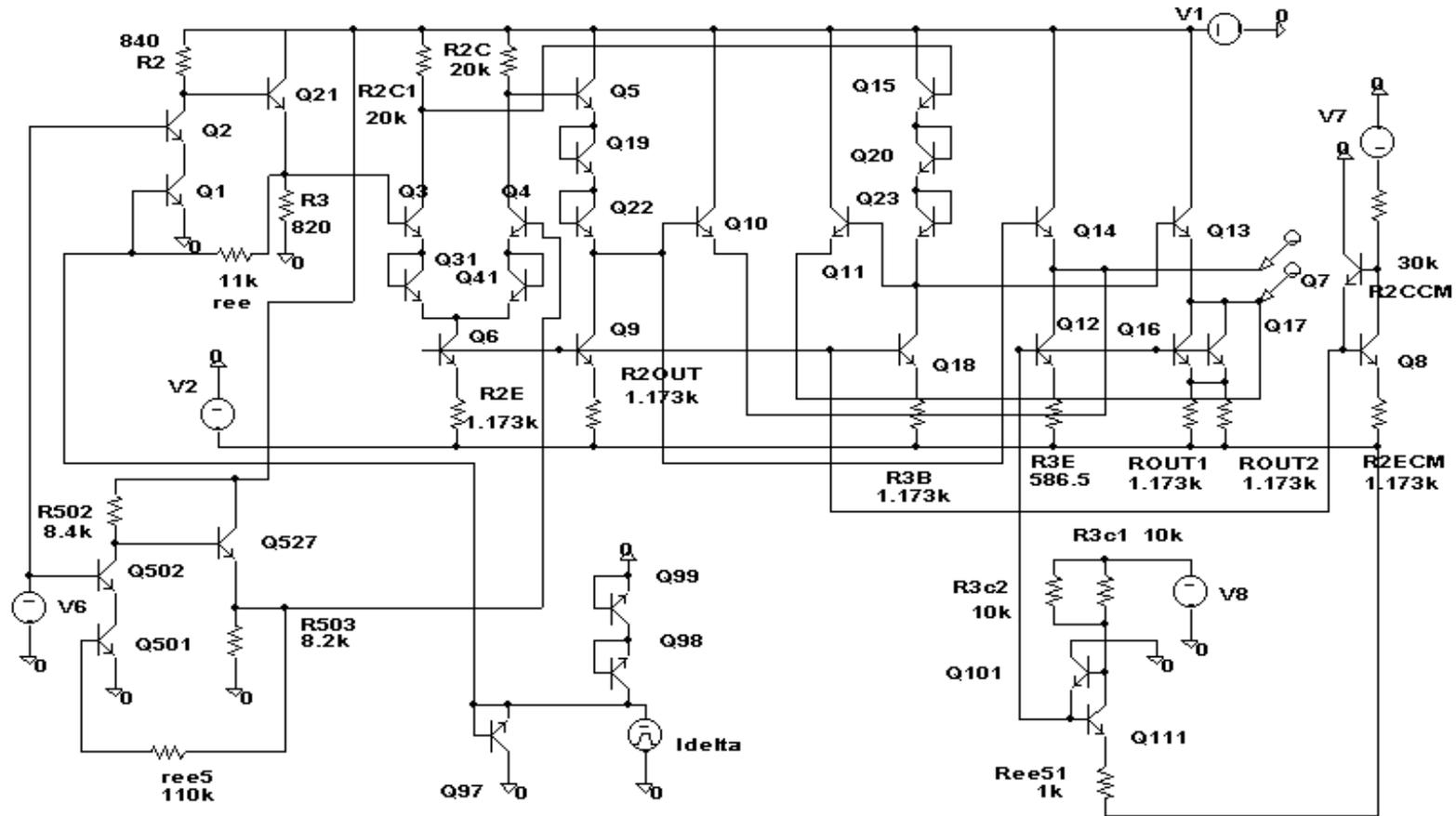


Fig.4-2. The cascode current amplifier AMPL-8 v.3

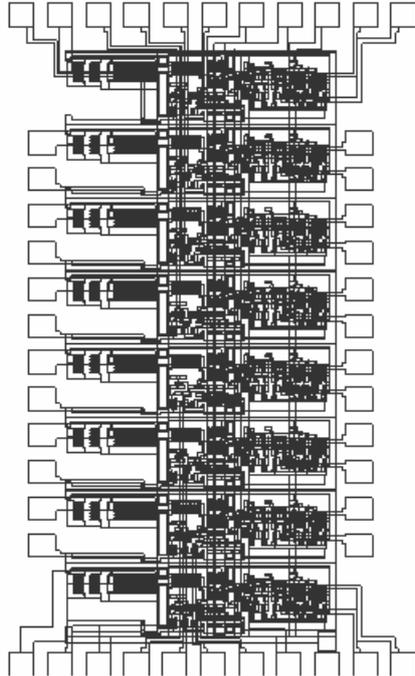


Fig.4-3 The cascode current amplifier AMPL-8 v.3

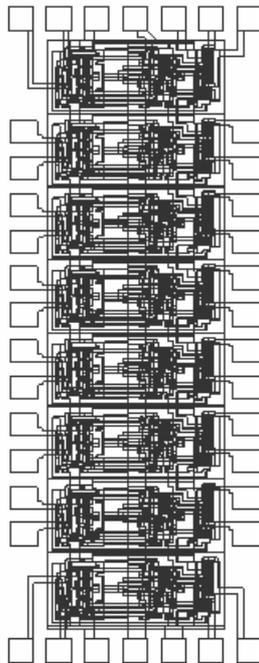


Fig.4-4. The discriminator DISC-8 v.2 layout.

### THE PACKAGE

The IC is encapsulated in a 48-pin four-side planar package. The package has been designed especially for the D0M Ampl-8 and Disc-8 ICs. It consist of an aluminium base, a covar leaded chip carrier (mounting pad), and a covar grounded cover. The package pinouts for the chips are shown in Figs.5-1 - 5-3

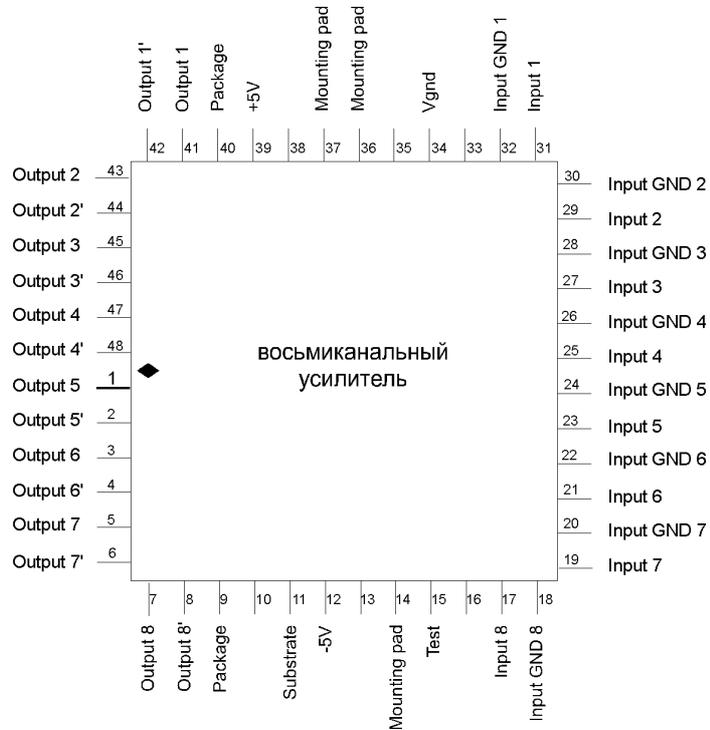


Fig. 5-1. The pinouts for AMPL-8 version 1

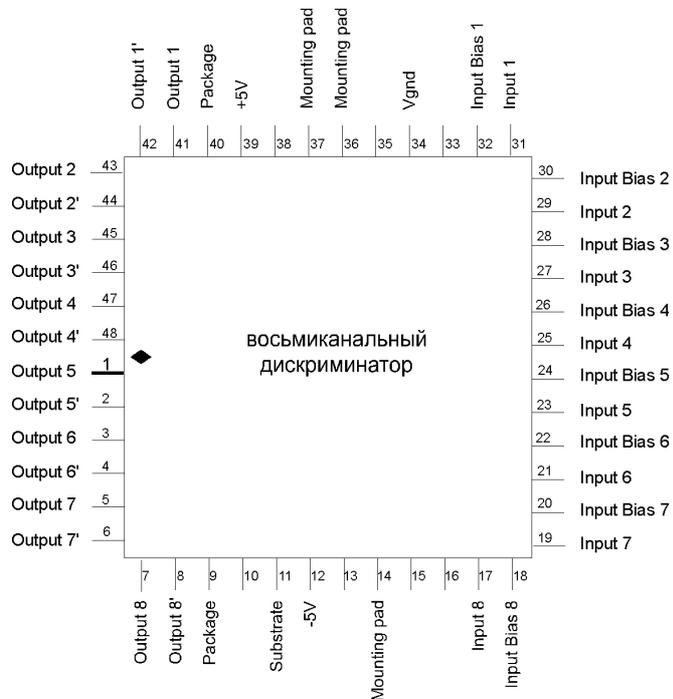


Fig. 5-2. The pinouts for DISC-8 version 2

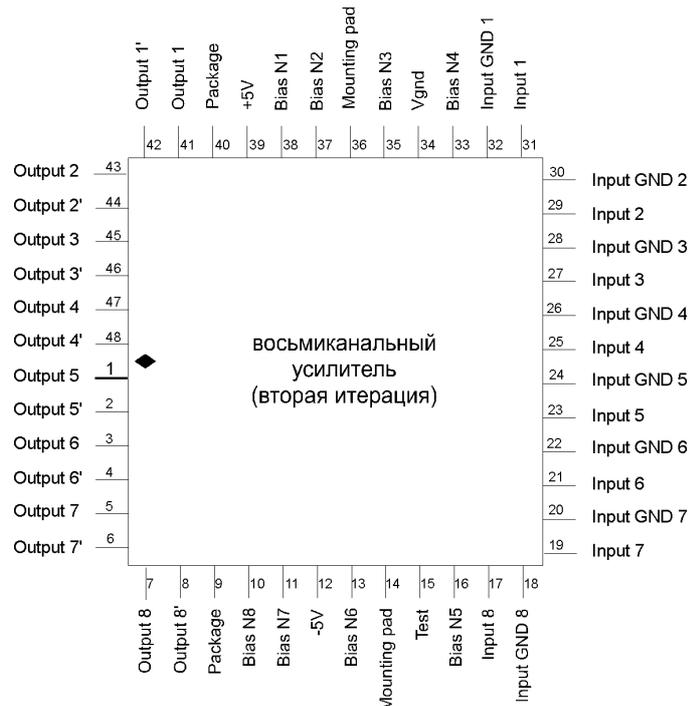


Fig. 5-3. The pinouts for AMPL-8 version 2

### Present industry practicality

At present "Integral" applies in mass-production the following types of oxidised-aluminium packages:

- 48 pins with 1.25 mm and 1.0 mm pitch (2 versions)
- 64 pins with 1.25 mm and 1.0 mm pitch (3 versions)
- 100 pins with 1.25 mm and 0.625 mm pitch (2 versions)
- 84 pins with 1.27 mm
- 24 pins with 1.25 mm
- 124 pins with 0.625 mm and 0.625 mm pitch (2 versions)
- 17 pins with 1.27 mm (2 versions)

All the aforementioned packages have technical documentation and technological tried-out production process. So the oxidised-aluminium packages appears to be rather traditional construction solution.

### Testing

The 16-pin square four-side oxidised aluminium package (analogue of the commercial ceramic-metal package H04.16-1B UFO.481.005 TU) containing the monolithic integrated circuit HT011 have passed test in Minsk Scientific Research Instrument Institute according to GOST 20.57.406-81 (GOST 20.57.406 Products of electronics engineering, quantum electronics, and electrical engineering. Test methods) by the following methods:

- Short-term vibration strength test in accordance with the method 103-2 GOST 20.57.406 (9-th degree of stiffness) without electrical feeding of the IC;
- Impact resistance test in accordance with the method 104-1 GOST 20.57.406 (1-st degree of stiffness) without electrical feeding of the IC;

- Single impact resistance test in accordance with the method 106-1 GOST 20.57.406 (3-rd degree of stiffness) without electrical feeding of the IC;
- Pin stretching strength resistance test in accordance with the method 109-1 GOST 20.57.406 (pin number = 3);
- Pin bending resistance test in accordance with the method 110-1 GOST 20.57.406 (the number of pin subtracted to the test was equal to 3, bending were made in one direction, the bending number = 3);
- Pin soldering ability test in accordance with the method 402-1 GOST 20.57.406. Temperature of a soldering bit tip = 280°C.
- Soldering heat stability test in accordance with the method 403-1 GOST 20.57.406. Temperature of a soldering bit tip =280°C, distance between the package and pin soldering point not less than 1 mm.
- Ambient temperature change resistance test in accordance with the method 205-1 GOST 20.57.406. Test number = 3. Holding time in every heat chamber = 0.5h. Holding time at normal conditions after testing = 0.5h.
- Increased ambient temperature test in accordance with the method 201-2.1 GOST 20.57.406. Holding time in heat chamber = 0.5h. Holding time at normal conditions after testing = 0.5h.
- Increased humidity test in accordance with the method 207-2 GOST 20.57.406 (3-rd degree of stiffness). Test duration - 4 days (96 h).
- Decreased ambient temperature test in accordance with the method 203-1 GOST 20.57.406. Holding time in heat chamber = 1 h. Holding time at normal conditions after testing = 0.5h.
- Minimum ambient temperature test in accordance with the method 204-1 GOST 20.57.406. Holding time in heat chamber = 1 h. Holding time at normal climatic conditions after testing = 0.5h.
- Failure-free test for 3 samples of the ICs during 500 h at 70°C.
- Longevity test for 3 samples of the ICs which have passed the aforementioned failure-free test during 500 h at normal conditions.

The tests have shown that the package satisfies the following requirements:

- A.Package's pins including points of attachment have withstand to stretching strength 2.5 N (0.25 kgf) directed along pin axis.
- B.Package's pins have withstand bending strength without mechanical damage.
- C.Requirements to resistance and strength during mechanical and climatic exposure:

#### Resistance to mechanical action exposure

- Sinusoidal vibrations:
  - Frequency range, Hz 1-500
  - Acceleration amplitude, m/s<sup>2</sup>(g) 50 (5)

- Single mechanical impacts:
  - Peak impact acceleration,  $m/s^2$  (g) 1500 (50)
  - Duration of impact acceleration action, ms 2-20
- Multiple mechanical impacts:
  - Peak impact acceleration,  $m/s^2$  (g) 150 (15)
  - Duration of impact acceleration action, ms 2-20

#### Climatic resistance:

- Increased ambient temperature:
  - operational, °C 70
  - ultimate, °C 70
- Decreased ambient temperature
  - operational, °C minus 30
  - ultimate, °C minus 60
- Ambient temperature change
  - Temperature range, °C from minus 60 to plus 70
- Increased air humidity:
  - Relative humidity at 25°C, % 98
- Decreased atmospheric pressure:
  - operational, Pa (mmHg)  $5.3 \cdot 10^4$  (400)
  - ultimate, Pa (mmHg)  $1.2 \cdot 10^4$  (90)

#### Glue

Choice of the glue to paste together package parts has been carried out in accordance with OST 4G 0.029.204 Glues. Features. Fields of application. According to this document the glue VT-25-200 used to paste together package parts provides vacuum tight seams. It has shift resistance  $125 \text{ kgf/cm}^2$  at normal conditions and  $40 \text{ kgf/cm}^2$  at increased temperatures (+180°C).

The glue ECH-C to paste chips has following features:.

- The chip back side has no metallization to solder it onto the mounting pad.
- In addition, fluxes are provided to be used to delete soldering-alloy oxide-film when soldering chips by low-temperature alloys. Removal of flux remainders from the packages makes some problems.
- Contact-reactive soldering by creating of gold-silicon eutectic alloy is impossible due to the package design.
- To attach the package lead by any other method rather than pasting is unreasonable because the chip's base, pin frame, and rings are mounting with using the glue VT-25-200.

### The aim of the package design

The oxidised-aluminium package presented has been designed due to absence of any 48-pin 1.27-pitch square four-side planar metal-ceramic package in former USSR. In our opinion, it presents cheap flexible solution for custom ICs. To make an ultimate decision we have to choose one of the following ways:

- To carry out full scale test of packaged ICs according to the GOST 20.57.406. (The test duration is estimated to be equal to 2 month).
- To go on to using of commercial metal-ceramic 48-pin 1 mm pitch square planar packaged produced in Russia. The gold-free (i.e. cheaper) package may have produced. (42 pin square planar gold-free version is commercially available.). The packages may be presented by JINR to diminish expenses.
- The gold-containing packages can be used, and fitting on gold-silicon eutectic layer is possible too (The gold problems seems to becomes more simple when JINR provides required volume of gold foil (an order of milligrams) with the packages). The contact test socket device can be done over again (PCB and fitting socket).
- To use metal-ceramic packages of foreign production (e.g. USA). Plastic packages seem to be not the best solution.

### *The amplifier-discriminator multilayer PCB (version 1.0)*

The PCB is intended to amplify and discriminate signals from 32 channels of muon detector tubes. It contains 4 ICs each of Ampl-8 and Disc-8. The PCB has following parameters:

- Size: 213mm x 83mm x 1.5mm
- Number of layers: 6
- Type of mounting: SMD
- Material: glass-cloth-base laminate  
FR-4.

In addition to 8 amplifier and discriminator chips with their power supply line filters there are a test signal generation channel, a threshold control channel, and adjustable voltage stabiliser to feed the discriminator open collector resistors on the PCB. The view of the PCB from the side of elements is shown in Fig.\_\_\_.

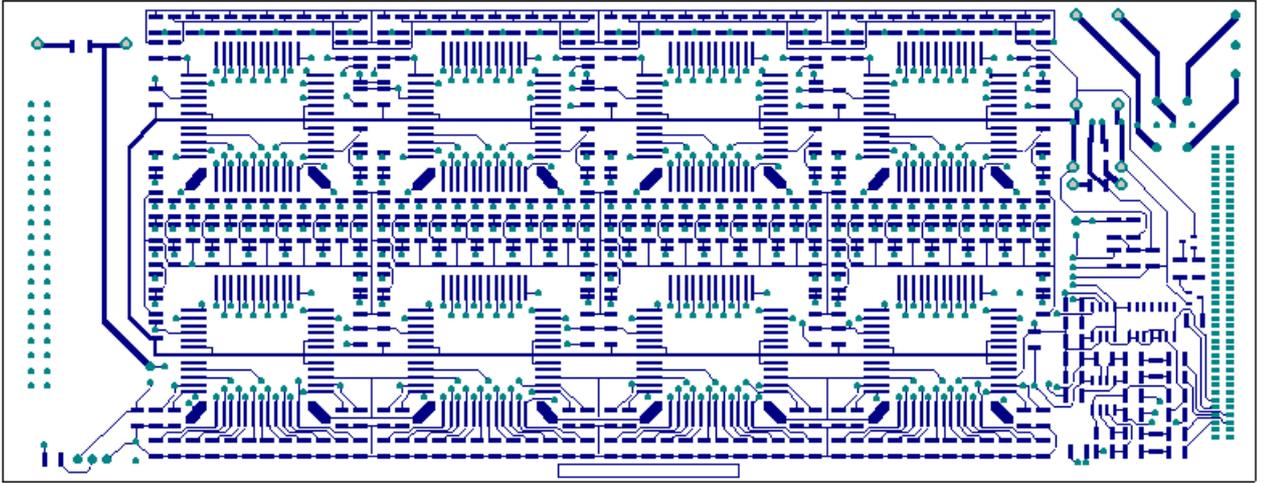


Fig.5-4.The amplifier-discriminator PCB v.1.0 top layer.

### References

- [1] M.A.Baturitsky et al. Nucl. Instr. and Meth. A 378 (1996) 570-576.
- [2] M.A.Baturitsky et al. Nucl. Instr. and Meth. A 352 (1995) 604-609.