

D0 Muon PDT Control Board Specification

Sten Hansen Revised 6-1-98

I Functional Description:

The Proportional Drift Tube (PDT) Control Board (CB) is connected to as many as four front end boards (FEBs). It is the interface between these boards and the Muon Readout Card (MRC) and monitoring systems. A block diagram is shown in Fig. 1.

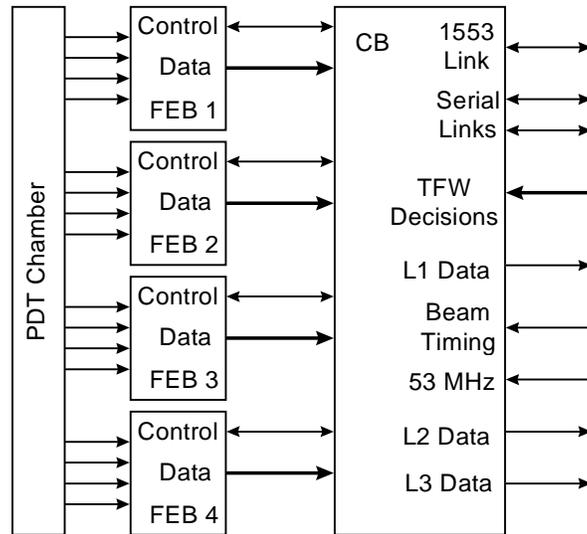


Fig. 1 PCB Data and Control Links

When in data taking mode, a new set of hit bits is sent to the L1 trigger system every 132 ns by means of a 1 Gbit/s serial link mounted on a daughter board designed by Arizona University. In response to an L1 accept trigger, data is read from the FEBs and stored in CB memory pending the outcome of an L2 decision. Data from each L1 accept is also processed and then transmitted on a 160 Mbit/s serial link to the L2 trigger system. An L2 accept initiates the transmission of an event to the Daq system in the movable counting house (MCH) also by means of a 160 Mbit/s serial link. An L2 Reject causes the data stored for that event to be discarded.

Trigger decisions are sent to the CB by means of a 25 pair ribbon cable running from the MRC in the MCH to the collision hall. Peaking networks are fitted to each signal pair to increase the effective bandwidth of the cable, since the intrinsic bandwidth of this cable is less than 7MHz, the reciprocal of the crossing rate. To keep E.M.I. radiation to a minimum, current mode transmission is used. Encoded timing information is sent on one section of a four conductor ribbon coaxial cable also running from the MRC to the platform. The other conductors are used for L2 trigger data, L3 data and a 53MHz clock. To enforce a balance between center conductor and shield currents, and thus reduce E.M.I., transformer coupling is used. This has the additional feature of breaking the ground loop that would occur if the cable shields were attached directly to ground at both the MCH and the platform.

An on-board timing generator can delay all the arriving timing signals a programmable amount as a means of synchronizing the operation of all FEBs in the muon system. For test pulsing, a programmable test pulse generator is fitted.

The board uses two DSP microprocessors, one as the data acquisition processor, the other as the control interface. This control processor handles the serial ports, 1553 interface, FEB control functions, the on board test pulse generator, the timing generator settings, DACs for setting test pulse amplitudes and wire discriminator thresholds, and ADCs measuring power supply voltages and the PDT chamber differential gas pressure.

Inter-processor communication is limited to remote downloading of readout processor code and changing readout operational modes. The data paths FEBs and the CB for control and data taking between are completely separate.

II L1 Hit transmission

The L1 trigger hardware requires a wire hit map to be delivered to the L1 trigger system once per crossing. 96 bits must be sent every 132 ns which requires a 670 Mbits/s transmission rate. The closest industry standard match to this bandwidth is a 1 Gbit/s link. Arizona University has chosen an AMCC device and will provide daughter boards with a 16 bit, 53MHz parallel interface for use by Muon sub-system front-ends. There are four 25 pair ribbons connecting each FEB to the CB for the purpose of transmitting hit bits. The bits are clocked in at 7 MHz into six tri-state registers. Their outputs are multiplexed into the daughter board at 53MHz. Six 53MHz clock periods are used to send 96 bits of data, the seventh interval is used to send a parity word. The phasing of the 7 MHz clock is adjustable within the timing generator, detailed later in the document. The L1 system expects null characters to be sent during Sync Gap (Sgap). Incoming Sgap can also be delayed a programmable amount such that the hit candidates sent could only have come from active crossings.

III FEB Interface

The FEB uses a KEK designed TDC chip which has several control registers that must be loaded with setup data. Control logic adjusting pad ADC pipeline depth and input enables for the wire channels along with miscellaneous control bits (see FEB specification) must be set prior to operation. The input enables can be used to select a particular subset of the channels for test pulsing, or to disable a bad channel during data taking. An eight bit bi-directional data bus and a seven bit address bus connects the control logic from each FEB to the CB. An address map of the FEB control function is contained in the FEB specification. A set of four of these maps is included in the address map of the control processor. A Read/Write and Strobe line control transfers on this control bus.

The readout data path is an 18 pair uni-directional LVDS level bus. LVDS was chosen principally for its low E.M.I., but has the additional advantages of low power consumption and high speed. When readout is in progress (indicated by Read Enable high), data is sent from the FEB to the CB and is accompanied by a readout clock. The data has a specified setup and hold with respect to the rising edge of the readout clock. For each event, Read Enable is asserted twice per FEB, first for wire information then for pad data. Timing diagrams for control and data operations are shown in fig. 2.

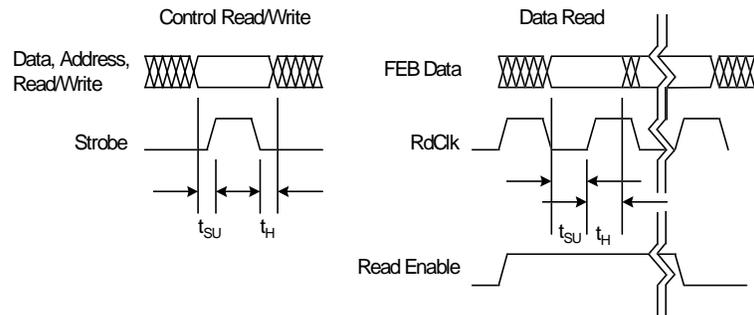


Fig. 2 FEB Control and Data Transaction Timing

IV Readout Controller

The 18 bit read data from the FEBs is re-formatted, then written to a 16 bit dual port RAM by means of hardware sequencer. This sequencer delivers 16 bit wide, zero suppressed data to the RAM, relieving the processor of the lowest level of bit manipulation tasks and allowing it to

perform higher level operations on the data for which it is better suited. The incoming and outgoing data formats are summarized in tables 1,2 and 3 in the appendix. The controller output for wire data is divided into four sections because each FEB produces three leading words of TMC read pointer data which cannot be distinguished from time data. By leading with a word count for each FEB, the location of the read pointers is known.

The pad data consists of a single word count followed by paired address and data words. The address defines a tube pair in the range of 0 to 47. Bit 15 is used to distinguish between address and data words. The tag bits within the pad data word are used to identify the source of the ADC data. There are two pad electrodes per PDT cell, and in order to reduce the number of pipeline buffers, one buffer is used to store the data for two channels (Refer to the FEB specification for details). Finally, a marker to identify the ADC value as being either a baseline or a peak signal sample (denoted B/P).

V DAQ Control Signals

The signals arriving from the Trigger Framework (TFW) include INIT, L1 Accept, L2 Accept, L2 Reject and eight bits of crossing number associated with a particular trigger decision. An L1 Accept triggers two programmable digital one-shots whose signals are used to control the transfer of data between the L1 pipeline and L1 FIFOs situated on the FEBs. L1 Accept is the highest priority interrupt of the readout DSP while L2 accept and reject are OR'ed to form the next highest priority DSP interrupt. The incoming crossing number is latched in the case of L1 Accepts or written into a crossing number FIFO in the case of L2 decisions, for later reading by the processor during its trigger decision interrupt service routine. This number is compared to on-board crossing and turn counters as a check for proper event synchronization. The signals BUSY 1, BUSY 2, ERROR 1, and ERROR 2 are returned to the TFW by way of the MRCs when the appropriate condition occurs.

VI Timing decoder

Timing signals must be recovered from the encoded serial stream. A custom made voltage controlled crystal oscillator with a center frequency of 53.1047 MHz and a 20 KHz adjustment range serves as the basis of phase locked loop frequency multiplier used to produce 106MHz locked to the incoming encoded data stream. This signal clocks a state machine realized with a 7ns PZ5064 CPLD chip which de-serializes the data into First Crossing, GAP, and Sync Gap and divides the 106MHz down to a symmetric 53MHz. For the PDTs, GAP has no relevance and is not used. By sending clock and data through the same drivers, receivers and cable, their phase relationship is constant. The 53MHz reference clock for the TDCs coming from the TFW SCL board is de-jittered by means of a CY7B991 clock buffer before being sent to the FEBs. This chips has four independent sets of jumper selectable phase adjustments of 9 steps of about 1.2 ns each.

VII Control Processor

An ADSP 2181 processor is used as the controller for all functions not related to data taking. The readout processor can read and write data to and from the IDMA port of the control processor. An address map of a subset of the internal memory of the control processor is agreed upon in the software of the two processors. The lowest priority external interrupt on the readout processor is a service request from the control processor. A connection diagram showing the connections to the control bus is shown in Fig. 3. The peripherals under the control of the processor in addition to the FEB control path include:

Heartbeat

The system reset chip will issue a processor reset if it does not receive a heartbeat input within about a second. This will obviate the need for remote reset in the event of a software hang. A flag out pin on the processor is attached to the heartbeat pin of the reset chip. There are a

number of ways that a heartbeat can be issued. A internal periodic interrupt from the processor's on-chip timer is one possibility.

Serial Ports:

One channel of an AM85C30 dual SCC is used as a local RS-232 terminal port and the second channel is setup to run at 2.5 Mbits/s on two pairs of lines for transmit and receive connected to the MRC. It is possible, if desired, to use a break character as a remote processor system reset. This feature can be disabled.

1553 Interface:

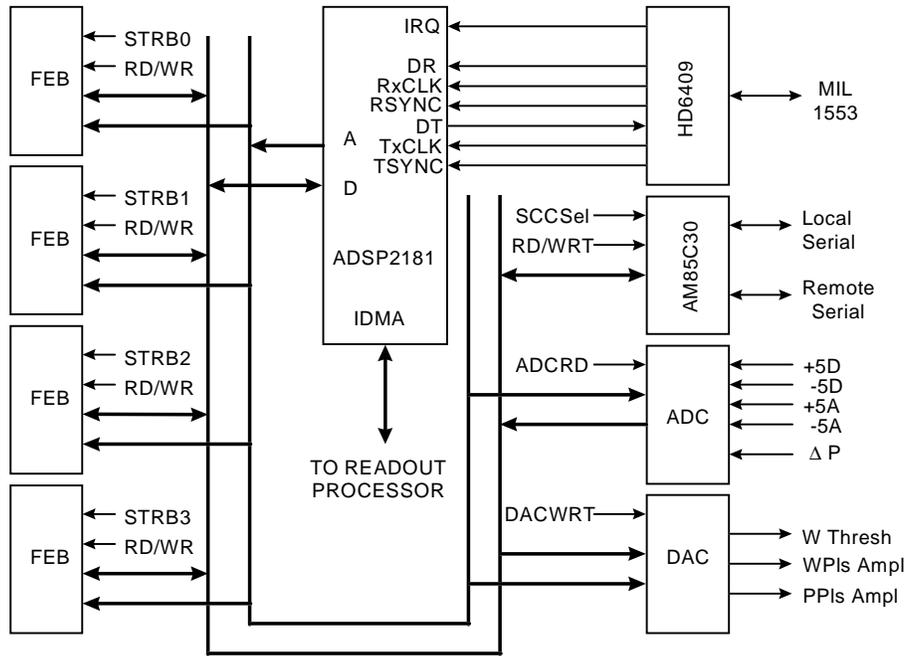


Fig. 3 Control Processor Sub-Block

A Harris HD6409 MIL1553 to serial interface operating at 1 Mbit/s is attached to the synchronous serial ports of the control processor. The physical layer driver, receiver and transformer are identical to those already in service at D0. An inverted copy of the Valid Word signal from the interface is attached to the processor's external interrupt pin. Decoding of the command word and transmission of the appropriate response is done in software. If there have been no 1553 accesses for 10 seconds, the processor issues a Remote Terminal reset, in order to conform to D0 CDAQ requirements. The processor's on chip timer is suitable for this function. Status LEDs signaling remote terminal access and reset are fitted.

DACs, ADCs:

An eight channel ADC and a four channel DAC are connect to the control processor. As of now, only five ADC values and three DAC values are used. The DACs and ADCs have a precision of eight bits with a span of 0 to 4.096 volts or 16 mV per bin. ADC channels 0,1,2, and 3 are attached to the +5 digital, -5 digital, +5 analog, and -5 analog power supplies. The negative supplies are inverted then divided by 2 before being attached to the ADC inputs. The positive supplies are divided by 2. When the power supplies are at their nominal values, the four ADC channels will read ½ scale. The fifth ADC channel expects an input from an Exar SM5552 differential pressure sensor. 0 to 255 on the ADC corresponds to 0 to 10 inches of water differential pressure. The three uncommitted ADC inputs are attached to gain of 200 instrument amplifiers for use by any standard 25mV output sensor, in the event some other external quantities need to be monitored. A +10 V reference is also supplied to these inputs. The DAC

outputs set wire discriminator threshold, wire test pulse amplitude and pad pulse test amplitude. Op-amp buffers are used to isolate the DAC outputs from any loads presented by the FEBs.

Test Pulse Generator

Separate turn and crossing counters are implemented to allow the adjustment of the timing and repetition rate of test pulses. A 16 bit counter counts turns while a crossing counter counts at the 7 MHz rate and a vernier modulo seven counter runs at 53MHz. A test pulse can be generated at a resolution of 2 ns anywhere within a turn every N turns where N is a 16 bit prescale value loaded into the turn counter. To a resolution of 19 ns, counters determine the pulser timing. The finest steps are adjusted by means of a 10 tap 2ns per tap delay line.

Timing Generator

It is the responsibility of the TFW to send beam timing information early enough so that the detector with the greatest cable delay will still get the timing information ahead of the actual beam crossings. It is the responsibility of each front-end system to trim the timing on these incoming signals so that they match the local timing of the interactions. This timing depends on many factors: cable lengths, electronics delays, physical distance from the interaction region etc.

The length of the pipeline delays must be adjusted to match exactly the sum of the propagation delays and the L1 trigger decision time. This cannot be known a priori to the necessary precision and must be trimmed based on measured times. The test pulse generator can be used to measure the trigger decision time, and thus the value of the pipeline delay. Beam data is used to align the timing sequence to the interactions. For this adjustment, the beam and pipeline delays must be moved together to preserve a fixed relationship between the data emerging from the pipeline and the time of arrival of L1 Accept.

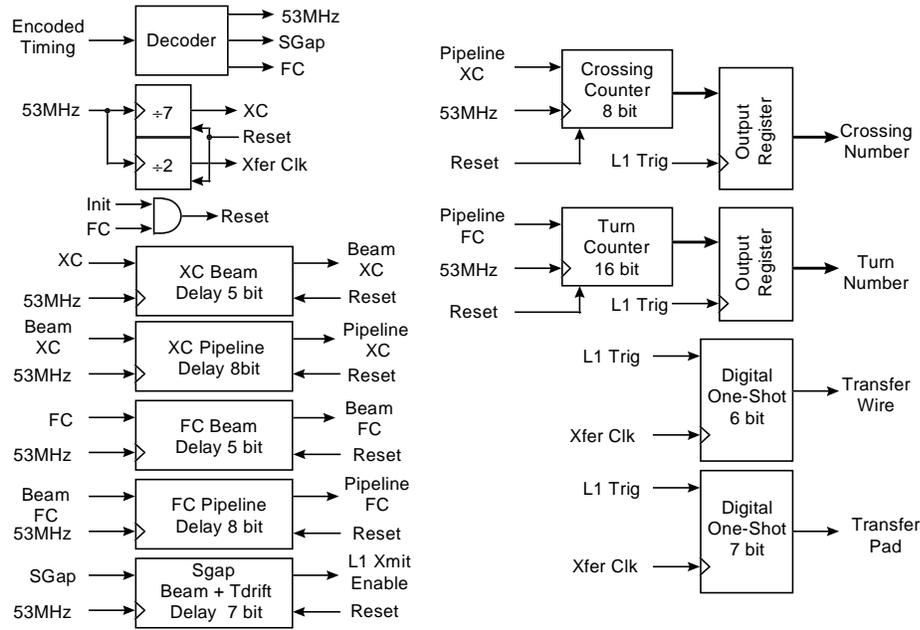


Fig. 4 Timing Generator

The third relevant timing parameter is the adjustment of the drift time. The two transfer gates determine the length of time data emerging from the TDC and ADC pipeline delays are written into the L1 FIFOs. Because of the charge collection time of the pads and the additional time required to multiplex two analog signals into one ADC, the pad transfer is about 500 ns longer than the TDC transfer gate. The L1 transmit enable, a delayed copy of SGap is used to enable the transmission of hit bits being sent to the L1 system. A block diagram of the timing generator is shown in Fig. 4. The hardware can accommodate individual adjustment of all five delays, although it should be possible with suitable software in the control processor to simplify

the external user interface by having one number for beam related delays and a second number for pipeline related delays.

VIII Readout Processor

The readout processor is used to execute data taking related tasks. To that end there are interrupts for trigger decisions, the completion of the reading of an event by the readout hardware, and a service request from the control processor. The processor chosen is an AD21Csp-01 fixed point DSP processor running at 50MHz. This device is sufficiently powerful to perform all higher level data formatting and buffering under software control, thus affording a degree of flexibility in the face of changing requirements. It also has the effect of shifting the design burden from hardware to software. A block diagram of the main processor sub-section is shown in Fig. 5.

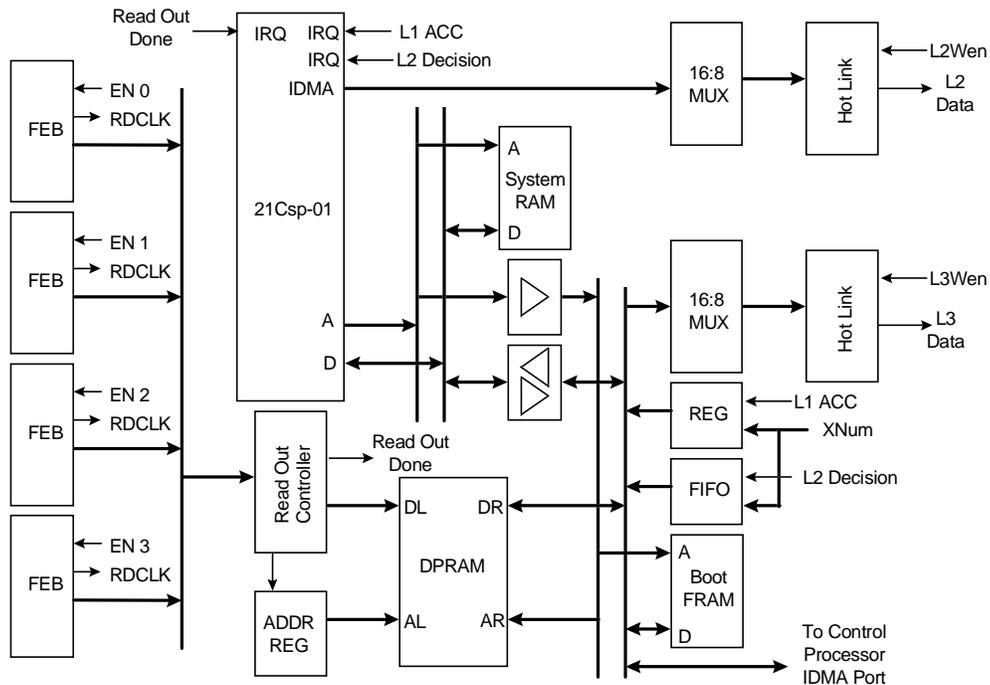


Fig. 5 Readout Processor Sub-block

Local Triggering

For self triggering on wire discriminator hits, a 24 fold OR from each FEB is brought to the CB. The FEB Ors can be used to form a single OR with contributions from as many as 96 wires. For those PDT chambers with less than four FEBs, unused ORs can be masked. A delayed copy of the FEB signal synchronized to the 53MHz RF and limited in width to two clock periods is sent to the L1 trigger interrupt of the readout processor and the Trig Out LEMO. This delay simulates the timing of the TFW, and when set correctly, there will be no need to modify the timing generator settings when switching between local triggers and the TFW. A Trig IN LEMO is also provided for NIM level external triggers from a local scintillator coincidence or the L1 trigger system. Trig IN is synchronized and truncated in the same manner as the FEB Ors.

Trigger Information Registers

In addition to the crossing number coming from the TFW, on board crossing and turn counters are clocked by appropriately trimmed copies of the beam orbit timing signals. The processor can immediately check the internal and external crossing numbers for consistency, but because the bandwidth required to ship turn numbers from the MCH along with the triggers is prohibitively large, the internally generated turn number is sent to the MCH as part of the L3 data block and compared to the TFW generated turn number there.

L2 Data Transmission

Each L1 accept begins the readout process. Once the readout controller has finished writing an event into the DPRAM, the processor must reformat wire data and strip off pad data prior to sending it to L2. Arbitrary units are normalized to standard units and local address references may have to be re-mapped to a global numbering scheme. The 16 bit wide IDMA port is used to send L2 data without processor intervention. The HOTLink transmitters have an input pin that selects between sending control or data streams. A line to drive this pin is not available on the IDMA port. To perform this function, the external hardware sequencer controlling the L2 HOTLink interprets the first and the last word in the DMA block as control characters. From the software point of view, a DMA transfer is started by writing the number of words in the DMA block including the block boundary control characters to an external I/O location. This loads a counter in the sequencer which decrements with each word sent. The first word leaving the IDMA port is sent with the transmitter in control mode while subsequent words are transmitted as data. When the counter reaches one, the transmitter is set to control mode and the last word is sent as a control character. The controller sends only the lower eight bits of the first and last words.

L3 Data Transmission

The transmission of L3 data is under direct processor control and is presumably a low priority background process, since the expected L3 event rate is low. One I/O location sends 16 bits of data, while a second location sends eight bits of control information. The test modes of both Hot Link interfaces are controlled by the readout processor.

IX Power Supplies

The only input power used is +5 and -5 digital. +5 and -5 analog are brought to the board only for monitoring by the scanning ADC. The pressure sensor, DAC reference voltage and the DAC require a voltage greater than +5. A DC-DC step-up converter set to +12V is used to generate these voltages. The 1553 drive section requires +10V. Again a step-up converter set to +10V is implemented. Finally, the Arizona daughter board requires about 200mA of +3.3V. In the interest of reducing power consumption, a switching type step down regulator is fitted. The stated efficiency for all the on board voltage converters is greater than 85%.

Appendix:

Table 1
Readout Controller Wire Data Format

No. Bits	5		3	8	
FEB 1 Wire Word Count:	0		# FEBs	Word Count	
No. Bits	1	7		1	7
FEB 1 Read Ptr 1	0	TMC 1 Rd Ptr		0	TMC 2 Rd Ptr
FEB 1 Read Ptr 2	0	TMC 3 Rd Ptr		0	TMC 4 Rd Ptr
FEB 1 Read Ptr 3	0	TMC 5 Rd Ptr		0	TMC 6 Rd Ptr
No. Bits:	1	5		5	
First FEB 1 Data Word	0	FEB 1 Chan #	Coarse Count		Vernier Count

•
N FEB 1 Data Words
•

No. Bits	8		8		
FEB 2 Wire Word Count:	0		Word Count		
No. Bits	1	7		1	
FEB 2 Read Ptr 1	0	TMC 1 Rd Ptr		0	
FEB 2 Read Ptr 2	0	TMC 3 Rd Ptr		0	
FEB 2 Read Ptr 3	0	TMC 5 Rd Ptr		0	
No. Bits:	1	5		5	
First FEB 2 Data Word	0	FEB 2 Chan #	Coarse Count		Vernier Count

•
N FEB 2 Data Words
•

No. Bits	8		8		
FEB 3 Wire Word Count:	0		Word Count		
No. Bits	1	7		1	
FEB 3 Read Ptr 1	0	TMC 1 Rd Ptr		0	
FEB 3 Read Ptr 2	0	TMC 3 Rd Ptr		0	
FEB 3 Read Ptr 3	0	TMC 5 Rd Ptr		0	
No. Bits:	1	5		5	
First FEB 3 Data Word	0	FEB 3 Chan #	Coarse Count		Vernier Count

•
N FEB 3 Data Words
•

No. Bits	8		8		
FEB 1 Wire Word Count:	0		Word Count		
No. Bits	1	7		1	
FEB 4 Read Ptr 1	0	TMC 1 Rd Ptr		0	
FEB 4 Read Ptr 2	0	TMC 3 Rd Ptr		0	
FEB 4 Read Ptr 3	0	TMC 5 Rd Ptr		0	
No. Bits:	1	5		5	
First FEB 4 Data Word	0	FEB 4 Chan #	Coarse Count		Vernier Count

•
N FEB 4 Data Words

Table 2
Readout Controller Pad Data Format

No. Bits:	16
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Pad Word Count:	Word Count						
No Bits:	1	9	6				
Pad Pair Address:	Addr/Data	N.A.	Pair #				
No. Bits:	1	1	1	1	1	1	10
Pad Data:	Addr/Data	Chan A/B	Pad A/B	B/P	OVF	UF	ADC Data

•
N Words of Pad Data

Table 3
Example of Pulser Data set for 4 FEBs connected to CB.

0407	2B2B	2B2B	2B2B	01D4	09D4	13D6	19D4	0007
2323	2323	2323	00D4	08D4	10D2	18D6	0007	1B1B
1B1B	1B1B	03D5	0BD4	13D7	1BD7	0007	1313	1313
1313	02D6	0AD5	12D5	1AD5	0050	8000	3046	1048
02E4	22E2	8001	304C	1054	02F2	22DA	8002	3050
1050	12F4	330A	8003	3052	1052	0318	2304	800C
304C	104E	0308	22F2	800D	3048	1047	0303	22EC
800E	304A	1048	0302	22F1	800F	304E	104B	02FF
22E4	8018	3050	1052	0309	2301	8019	304F	104D
030A	22F3	801A	3051	1051	0302	22E6	801B	3050
1046	0314	22FB	8024	3060	105F	0325	2317	8025
3057	1057	0324	2310	8026	3061	105C	031D	2311
8027	305B	1059	0327	230E				

Processors:

Control - Analog Devices ADSP2181 operating at 40MHz
Readout - Analog Devices ADSP21Csp-01 operating at 50MHz

FEB Interface:

Control Interface:

t_{SU} Control Data, R/W to Strobe - 20 ns
 t_H Strobe to Control Data, R/W - 20 ns

Data Interface:

Data Readout Clock Rate - 12.5 MHz
 t_{SU} RdEn to RdClk - 35 ns
 t_H RdClk to RdEn - 35 ns
 t_{SU} Data to RdClk - 10 ns
 t_H RdClk to Data - 10 ns

Serial Data Link Rates:

Remote Serial Port Data Rate - 2.5 Mbits/s
MIL 1553 Data Rate - 1Mbits/s
L1 Transmission Rate - 1060 Mbits/s
L2 Transmission Rate - 160 Mbits/s
L3 Transmission Rate - 160 Mbits/s
Encoded Timing Data Rate - 106 Mbits/s

Timing Generator:

Beam Delay Range/Resolution - 600/19 ns
Pipeline Delay Range/Resolution - 4802/19 ns
L1 Enable Delay Range/Resolution - 2391/19 ns
L1 Pad Transfer Duration Range/Resolution - 2410/38 ns

L1 Wire Transfer Duration Range/Resolution - 1205/38 ns

Test Pulse Delay Resolution - 2ns
 Test Pulse Prescale Range - 1 to 65535

Internal Trigger Delay Range/Resolution - 4802/19 ns

Control Processor Interrupts (in order of priority):

IRQ2 - 1553 Valid Word
 EIRQ1 - Test Pulse
 LIRQ1 - Init
 Sport0 Rx - 1553 Data Received
 Sport1 Tx - 1553 Data Sent
 Timer - Remote Terminal Timeout, Heartbeat, Read scanning ADC

Control Processor I/O Map

RAM Address(Hex)	Device	No. of Bits
PM(0 - 3FFF)	Internal Program Ram	24
DM(0 - 3FFF)	Internal Data Ram	16
I/O Address		
0 - 7F	FEB 0 Control	8
80 - FF	FEB 1 Control	8
100 - 17F	FEB 2 Control	8
180 - 1FF	FEB 3 Control	8
200	Test Pulser Turn Prescale Lower byte	8
201	Test Pulser Turn Prescale Upper byte	8
202	Test Pulse Crossing Value	8
203	Test Pulse Vernier Count and Delay Tap	3
204	CSR Register	8
205	Issue Internal Clear	X
206	Flash 1553 Time Out LED	X
207	Issue 1553 Encoder Enable	X
208	FC Beam Delay Register	5
209	FC Pipeline Delay Register	8
20A	XC Beam Delay Register	5
20B	XC Pipeline Delay Register	8
20C	Sgap Tdrift Delay Register	7
20D	Wire Transfer Length	6
20E	Pad Transfer Length	7
20F	Not used	
210 -213	SCC Interface	8
214 - 217	4 Channel DAC	8
218 - 21F	8 Channel ADC	8
SPORT0 RX	1553 Data Receive	16
SPORT1 TX	1553 Data Transmit	16
Flag Out 0	Readout Processor Service Request	1
Flag Out 1	1553 Decoder Reset	1

Flag Out 2	Heart Beat Timer Reset	1
Pflag 0	1553 Power Driver Enable	1
Pflag 1	1553 Encoder Enable	1
Pflag 2	1552 Sync Select	1
Pflag 3	Enable FEB 1	1
Pflag 4	Enable FEB 2	1
Pflag 5	Enable FEB 3	1
Pflag 6	Enable FEB 4	1

Readout Processor Interrupts (in order of priority):

IRQ3 - L1 Accept
 IRQ2 - L2 Decision
 IRQ1 - Readout Controller Done
 IRQ0 - Control Processor Service Request

Readout Processor Map

RAM Address(Hex)	Device	No. of Bits
0-1FFF	Internal RAM	24
10000-17FFF	External SRAM	
400000-403FFF	External Dual Port RAM	16
800000-820000	Flash RAM	8
I/O Address	Device	No. of Bits
0	L2 Crossing FIFO	8
1	L1 Crossing Latch	9
2	Issue Timing Decoder Reset	X
3	Issue Timing Decision Fifo Reset	X
4	L3 Data Word	16
5	L3 Control Word	8
6	Local/Remote Clock Select	1
7	Internal Turn Counter	16
8	Internal Crossing counter	8
9	Crossing PAL CSR Register	10
A	Trigger Delay	8
B	Issue L1 Trig	X
C	Clear Trigger Inhibit	X
D	Set L2 Hot Link Control Bits	7
E	Set L3 Hot Link Control Bits	7
F	Control Processor IDMA Data	16
10	Control Processor IDMA Address	16
11	Issue Transmit FIFO Reset	X
12	Issue Readout Controller Reset	
13	Issue Readout Controller Start	X
12	DMA Transfer word count	8

13	Stop DMA transfer	X
14	DMA transfer status	3
Flag Out 0	Busy 1	1
Flag Out 1	Busy 2	1
Flag Out 2	Err 1	1
Flag Out 3	Err 2	1
Flag In 0	Init	1
Flag In 1	L2 Decision FIFO Empty	1
Flag In 2	L2 Decision FIFO Full	1

Sensor Connector Pinouts (P11..P14)

Pin #	Label	Description
1,2	In1+	25mV Diff. Signal
3	+10V	Power
4	Gnd	Ground
5,6	In1 -	25mV Diff. Signal

L1 Transmitter Daughter Board Pinouts

Pin #	Label	Description
1	GND	Ground
2	GND	Ground
3	Data_In_0	LSB of Input Data
4	Data_In_1	Input Data
5	Data_In_2	"
6	Data_In_3	"
7	Data_In_4	"
8	Data_In_5	"
9	Data_In_6	"
10	Data_In_7	"
11	Data_In_8	"
12	Data_In_9	"
13	Data_In_10	"
14	Data_In_11	"
15	Data_In_12	"
16	Data_In_13	"
17	Data_In_14	"
18	Data_In_15	MSB of Input Data
19	Fast_OR	Fast Or Output
20	Word_Clock	RF Clock
21	Enable	High = Data Enabled
22	Parity_Enable	High = Transmit Parity
23	Spare	
24	GND	Ground
25	+5V	+5 volt Power Supply
26	+5V	+5 volt Power Supply
27	+3.3V or +5v	Output Power Supply
28	GND	Ground

Pin #	Label	Description
29	+3,3V	+3.3 volt Power Supply
30	+3.3V	+3.3 volt Power Supply

25 Pair MRC Connector Pinouts

Pin #	Label	Description
1	XN0+	Crossing Number
2	XN0-	"
3	XN1+	"
4	XN1-	"
5	XN2+	"
6	XN2-	"
7	XN3+	"
8	XN3-	"
9	XN4+	"
10	XN4-	"
11	XN5+	"
12	XN5-	"
13	XN6+	"
14	XN6-	"
15	XN7+	"
16	XN7-	"
17	Init+	TFW Init
18	Init-	"
19	L1Acc+	Level 1 Accept
20	L1Acc-	"
21	L2Err+	Level 2 Error
22	L2Err-	"
23	L2Acc+	Level 2 Accept
24	L2Acc-	"
25	L2Rej+	Level 2 Reject
26	L2Rej-	"
27	Tx+	Serial Transmit from MRC
28	Tx-	"
29	Done+	MRC to VBD Transfer Done
30	Done-	"
31	Strb+	7 MHz Crossing Clock
32	Strb-	"
33	Rx+	Serial Receive to MRC
34	Rx-	"
35	L1Err+	Level 1 Error
36	L1Err-	"
37	Busy1+	Level 1 Busy

Pin #	Label	Description
38	Busy1-	"
39	Busy2+	Level 2 Busy
40	Busy2-	"
41..50	Ground	Not Used

Power Consumption:

+5D: 2.2A
-5D: 0.5A
+5A, -5A: 15mA

Mechanical:

6.5" x 23.25" .093" thick
4 100 pin high density connectors for FEB data and control
4 50 pin high density connectors for FEB hit bits
1 50 pin standard density connector for MRC interface
1 8 pin Ribbon Coaxial Connector for Beam Timing, 53MHz, L2 Data, L3 Data
1 9 pin "D" connector for the local terminal port
1 10 pin ISP programming connector
2 Trompeter Tri-Axial Connectors for the MIL 1553 Connection
3 6 pin S.I.P connectors for external sensor connections
1 12 pin Ribbon Power Connector
1 Lemo connector for trigger out
1 Lemo connector for trigger in
1 System Reset Switch

LEDs:

+5D,-5D,+5A,-5A power indicators
MIL 1553 Remote Terminal Access
MIL 1553 Remote Terminal Timeout
Trigger In
Trigger Out
53 MHz clock present
Encoded timing signals present