

## PDT Control Board 1553 Interface Address Map

The preliminary specification describing the assignment 1553 sub-addresses to presently known functions implemented in the CB follows. Functions may be added or deleted as dictated by operational experience. The specification will be finalized after system testing is completed. Read and Write are from the point of view of the controller.

Table 1. Muon CB sub-address assignments:

Sub Address(Hex)	Device	No. of Bits	Access Type	# Words	Parm Type	Function	Data Type
0	Mode Command	16	W	1	SW	Error Recovery	Bit
1	Trigger Gate	6	R/W	1	HW	Cold Start	"
2	FEB 1 Run Control	6	R/W	1	"	"	"
3	FEB 2 Run Control	6	R/W	1	"	"	"
4	FEB 3 Run Control	6	R/W	1	"	"	"
5	FEB 4 Run Control	6	R/W	1	"	"	"
6	FEB Channel Enables 1..16	16	R/W	1	"	"	"
7	FEB Channel Enables 17..32	16	R/W	1	"	"	"
8	FEB Channel Enables 33..48	16	R/W	1	"	"	"
9	FEB Channel Enables 49..64	16	R/W	1	"	"	"
A	FEB Channel Enables 65..80	16	R/W	1	"	"	"
B	FEB Channel Enables 81..96	16	R/W	1	"	"	"
C	ADC Pipeline Length TMC Setup Registers	8	R/W	3	HW <sup>1)</sup>	"	Analog
D	FEB L1 FIFO Empty Flags	16	R	6	N.A.	Debug	Bit
E	FEB ADC Pipeline Empty Flags	16	R	6	N.A.	"	"
F	FEB L1 FIFO Full Flags	16	R	6	N.A.	"	"
10	Monitoring ADC	8	R	8	N.A.	Monitor	Analog
11	CB Control Register	16	R/W	1	HW <sup>1)</sup>	Cold Start	Bit
12	CB Status Register	16	R/W	1	N.A.	Monitor	Bit
13	Wire Threshold	8	R/W	1	HW	Cold Start	Analog
14	Wire test pulse amplitude	8	R/W	1	HW	"	"
15	Pad test pulse amplitude	8	R/W	1	HW	"	"
16	Test pulse turn prescale value	16	R/W	1	HW	"	"
17	Test pulse delay setting	16	R/W	1	HW	"	"
18	CB Delay Settings	8	R/W	5	HW	"	"
19	Not Used	-	-	-	-	-	-
1A	Not Used	-	-	-	-	-	-
1B	Multi-Block Command Words	16	R/W	7/6	SW	Setup	N.A.
1C	Download Multi-Block	16	W	Variable	SW	"	N.A.
1D	Upload Multi-Block	16	R	Variable	N.A.	Debug	N.A.
1E	CB Internal Status	16	R	1	N.A.	Debug	Bit
1F	Broadcast Mode Cmd.(not used)	-	-	-	N.A.		

<sup>1)</sup> Note: Because of hardware limitations, these parameters cannot be updated immediately. Update occurs at INIT, as are the software parameters.

Mode Commands used :

- 0x 01 - Clear Multi-Block operation in progress
- 0x 08 - Reset Remote Terminal - Control and readout processor reset.

The following sub-addresses perform these functions:

(0x01) These bits set the length of the trigger pulses generated by the FEB on-board one-shots.

(0x02..0x 05) FEB run control register bits enable different data-taking modes on the FEB.

(0x 06..0x 0B) FEB channel enable bits enable individual FEB channels.

(0x 0C) Word 0 - ADC Pipeline delay in units of RF/4 (6 bit word).

Word 1 - TMC Read pointer setting in units of RF/2 (typically set to 0, 7 bit word).

Word 2 - TMC Write pointer setting in units of RF/2 (7 bit word).

TMC Pipeline delay is (Write pointer - Read pointer)

(0x0D) L1 FIFO empty flags. Used as a diagnostic.

(0x0E) ADC FIFO empty flags. Used as a diagnostic.

(0x0F) L1 FIFO Full flags. Used as a diagnostic.

(0x10) Scanning ADC readback values.

Words 0,1: +5V Digital, Analog power supply (33 mV / count)

Words 2,3: -5V Digital, Analog power supply (33 mV / count)

Words 4..6: External Transducers (100 uV / count)

Word 7: On - board temperature (0.4 °C / count, 0 counts  $\cong$  10 °C)

(0x11) CB control register (see below).

(0x12) CB status register (see below).

(0x13) Sets wire discriminator threshold (1.6mV (at the FEB) per count, 8 bit word).

(0x14) Wire test pulse amplitude setting (16mV per count, 8 bit word).

(0x15) Pad test pulse amplitude setting (16mV per count, 8 bit word).

(0x16) Test pulse frequency setting. Frequency = 47.7KHz/(1 + value).

(0x17) Test pulse delay word.

Bit assignments:

0..3 - Delay tap select 0..9. A value > 9 is saturated at 9 (2 ns per count)

4..6 - RF clock tick within a crossing 0..6. A value > 6 is saturated at 6 (18.8 ns per count)

7 - Not used

8..15 - Crossing number 1..159. A value > 159 is set to 159, a value of 0 is set to 1.

(0x18) Internal CB timing settings.

Word 0: Beam delay value (18.8 ns per count, 5 bit word).

Word 1: Pipeline delay value (18.8 ns per count, 8 bit word).

Word 2: Drift time delay value for Sync Gap (18.8 ns per count, 6 bit word).

Word 3: Pad data transfer gate width value (37.7 ns per count, 6 bit word).

Word 4: Wire data transfer gate width value (37.7 ns per count, 5 bit word).

(0x1B) Multi-block transfer command words.

Word 0: Download FLASH RAM program enable. (Ignored during uploads)

A value of 0 updates SRAM only, a non-zero value will load  
FLASH RAM as well as update SRAM.

Word 1: Source/Destination start address in SRAM.

Note: Address also applies to FLASH if write is enabled, start address must be an  
even multiple of 128. (FLASH page boundary)

Word 2: Multi-block total byte count upper word

Always 0 due to physical RAM size limit.

Word 3: Multi-block total byte count lower word

Limited to the page size of the FLASH RAM - 0x4000.

Word 4: Data Checksum

Word 5: Write Status.

Bit assignments: 0 - Rx, 1 - Tx

Word 6: Read Status.

Bit assignments: 0 - Checksum error, 1 - Multi-block error, 2 - Word count overrun.

(0x1C) Multi-block downloading to SRAM with optional writing to FLASH RAM.

(0x1D) Multi-block uploading from SRAM.

Note: See the Muon group engineering note on multi-block transfer for operational details of this operation.

(0x1E) Internal CB status. Used as a diagnostic.

Control register bit assignments (sub address 0x11):

0..3 - FEB enable bits. Bits 0..3 correspond to FEB 1..4.

Note: The only allowed values for these bits are 1, 3, 7, and 0xF.

4 - Internal test pulser enable. 1 - Enabled. 0 - Disabled.

5..8 - Trig 'OR' Enables. Set to one when FEB n 'OR' out is to contribute to self trigger

9,10,11 - Trigger type select bits.

000: Triggers disabled

001: Data taking. Trigger is from MRC

010: External trigger from CB LEMO input.

011: Trigger is FEB 'OR' inputs

100: Trigger is CB on board test pulse generator

101, 110 and 111: Not used

12 - Not Used.

13 - RF Clock source. 0 - Remote, 1 - Local.

14 - Not Used.

15 - Timing Generator Reset. 1 - Issue reset, 0 - No action.

Status register bit assignments (sub address 0x12):

Bits 0..5 are latched. They can only be cleared by an Init cycle.

0 - L1 Error

1 - L2 Error

2 - FEB Error

3 - L1 Buffer Overflow

4 - L2 Buffer Overflow

5 - L2 Buffer Underflow

6 - L1 Busy

7 - L2 Busy

Bits 8..11 are latched. Writing a 0 to them will clear them, writing a 1 has no effect.

8 - A DSP hardware reset has occurred, either from the watchdog timer or power up.

9 - Readout Controller timeout

10 - Timeout Waiting for MRC Done to go low in response to transmission of L3 data

11 - Event Multiplicity Overflow

12 - Multi-Block 1553 operation in progress.

13 - RF Clock Detect (0 indicates presence of signal)

14 - Encoded timing Detect (0 indicates presence of signal)

15 - Not yet assigned