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PPD/D0 Muon Upgrade

Hardware Release 17.00

D0 Muon Trigger Fanout Card

Technical Specification
(revised)

February 11, 2002

Batavia, Illinois

1. Introduction

The Trigger Fanout Card (TFC) is designed to provide the muon system with an ability to synchronously run several muon crates in local data taking and testing modes. Having the TFC provides the following test features for the muon system:

- ability to simultaneously readout information from different muon detectors for processing on a host computer, thus allowing small scale physics analysis of the data
- ability to run locally all muon sub-systems or any part of the muon system with beam, cosmic ray triggers or pulsers without involving the D0 Trigger Framework (TFW) and the D0 data acquisition (DAQ) systems
- ability to mimic most of the TFW functions using internal TFC sequencer without having the TFW running, which allows for debugging of the muon sub-systems independently

2. System configuration

Fig. 1 illustrates a possible configuration of the muon system using the TFC as a TFW simulator along with the connections between the TFC and the MFC modules. The TFC can generate timing and trigger signals, and supply them to the number of MFCs connected by serial links to the TFC. The HOTLink™ chipset is used to transfer timing and control bits to the MFCs. The TFC itself can use different sources of the timing clock. If beam synchronization is desired, TFW timing received via the SCL serial link is used. All Geographic Sections (GS) with MFCs connected to the TFC can be synchronously triggered and read out.

3. Modes of operation

There are two possible sources of timing synchronization, which the TFC can use:

- Internal timing (**SEQ**)
- External timing (**TFW**)

In the SEQ mode the TFC uses timing signals generated internally by a sequencer that is not synchronized to the accelerator beam. In the TFW mode the TFC generates the same timing signals, but the sequencer is synchronized to the TFW timing decoded by the Serial Communication Link (SCL) daughter card. There are two possible ways to generate trigger signals:

- Internal triggers from pattern memory (**INT**)
- External NIM triggers (**EXT**)

In the INT mode all the trigger information is generated by a pattern memory of the TFC. Trigger information for this mode is stored in a dual port memory and is user programmable via VME interface. In the EXT mode the TFC attaches a proper value of the crossing and turn numbers to the L1 and L2 Accept signals. The L1 signal is generated upon receiving any of the four input trigger signals. L1 and L2 Accept signals are generated sequentially with a programmable delay between L1 and L2 Accepts set by software. There is no provision to generate L2 Reject in the EXT mode.

The TFC also has an internal flip-flop that is set by the external trigger signal or if a number of received external trigger signals exceeds the number of generated L2 Accept signals by 16. It can also be set and reset by a VME command. The output of this flip-flop is a BUSY signal that indicates that the TFC cannot accept more external triggers. The state of the BUSY signal is readable via VME and is indicated by the LED.

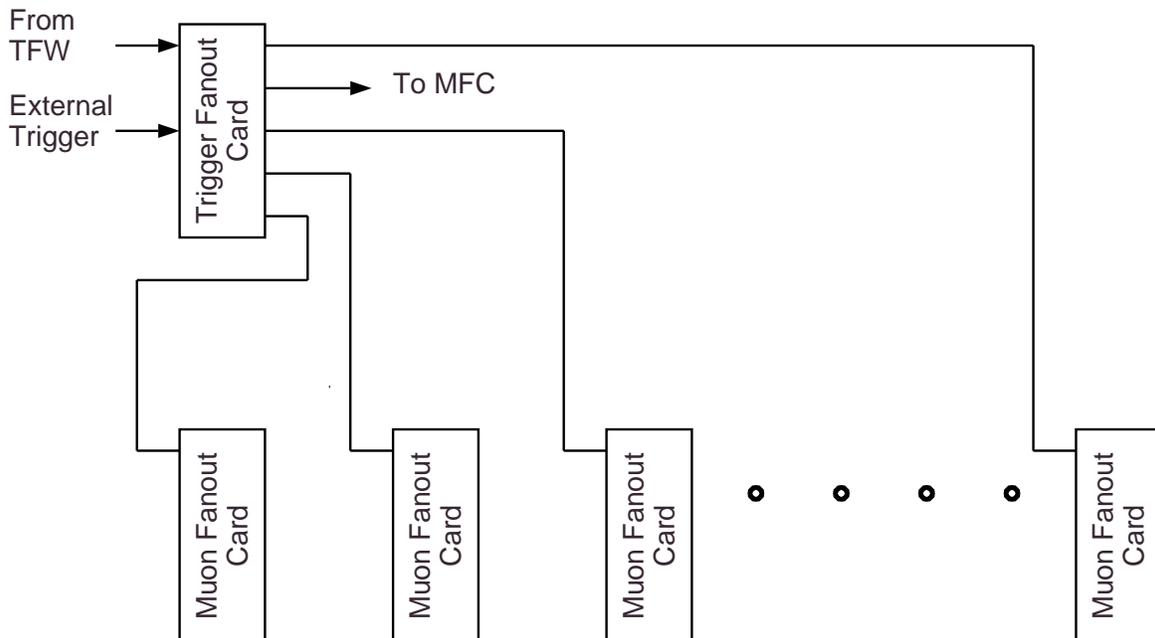


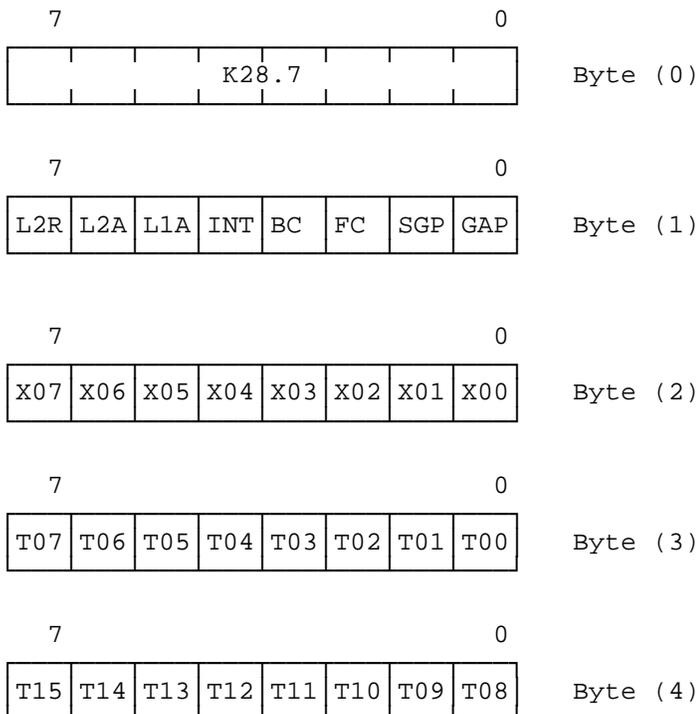
Fig. 1 System Configuration with the TFC.

4. Timing and trigger signals

The TFC sequencer generates the following timing and trigger signals and trigger related information:

- RF - 53.1047 MHz clock
- STR - 7.59 MHz clock
- INIT - Initialization
- FC - First crossing
- BC - Beam crossing (beam is present)
- SGAP - Synch gap (no L1 Accepts are allowed)
- GAP - Gap (no beam, L1 Accepts are allowed)
- L1ACC - L1 Accept
- L2ACC - L2 Accept
- L2REJ - L2 Reject
- T 00..15 - L1/L2 turn number (16-bit word)
- X 00..07 - L1/L2 crossing number (8-bit word)

The TFC's HOTLink transmitter is clocked by 5/7 RF (37.932 MHz) frequency generated by PLL circuit based on Cypress CY7B991 Programmable Skew Clock Buffer chip. The TFC sends five bytes of timing and trigger information via the HOTLink transmitter every 53/7 clock period in the following order:



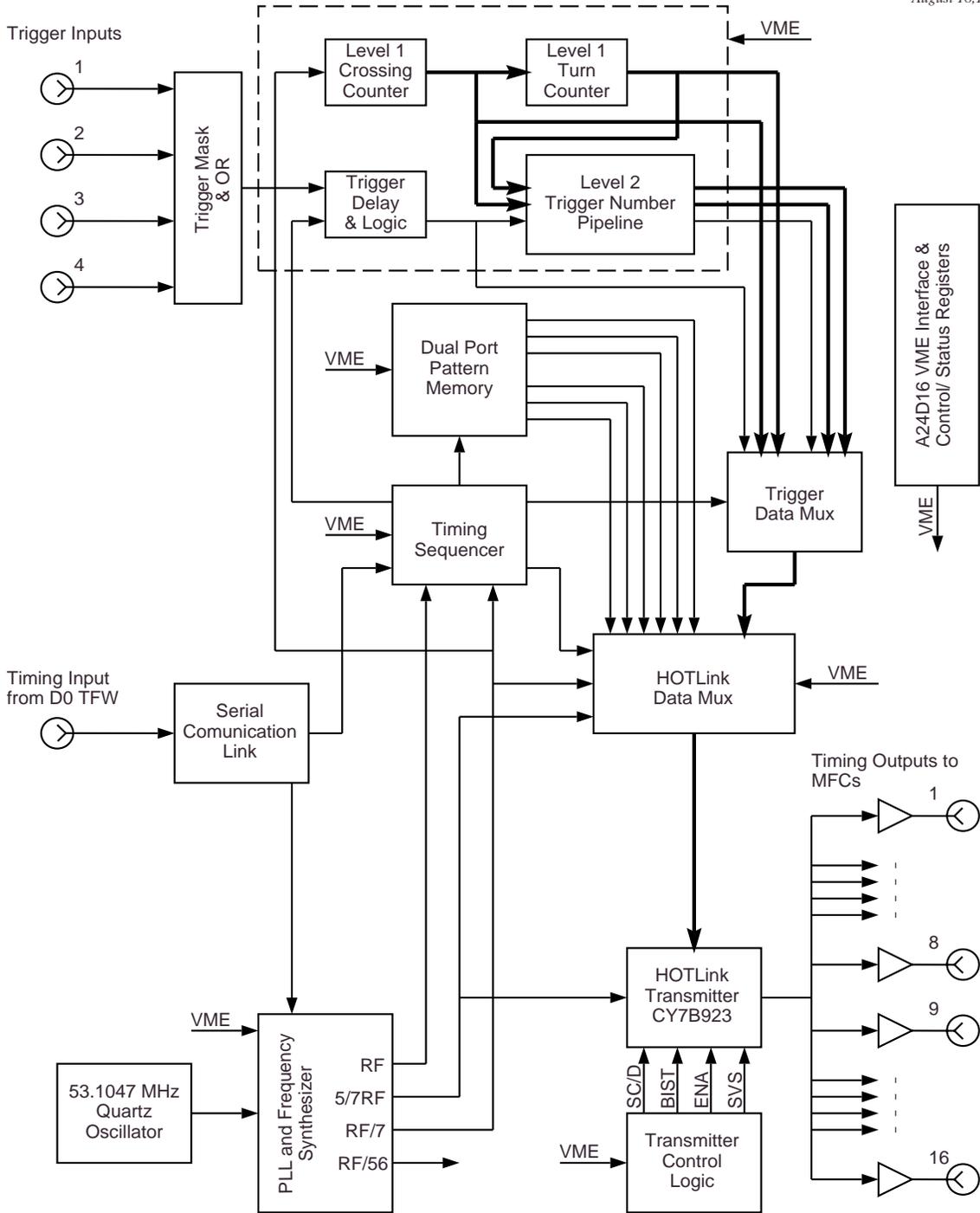


Fig. 2 Trigger Fanout Card block-diagram.

5. TFC block-diagram

A block-diagram of the TFC is shown in Fig. 2. The Timing Sequencer is a source of all timing and control signals. The sequencer is synchronized to 53.1047 MHz quartz oscillator. The internal PLL is used to synchronize it to the external SCL beam timing. In order to preserve beam synchronization of the front-ends, the TFC sequencer is re-synchronized by the SCL First Crossing signal that is offset in such a way that the TFC timing signals received by the front-ends are identical to the original TFW timing. There are two preset registers to provide fine and coarse timing offset to the TFC sequencer. The fine offset has seven steps of 18.9 ns and the coarse offset is done in 132 ns steps. There is a special SYNCR signal, which can be issued by the VME command that forces re-synchronization.

Only 53 MHz clock and 53/7 MHz clock and First Crossing signals are used from the set of SCL timing signals. All other SCL signals are connected to two 34-pin headers for detailed diagnostic using logic analyzer. The TFC has a control/status register, which allows monitoring and controlling of the SCL card. Under normal circumstances after initial setup this register should not be used in order to maintain local status of the SCL connection, but it can be used for debugging of the SCL.

The sequencer drives address lines of the dual port memory (DPM) that is used to generate trigger patterns. The memory is accessible for read/writes via VME interface. The trigger event consists of two 16-bit words. First word is a crossing and turn number, at which trigger is to be generated (actual crossing number has to be one less). The second word is actual trigger data (L1 Accept, L2 Accept, L2 Reject and trigger number). In the internal trigger mode sequencer fetches first word and waits for the specified crossing and turn. At this point it increments DPM address and fetches the next word from the DMP. The trigger data is picked up by the Trigger Mux and sent to the HOTLink Data Mux. The HOTLink Data Mux encodes trigger and timing information into five data bytes as described earlier. There are two bits (Sequencer Enable bit and Run One Cycle bit) available to control the sequencer.

There are four external trigger inputs, which accept NIM level signals. Each of the inputs can be individually masked using VME programmed mask register. The incoming trigger signal causes trigger logic to generate a delayed L1 Accept signal that is sent to the Trigger Mux. The trigger logic can be enabled/disabled by a separate bit in the TFC status/control register. The crossing and turn number attached to this signal are generated by additional crossing and turn counters because they are different from the current sequencer values (see Appendix A). The offset of the Level 1 Crossing and Turn counters is programmed via VME. That same L1 Accept signal is also delayed by the L2 pipeline. At the output of the pipeline this signal becomes an L2 Accept and is sent to the Trigger Mux. The pipeline delay is programmed in 132 ns steps.

The slave VME interface accepts standard 16-bit data and 24-bit address commands (A24:D16). There are total of six read/write registers within the TFC. Some of the bits are write or read only. See Section 8. for details.

6. Pattern memory data format

The pattern memory is accessible via standard VME commands as a 16 Kbyte memory block. The first 16-bit word in memory defines a crossing number and the second 16-bit word defines a turn number of the pointer. The pointer has to be set *one crossing earlier* than actual event, at which a decision is to be generated. The third and fourth 16-bit words define a trigger number and trigger bits of the decision. Bit 15 is added to the third word to simplify memory data decoding. The end of the valid data is marked by a terminator word with bit 11 set to one. There is no checks implemented in the hardware to prevent setting of multiple trigger decision bits. This function has to be performed by the software when downloading pattern memory.

- *Pointer crossing number* (relative address = 0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	X7	X6	X5	X4	X3	X2	X1	X0

X7..X0 - Pointer crossing number

- *Pointer turn number* (relative address = 2)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0

T15..T0 - Pointer turn number

- *Event crossing number* (relative address = 4)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	L2R	L2A	L1A	0	0	0	0	X7	X6	X5	X4	X3	X2	X1	X0

XP7..XP0 - Event crossing number

L1A - L1 Accept bit (1 – true)

L2A - L2 Accept bit (1 – true)

L2R - L2 Reject bit (1 = true)

- *Event turn number* (relative address = 6)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0

T15..T0 - Event turn number

- *Terminator word* (even relative address)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TM	0	0	0	0	0	0	0	0	0	0	0

TM - Terminator bit (1 – true)

7. Mechanical specification

The TFC is a single width VME 9U × 280 mm card. The front panel of the module is shown in Fig. 3.

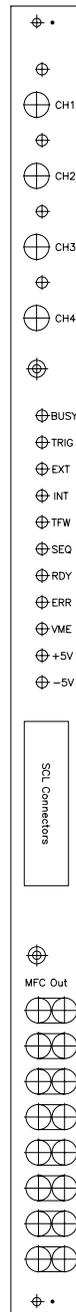


Fig. 3 Trigger Fanout Card front panel.

The front panel has the following elements:

- Fifteen LEDs indicating the following conditions:
 - ✓ EXT(green) - EXT trigger mode indicator
 - ✓ INT (green) - INT trigger mode indicator
 - ✓ TFW (green) - TFW timing mode indicator
 - ✓ SEQ (green) - SEQ timing mode indicator
 - ✓ CH1..4 (green) - Channel Enable indicator (4)
 - ✓ BUSY (green) - TFC cannot accept external triggers
 - ✓ TRIG (green) - External trigger LED indicator
 - ✓ RDY (green) - SCL ready
 - ✓ ERR (red) - TFC hardware error
 - ✓ VME (green) - VME command decoded
 - ✓ +5 (yellow) - +/- 5 V power indicators (2)
- Serial Control Link RF and multiple pin connectors
- Eight MFC external synchronization double LEMO connectors
- Four external trigger LEMO connectors

8. TFC registers

The TFC requires initialization from the VME bus. The following is a list of the internal registers accessible via standard VME commands (the relative hex address shown). By default, all registers support reads and writes unless specifically commented.

- *TFC control register, CSR0 (\$4000)*

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NC	NC	NC	NC	STR	TEN	EXT	SEN	NC	NC	NC	BRS	CLN	SYN	CLT	INIT

- INIT - INIT signal level (0 – low, 1 – high)
- CLT - Clear Trigger Latch (write 1)
- SYN - Synchronize sequencer (write 1)
- CLN - Clear trigger counter (write 1)
- BRS - Board Reset (write 1)
- SEN - Sequencer timing mode (1 – sequencer, 0 – TFW)
- EXT - External trigger mode (1 – external, 0 - internal)

- TEN - Enable external trigger logic (1 – enabled)
- STR - Enable single trigger mode (1 – single trigger mode)

- *TFC status/control register, CSR1 (\$4002)*

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NC	NC	L2E	L2B	L1B	L1E	IAC	ACK	BUS	NC	ERR	SL	DER	SER	RDY	INIT

- INIT - SCL INIT signal (read-only)
- RDY - SCL Ready (read-only)
- SER - SCL Sync Error (read-only)
- DER - SCL Data Error (read-only)
- SL - SCL Sync Lost (read-only)
- ERR - Global TFC error bit (read-only)
- BUS - TFC Trigger logic BUSY (read-only)
- ACK - SCL Acknowledge
- IAC - INIT Acknowledge
- L1E - Level 1 Error
- L1B - Level 1 Busy
- L2E - Level 2 Error
- L2B - Level 2 Busy

- *HOTLink control register CSR2 (\$4022)*

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0	NC	NC	NC	NC	TST	SVS	BSE	TEN

- TEN - Transmitter enable (1 – enable)
- BSE - BIST test enable (1 – enable)
- SVS - Send violation symbol
- TST - Test enable
- TD7..TD0 - Test data pattern

- *Sequencer synchronization preset & control register, CSR3 (\$4024)*

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	NC	NC	1C	ES	NC	FF2	FF1	FF0

- FF2..FF0 - First Crossing fine delay preset (18.9 ns step)
- ES - Sequencer Enable bit (1 – enable, 0 – disable)

- 1C - Run One Cycle control bit (write 1)
- FC7..FC0 - First Crossing coarse crossing counter preset

- *Channel mask and L2 pipeline delay register, CSR4 (\$4028)*

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH4	CH3	CH2	CH1	NC	NC	PD2	PD1	PD0							

- CH1 - Channel 1 Enable
- CH2 - Channel 2 Enable
- CH3 - Channel 3 Enable
- CH4 - Channel 4 Enable
- PD9..PD0 - L2 decision delay preset (1..1023, 132 ns step)

- *Crossing number and trigger delay register, CSR5 (\$402A)*

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NC	NC	LD5	LD4	LD3	LD2	LD1	LD0	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0

- CR7..CR0 - External trigger crossing number preset (1..159)
- LD5..LD0 - External trigger delay (20..63, 132 ns step)

9. Addressing

There are two address segments in the VME address space that are associated with TFC dual port memory and CSR registers. Starting addresses for these segments are given in Table 1. TFC base address (A23..A16) is defined by a DIP switch on the board.

References.

1. Muon TDR D0 Note #3299, August 7, 1997,
http://d0server1.fnal.gov/users/baldin/public/muel_tdr/muon_tdr.pdf

Table 1. Trigger Fanout Card VME Address Map

Starting Address	Size (bytes)	Comment
Card Base Address + 000000	16K	DPM memory
Card Base Address + 004000	2	TFC control register
Card Base Address + 004002	2	TFC status/control register
Card Base Address + 004022	2	HOTLink control register
Card Base Address + 004024	2	Sequencer synchronization preset & control register
Card Base Address + 004028	2	Mask bits and L2 pipeline preset register
Card Base Address + 00402A	2	Crossing number and L2 trigger pipeline register

Appendix A.

Note on MFC/TFC timing

This note describes a few aspects of Muon Fanout Card (MFC) and Trigger Fanout Card (TFC) timing issues. It is necessary to understand relative timing for all the elements of the muon system in order to design and set it up properly. Typical diagram of the muon system timing is presented in **Figure 1**.

MFC is a source of all timing signals for the entire Geographical Section (GS). Possible inputs to the MFC are TFW timing, internal sequencer and TFC timing. TFC timing can be synchronized to the TFW timing or be independent. The goal for the TFC design is to minimize setting changes when switching from TFW timing to TFC timing and back.

Expected difference between TFW and TFC timing relative to the beam is equal to the propagation delay from MFC to TFC and back. It is preferable to avoid timing adjustment delays in front-ends when switching from TFW timing to the TFC timing. **Figure 1** assumes no difference between timing sources mentioned above.

Timing sequence generated by MFC arrives at front-end (FE) location after *Cable delay 1* that includes cable delay between MCH and FE and, also, FE beam adjustment delay. At this point timing is synchronized to the beam. When event occurs, event data is stored in the FE pipeline and also trigger signal is send up to the MCH to signal TFC that event needs to be readout. In our example, this happens at crossing number six. (see FE timing in **Figure 1**).

The trigger signal will be delayed by *Cable delay 2* while it is propagating to the TFC location. TFC will have an internal adjustment delay to compensate for big FE pipeline delay set to the Level 1 decision time. The TFC internal delay will eliminate re-adjustment of the pipelines when timing is switched to the TFC timing. The delay will have fine settings 0 to 7 in 53 MHz steps and coarse settings 0 to 4.8 μ s in 53/7 MHz steps. The delay settings have to be adjusted that way, that setup and hold for logic generating L1 Accept signal associated with the trigger are fully satisfied.

L1 Accept signal arriving at the FE location will have to meet data flowing out of the pipelines at delayed crossing number six if all the settings are correct. The data will then be registered and transferred to the MCH via standard muon data interface. Observing **Figure 1**, one can derive simple equations describing relationship between different settings.

$$P \text{ min} = T_{cab1} + T_{cab2} \text{ (1),}$$

where P is pipeline delay, Tcab1 and Tcab2 are cable delays.

$$D = P - (T_{cab1} + T_{cab2}) \text{ (2),}$$

where D is TFC delay and the other members are the same as in equation (1).

$$\mathbf{DX = XTFC - (Tcab1 + Tcab2) \text{ (3)}}$$

where DX is crossing counter offset necessary to generate correct crossing number for L1 Accept, $XTFC$ is TFC crossing number at the time of trigger arrival, and the other members are the same as in equation (1).

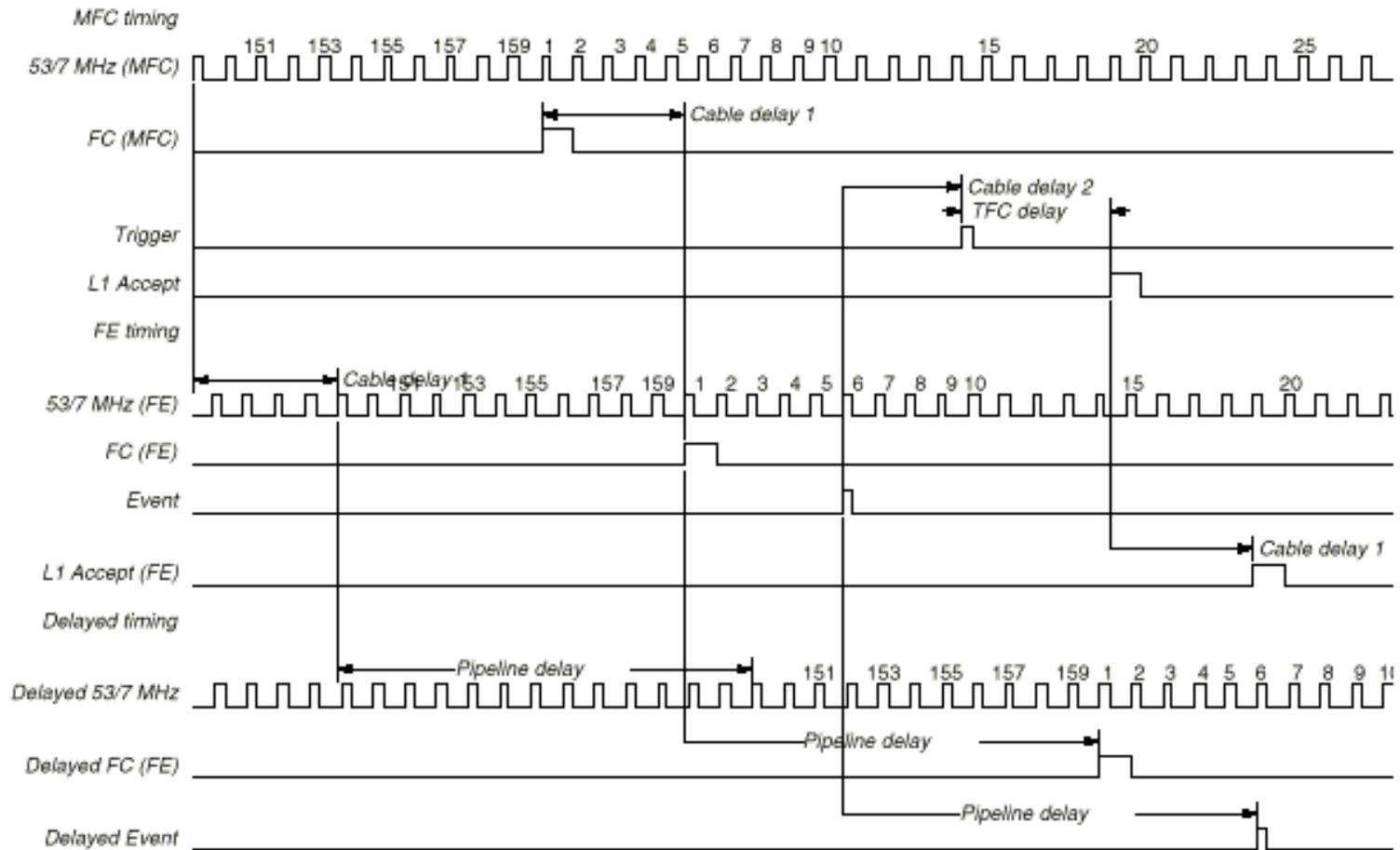


Figure 1. Muon System Timing Diagram.