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A memory map of PDT parameters to be downloaded via 1553 interface

1. Hardware Parameters *(internal RAM address for current value is shown)*

0x200: Tgate. Bits 0..5:Trigger gate width (18.8ns per bin). Bits 6,7:Pad and Wire test pulse enable. Default = 0xD0

15..8	7	6	5	4	3	2	1	0
Not Used	PttstEn	WttstEn	TGT5	TGT4	TGT3	TGT2	TGT1	TGT0

0x201: Run Control for FEB1. Default = 0xF

15..5	4	3	2	1	0
Not Used	Q Int Reset En	Pad Enable	Wire Enable	Pad ADC Run	Wire TDC Run

0x202: Run Control for FEB2. Default = 0xF

15..5	4	3	2	1	0
Not Used	Q Int Reset En	Pad Enable	Wire Enable	Pad ADC Run	Wire TDC Run

0x203: Run Control for FEB3. Default = 0xF

15..5	4	3	2	1	0
Not Used	Q Int Reset En	Pad Enable	Wire Enable	Pad ADC Run	Wire TDC Run

0x204: Run Control for FEB4. Default = 0xF

15..5	4	3	2	1	0
Not Used	Q Int Reset En	Pad Enable	Wire Enable	Pad ADC Run	Wire TDC Run

0x205: Channel Enables for FEB1. Default = 0xFFFF

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEB1 Channels 0..15															

0x206: Channel Enables for FEB1/2. Default = 0xFFFF

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEB2 Channels 0..7								FEB1 Channels 16..23							

0x207: Channel Enables for FEB2. Default = 0xFFFF

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEB2 Channels 8..23															

0x208: Channel Enables for FEB3. Default = 0xFFFF

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEB3 Channels 0..15															

0x209: Channel Enables for FEB3/4. Default = 0xFFFF

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEB4 Channels 0..7								FEB3 Channels 16..23							

0x20A: Channel Enables for FEB4. Default = 0xFFFF

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEB4 Channels 8..23															

0x20B: CB_Ctrl[1,3] Default = 0x20F

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Tmg Rst	Not Used	Clk Rem/Loc	Not Used	Trig Type			Self Trig "OR" Enables				Pulser Enable	FEB Enables			

0x20C: Not used

0x20D: Wire test pulse height Default = 0x80;

15..8	7	6	5	4	3	2	1	0
Not Used	DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0

0x20E: Pad test pulse height Default = 0x80;

15..8	7	6	5	4	3	2	1	0
Not Used	DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0

0x20F: Wire Threshold Default = 0x20;

15..8	7	6	5	4	3	2	1	0
Not Used	DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0

0x210: ADC Pipeline Length[1] (75.32 ns/bin) Default = 0x3C;

15..6	5	4	3	2	1	0
Not Used	ADCPL5	ADCPL4	ADCPL3	ADCPL2	ADCPL1	ADCPL0

0x211: TMC Read pointer initial value[1] (37.7ns per bin). Default = 0;

15..8	6	5	4	3	2	1	0
Not Used	RP6	RP5	RP4	RP3	RP2	RP1	RP0

0x212: TMC Write pointer initial value[1] (37.7ns per bin). Default = 0x78;

15..8	6	5	4	3	2	1	0
Not Used	WP6	WP5	WP4	WP3	WP2	WP1	WP0

0x213: Pulser prescale value (1 Turn/bin). Default = 0;

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(Turns - 1) between test pulses															

0x214: Pulser Delay Value. Default = 0x2830;

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Crossing # (1..159)								Not Used	RF Tick in crossing (0..6)			2ns Delay tap (0..9)			

0x215..0x217: Not used

0x218: Beam Delay (18.8 ns/bin). Default = 2;

15..5	4	3	2	1	0
Not Used	Bdly4	Bdly3	Bdly2	Bdly1	Bdly0

0x219: Crossing Counter Pipeline Delay (18.8 ns/bin). Default = 0xE0;

15..8	7	6	5	4	3	2	1	0
Not Used	Pldly7	Pldly6	Pldly5	Pldly4	Pldly3	Pldly2	Pldly1	Pldly0

0x21A: Sync Gap Delay (131.8 ns/bin). Default = 4;

15..4	3	2	1	0
Not Used	SgapDly3	SgapDly2	SgapDly1	SgapDly0

0x21B: Pad Transfer Gate Width (37.7 ns/bin). Default = 0x29;

15..6	5	4	3	2	1	0
Not Used	Pxfer5	Pxfer4	Pxfer3	Pxfer2	Pxfer1	Pxfer0

0x21C: Wire Transfer Gate Width (37.7 ns/bin). Default = 0x15;

15..5	4	3	2	1	0
Not Used	Wxfer4	Wxfer3	Wxfer2	Wxfer1	Wxfer0

0x21D..0x21F: Not used

2. Software Parameters[2] *(internal RAM address for current value is shown)*

0x220: Module ID

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						Layer		Barrel				Octant			

0x221: No. of Front End Boards (FEBs)[3]. Default = 3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
													#FEBs (1..4)		

0x222: PDT Wire Length (100ps)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDT Wire Length (L + 10ns[100ps/bin])															

0x223: Calibration Constant Set ID

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					Calibration const. Set ID										

0x224: Alignment Constant Set ID

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Alignment const. set ID															

0x225: Alignment Constant : x/y offsets

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	Y offset distance (100 μm)							sign	x offset distance (100 μm)						

0x226: Alignment Constant : z/theta offsets

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	Z offset distance (100 μm)							sign	theta offset (10 μrad)						

0x227: Alignment Constant : phi/psi offsets

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sign	phi offset (10 μrad)							sign	psi offset (10 μrad)						

0x228..0x287: Channel Table[4]: Up to 96 16-bit words (one for each wire).

0x288..0x2E7: Wire T_Zeros[4] : Up to 96 16-bit words (one for each wire).

0x2E8..0x3A7: Pad Gains[4]: Up to 192 16-bit words for gains (two for each wire).

Notes:

1) The hardware arrangement requires that these parameters be updated only during INIT.

2) These parameters are loaded to the DSP memory only during INIT.

3) The number of FEBs is shown in two places. At INIT, the lower order four bits of CB_Ctrl (0x20B) are interpreted and the result is written into No of FEBs (0x221).

4) These sections of the parameter list must have a fixed length. In addition, values for a particular channel occupy the same memory locations regardless of the type and number of FEBs connected to the CB. Unused locations are ignored and may be padded with zeroes.