

## MRC STATUS REGISTER MANUAL

The original MRC status bit map (that can be found in MUON READOUT CARD SPECIFICATION dated 06/04/96) has been changed to accommodate software requirements. The new map is shown in **Table 1**. The byte swap within MRC required by 16-bit data format and Big Endian Motorola data addressing format is shown in columns 1 and 2. The following is a brief description of bit functions and their suggested use. 32-bit registers for both A and B sections can be read as either 16- or 32-bit VME data word (see VME data bits, column 1). Generally, first 16-bit word is read-only status word and second 16-bit word is a combination of read-only write-only and read/write bits.

VME bits 0..15 (read-only):

- TOUT\_DSTR bit is set, when data stream flip-flop is set for the longer than 4 ms time interval. Typically this means that Control Board did not complete data transfer and 'hangs'. This condition causes ERROR2 bit to be set.
- RVS\_DSTR bit is set during data transfer only and indicates unstable operation of the HOTLink chips. The data received has to be considered erroneous and has to be flagged properly. This condition causes ERROR2 bit to be set.
- OVF\_DSTR bit is set, when data address counter reaches 8 KByte boundary. The data received has to be considered erroneous and has to be flagged properly. This condition causes ERROR2 bit to be set.
- RVS\_BIST bit is set, when violation symbol is received during BIST test. This typically means that HOTLink chips do not work reliably.
- TOUT\_BIST bit is set, if BIST test was not completed within 4 ms. This typically means that HOTLink chips do not work reliably. This bit has to be checked by initialization software to insure proper BIST testing.
- TOUT\_REFR bit is set, if HOTLink receiver was not re-framed within 7 clock cycles from rising edge of REFRAM. This bit has to be checked by initialization software to insure proper reframe procedure.
- ZILOG SCC interrupt bit. It has not been tested yet.
- Bit 7 is not used in current version of the MRC. It will be implemented in the next version to eliminate floating data on it.
- CONN bit shows status of the HOTLink connection. It is on, if HOTLink receiver sees any transitions on its input.
- DSTREAM bit is set during data transmission by K28.0 control character and reset by K23.7 control character. The duration of this signal is equal to data transfer time.
- DONE bit indicates status of DONE line. DONE high indicates that MRC is ready to receive an event. DONE low means MRC is not accepting any events. DONE is by the raising edge of DSTREAM and reset by software command.
- SSRQ bit is Service Request status bit.

- BUSY1 is a status bit. The BUSY1 signal is coming from Control Board.
- BUSY2 is a status bit. The BUSY2 signal is coming from Control Board.
- ERROR1 is a status bit. The ERROR1 signal is coming from Control Board.
- ERROR2 is a status bit. The ERROR2 is logical OR of Control Board ERROR2 signal and internal MRC errors. MRC errors included in this status bit are TOUT\_DSTR, RVS\_DSTR and OVF\_DSTR.

VME bits 16..31 (read-only, read/write and write-only):

- ERROR1 test read/write bit allows to set and reset ERROR1 bit and appropriate J2 line. ERROR1 mask bit doesn't affect operations of this bit.
- ERROR2 test read/write bit allows to set and reset ERROR2 bit and appropriate J2 line. ERROR2 mask bit doesn't affect operations of this bit.
- SRQ test read/write bit allows to set and reset SRQ bit and appropriate J2 line. SRQ mask bit doesn't affect operations of this bit.
- RESET write-only bit clears all error and status bits and HOTLink control logic.
- REFRAM write bit starts reframe mode of HOTLink receiver. To insure proper status bits values, this operation can only be done, when Control Board transmitter is sending K28.5 pad characters. If reframe is successful, REFRAM read bit will be set to one, otherwise TOUT\_REFR error bit will be set.
- BIST write bit starts Built-In-Self-Test of HOTLink receiver. Control Board transmitter BIST mode has to be set on prior setting this bit. If receiver runs without errors for 7 BIST loops, BIST read bit is set to one. This procedure takes about 24  $\mu$ s and has to be included in initial setup routine after power-up. If BIST was unsuccessful for more then 4 ms, TOUT\_RVS error bit is set. The RVS\_BIST error bit is set during this procedure, if any violation symbols received.
- DSET write-only bit sets DONE signal high. This has to be done by software after event data has been read out.
- SRQ\_RES write-only bit resets service request flip-flop. This command has to be part of the interrupt service routine. The SRQ flip-flop is set by the trailing edge of DSTREAM and indicates that the data is ready.
- D00 and D01 bits are read-only and are used to differ A and B sections of the MRC. For A section CSR these bits are set to one decimal and for B section CSR they are set to two decimal. This is a debugging aid for software.
- D02 is read/write service request mask bit.
- D03 read-only bit is set to 0 in this version of the MRC.
- D04 is read/write BUSY1 mask bit.
- D05 is read/write BUSY2 mask bit.

- D06 is read/write ERROR1 mask bit.
- D07 is read/write ERROR2 mask bit.

**Table 1**

MUON READOUT CARD CONTROL/STATUS REGISTER

Data	Data	WRITE		READ	
Vbit#	Ibit #	NAME	REMARKS	NAME	REMARKS
0	24	-	-	TOUT_DSTR	Timeout during Data Transfer
1	25	-	-	RVS_DSTR	RVS during Data Transfer
2	26	-	-	OVF_DSTR	OVF during Data Transfer bit
3	27	-	-	RVS_BIST	RVS during BIST bit
4	28	-	-	TOUT_BIST	Timeout during BIST
5	29	-	-	TOUT_REFR	Timeout during Reframe
6	30	-	-	INTSCC	SCC Interrupt status bit
7	31	NC	NC	NC	NC
8	16	-	-	CONN	HOTLink Connection status
9	17	-	-	DSTREAM	HOTLink Data Transfer status
10	18	-	-	DONE	DONE status bit
11	19	-	-	SSRQ	SRQ status bit
12	20	-	-	BUSY1	BUSY1 status bit
13	21	-	-	BUSY2	BUSY2 status bit
14	22	-	-	ERROR1	ERROR1 status bit
15	23	-	-	ERROR2	ERROR2 status bit
16	8	D08	ERROR1 test bit (write 0,1)	D08	ERROR1 test bit
17	9	D09	ERROR2 test bit (write 0,1)	D09	ERROR2 test bit
18	10	D10	SRQ test bit (write 0,1)	D10	SRQ test bit
19	11	RESET	Reset HOTLink Control Logic and status bits	NC	NC
20	12	REFRAM	Reframe HOTLink	REFD	HOTLink reframe status bit
21	13	BIST	Set HOTLink BIST mode	BISOK	HOTLink BIST status bit
22	14	DSET	DONE reset bit (write 1)	NC	NC
23	15	SRQ_RES	SRQ reset bit (write 1)	NC	NC
24	0	-	-	D00	CSRA=1, CSRB=0
25	1	-	-	D01	CSRA=0, CSRB=1
26	2	D02	Service Request Mask bit	D02	Service Request Mask bit
27	3	-	-	D03	0
28	4	D04	BUSY1 Mask bit	D04	BUSY1 Mask bit
29	5	D05	BUSY2 Mask bit	D05	BUSY2 Mask bit
30	6	D06	ERROR1 Mask bit	D06	ERROR1 Mask bit
31	7	D07	ERROR2 Mask bit	D07	ERROR2 Mask bit

Notes:

1. Vbit# indicates VME Data Bus bit.
2. Ibit# indicates MRC internal data bus bit.
3. Bit 31 is not used in this prototype due to hardware limitations.