

D0 Muon Readout Card (MRC2) Design Specification

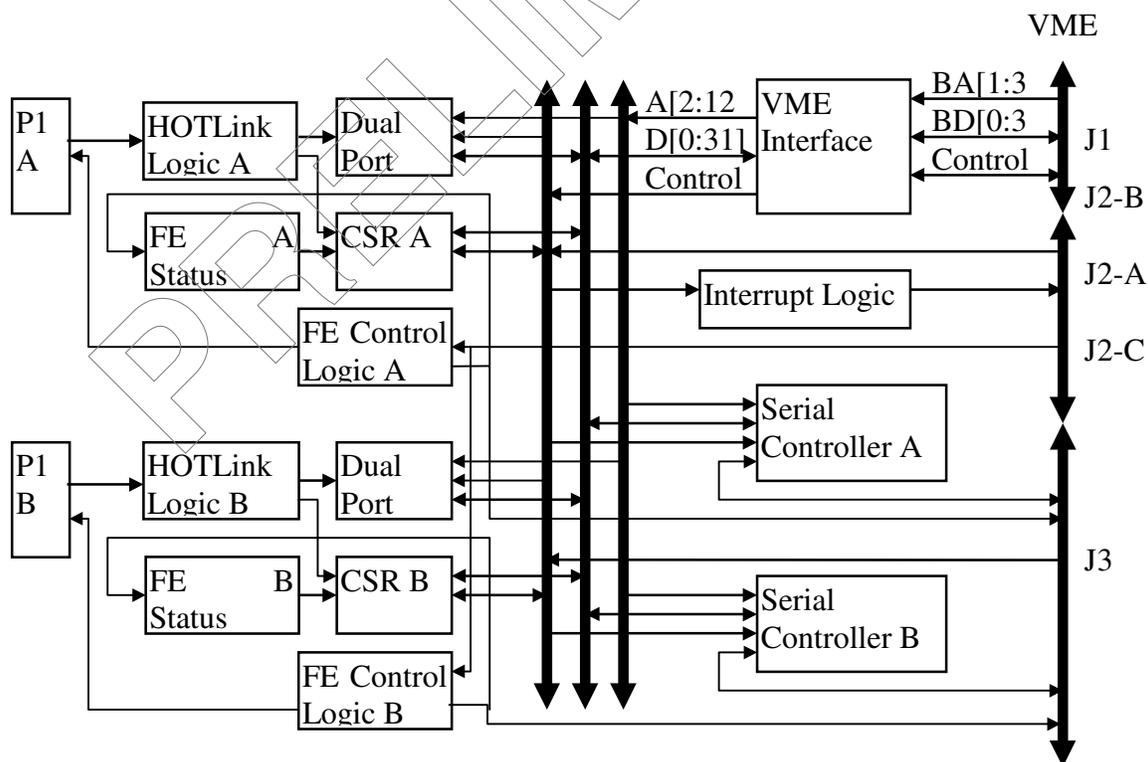
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INTRODUCTION

Purpose

The Muon Readout Card (MRC) is a part of D0 Muon Readout System and resides in the Movable Counting House (MCH). It will be located in existing 9U X 280mm VME crates with custom back-planes. Having only sequential logic and no processor the MRC will perform the following functions:

- Receives data from front-end electronics (FE) and buffers it in internal RAM;
- Sends Control signals to digital signal processor (DSP) in FE via universal asynchronous receiver/transmitter (UART);
- Transfers timing and control signals from MUON FANOUT CARD (MFC) to FE and status information from FE to MFC.



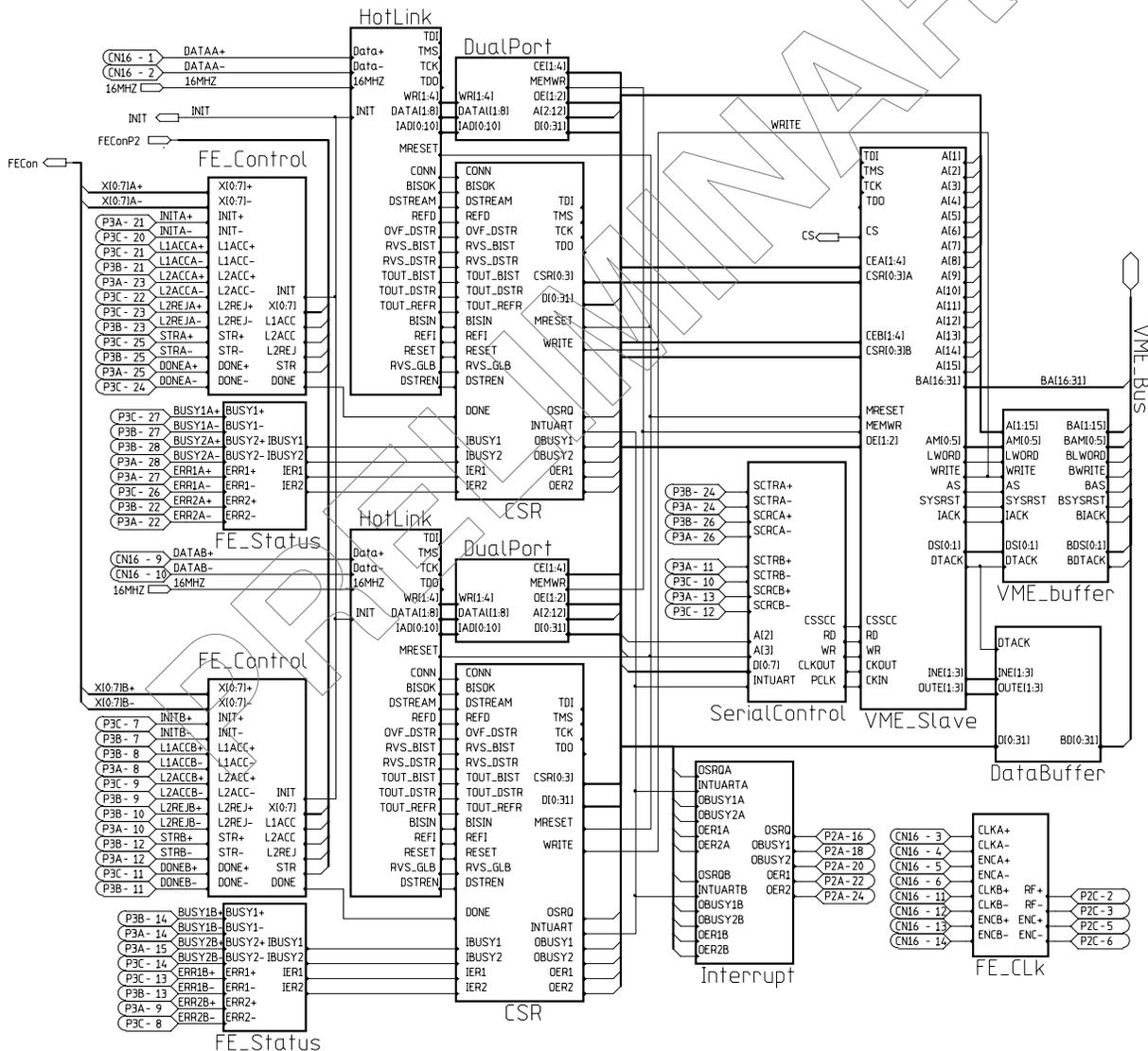
MRC Block Diagram

Functional Block Description

Each MRC connects to two FE data sources and consists of the following functional units:

- HOTLink Receiver CY7B933 and its Control Logic;
- 8K byte Dual Port RAM;
- Status Receivers from FE;
- Control Transmitters to FE;
- 2-channel High-Speed Serial Communication Controller AM85C30;
- 32 bit Control/Status Register;
- VME Slave Interface.

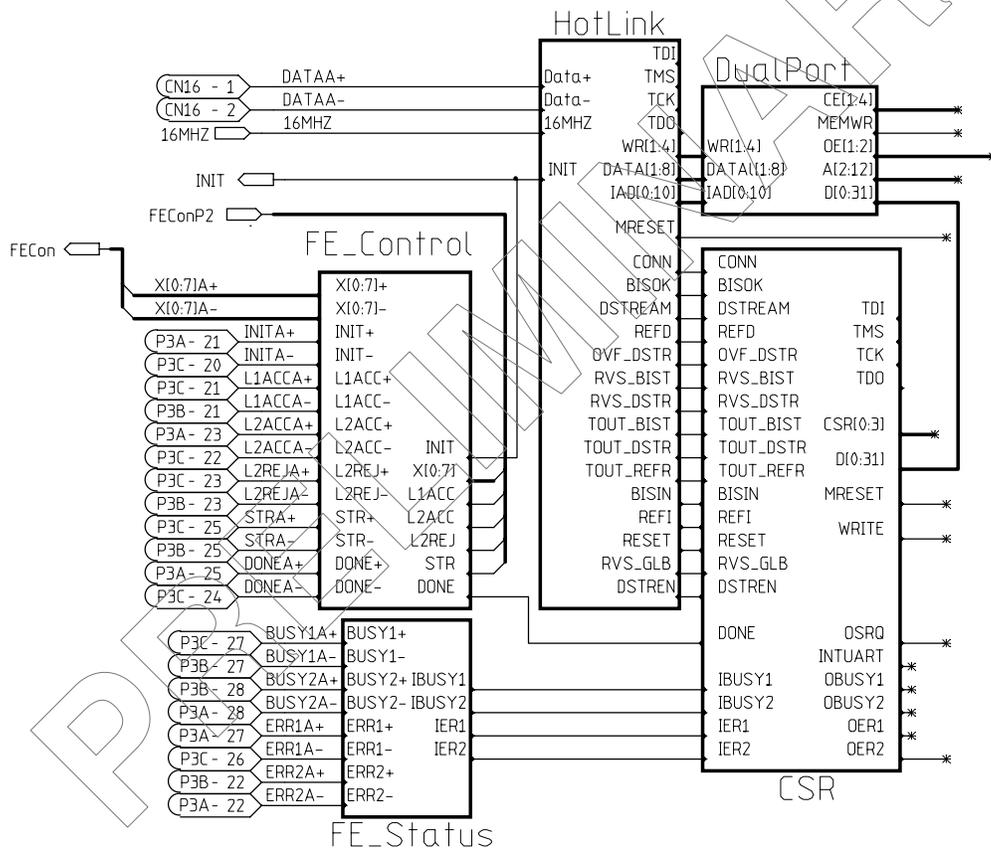
The above basic block diagram shows that there are two nearly independent interfaces on the MRC. Each interface is used to pass control signals to the FE modules and receive status information from them. The CSR registers, Dual Port Rams, and Serial controller can be read and written from the VME bus. The following is a detailed block diagram of the MRC.



MRC Detailed Block Diagram

It shows most of the signals, which connect the functional blocks. For the most part the two FE channels are supported independently except for the common use of one serial interface chip and common interrupt logic. The VME interface is also a common path. Although data may arrive independently, it must be read out over the common data bus by a VME crate master. There is no local processor on the MRC so all data readout is of the *raw* data from the FE. It is the VME crate master's job to monitor and control the MRC data buffers.

The MRC responds to the standard VME bus cycles via the J2 and J1 connectors. The FE connects to the MRC through two cables. The first is located on the front panel of the MRC. This is a 20pin connector, which mates to an AMP Coaxial Ribbon Cable, which splits into two cables to connect to 2 FE modules. The other path to the FE is through the J3 VME connector. The MRC receives and sends signals to the J3 connector, which are then split by the custom backplane into two 50 pin connectors which mate to 50 pin ribbon twist-n-flat cables. These cables then connect to two different FE modules. The MRC also communicates with the MFC via the J2-A and J2-C rows of the VME connector. The following drawing shows the logic for a single FE channel connection.



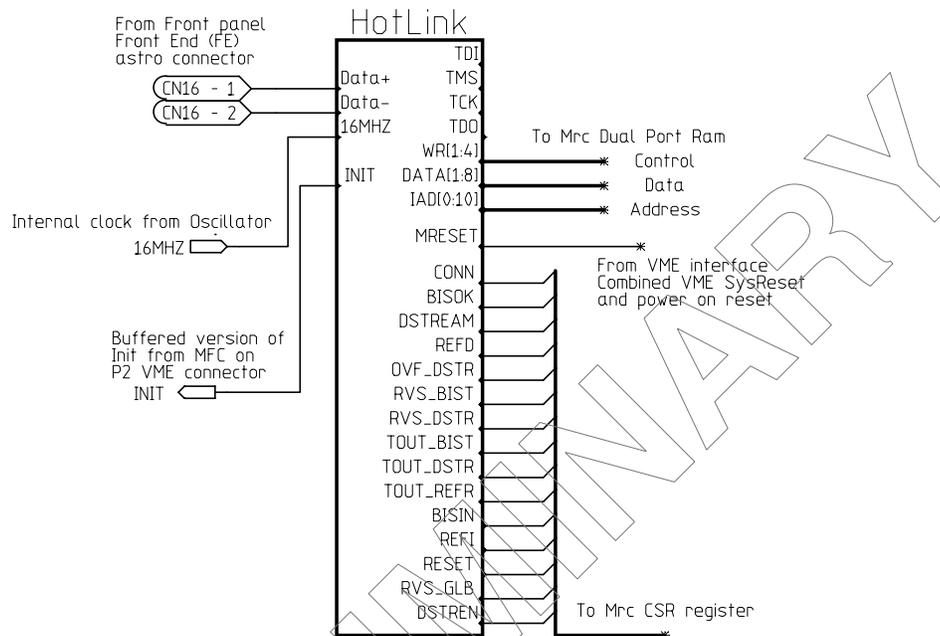
Single Channel FE Interface Block Diagram.

Each FE can communicate with the system through the MRC using predefined status and control signals, HOTLink interface and Serial interface. The MRC simply relays the status and control by converting signals to differential enabling the signals to driving cables for long runs. Incoming signals are received differentially and then routed to the backplane for the MFC to detect. Some information is stored in the CSR register and is accessible by way of VME. Each of the sections will be described in the following pages.

DESCRIPTIONS OF SUBSECTIONS

HOTLink RECEIVER CY7B933

HOTLink Receiver CY7B933 in MRC and HOTLink Transmitter CY7B923 in FE unit are point-to-point serial link for transferring data at 160 Mbit/sec in one direction from FE to MRC. The basic block for the HOTLink receiver and control is shown below.

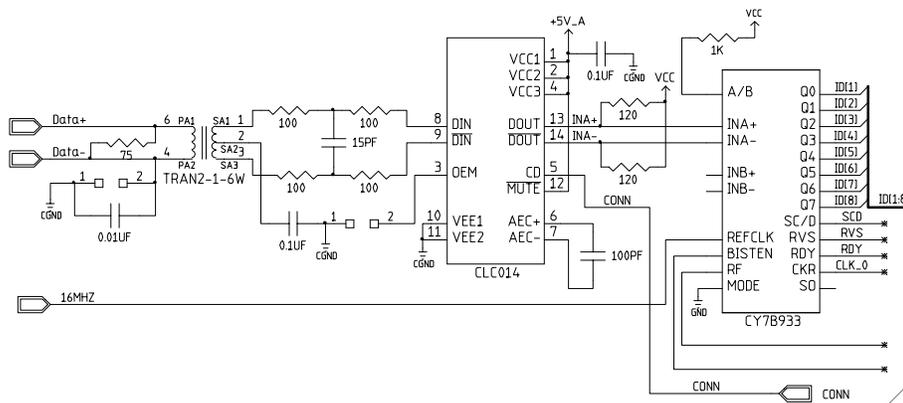


HOTLink Receiver and control logic block.

Eight bits of data are loaded into the HOTLink Transmitter on the FE then the serial data is shifted out of the differential Positive ECL (PECL) serial port at a bit rate which is 10 times the reference clock. The FE boards are connected to the MRC with ribbon coaxial cable where the distance between FE boards and MRC is about 280 ft. One ALTERA EPM7128S is needed to control the HOTLink. Many of the outputs of the HOTLink control chip go to the CSR for that channel. The VME has no direct connection to the HOTLink except through the ALTERA EPM7128S control chip.

At the MRC the signal is transformer coupled to a Comlinear CLCO14 cable equalizer chip, which then drives the HOTLink receiver input. The following figure shows the HOTLink receiver logic. The DATA+/- signals come from the 20 pin front panel connector. The DATA- pin can optionally be connected to GND. The reference clock frequency for the clock/data synchronizer is 16 MHz. A low on the Data Output Ready (RDY) pin of HOTLink Receiver indicates that new data has been received and is ready to be written to RAM. A missing pulse on RDY shows that the received data is the null character (normally inserted by the transmitter as a pad between data transfers).

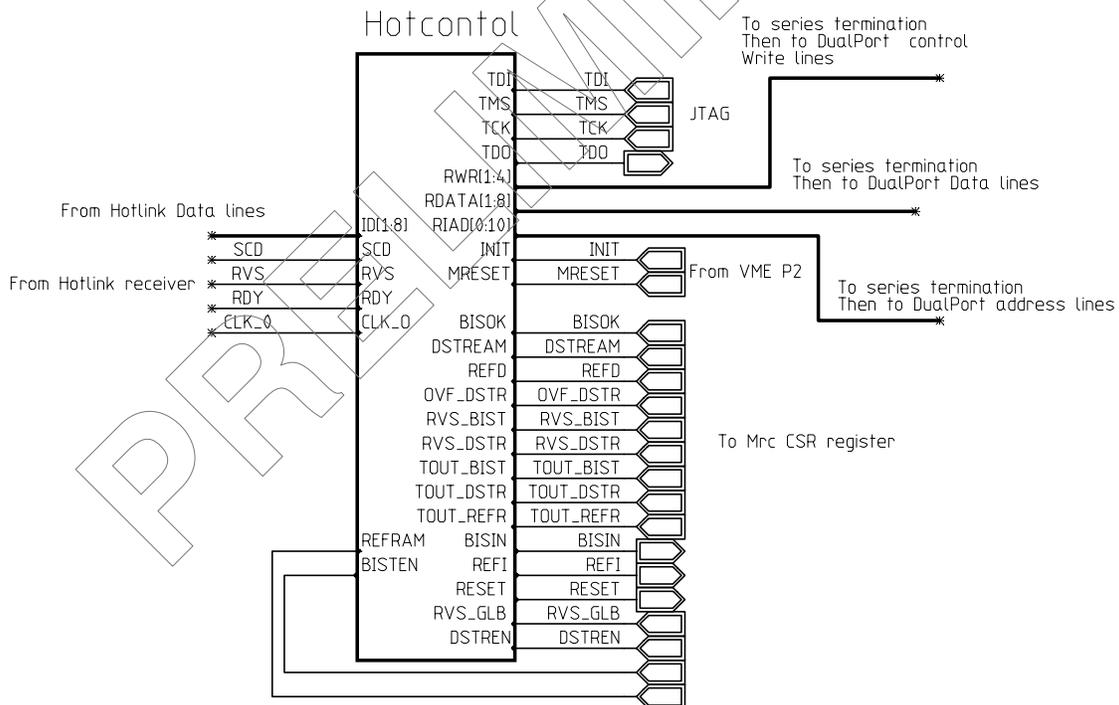
The data outputs (Q0-Q7, SC/D and RVS) all transition simultaneously, and are aligned with RDY and CKR within timing specification to interface directly with external memory. The data from the HOTLink must first pass through the ALTERA EPM7128S control chip before being written to a Dual-Port RAM.



HOTLink Receiver circuit.

HOTLink CONTROL

The HOTLink Control Logic is contained in one EPLD for each FE and is implemented with EPM7128S chips.



HOTLink Control Chip.

The HOTLink Control Logic contains an internal 8-bit register for the HOTLink Q0-Q7 data signals which is clocked by the RDY pulse, 12-bit RAM Address Counter which is used to address the Dual-Port RAM, 16-bit Time-out Counter, and other HOTLink control and interface logic. The MRC uses a

REFCLK of 16MHz. This gives an internal clock period to the HOTLink of 160 MHz. The single bit period would then be 6.25ns. At these rates the ID[1:8], SCD, and RVS have a minimum of 3.25ns of valid hold time after the RDY transition to high.

- **DSTREAM**

The DSTREAM Trigger is set on receipt of a K28.0 character. It is reset on receipt of a K23.7 character, time-out condition, MRESET and RESET pulse from CSR.

K28.0 = ID[1:8]= 0H, SCD= 1, RDY= 0
 K23.7 = ID[1:8]= 8H, SCD= 1, RDY= 0

DSTREAM will clock high on the rising edge of RDY after the receipt of the K28.0 word. It will remain high until reset. Reset is asynchronous and will occur on the falling edge of RDY when a K23.7 is detected.

- **RIAD[0:13]**

The Dual port RAM Address Counter is increased on the edge of the RDY pulse. DSTREAM must be present for the address to increment. REFRAME must be high and BISTEN must be low for the RAM Address Counter to count. Overflow of the RAM Counter (RIAD13=1) disables the assertion of WR1-WR4 signals to RAM and further counter increasing. RIAD13=1 also sets the OVF_DSTR trigger bit in the CSR. Four RAM Write signals WR1-WR4 are caused from RIAD0-RIAD1 and CLK_0 signal. The sequence is WR3, WR4, WR1 and WR2.

- **INIT**

INIT pulse (62.5ns. width at 16 MHz clock) is generated on INIT signal from TFW only when current Data Transfer had finished (DSTREAM=0) or Data Transfer had not finished (DSTREAM=1) (erroneous situation), but time-out period had expired. The time-out is determined by the 16-bit Time-out counter. The INIT signal is received from the J2 VME connector. All MRCs receive it in parallel in the crate. The next CLK_0 from the HOTLink will cause the INIT to be latched until the next CLK_0 or a RESET from CSR or a MRESET (master reset) from VME.

- **REFRAM**

The REFRAM signal is sent to the HOTLink chip to force a re-frame cycle. Upon generating REFI pulse from CSR by software the REFRAM trigger is sent to the HOTLink to initiate framing. Four delay elements (based on triggers) are designed to examine the RDY pin only after the 7-clock cycle delay (see HOTLink description). The RDY signal coming after this delay sets the REFD trigger (separate bit to CSR indicating the re-frame ended) and resets the REFRAM trigger. If re-frame status is not detected after seven clock cycles TOUT_REFR bit is set indication error condition.

- BISTEN

In Built-In-Self-Test (BIST) Mode, upon receiving BISIN pulse from CSR the BISTEN trigger is reset and BISTEN signal to HOTLink Receiver CY7B933 becomes active (low). This means that BIST is in progress. The BIST loop itself consists of 511 bytes transfer (see HOTLink description). The procedure of REFD generating in BIST Mode is the same as discussed above on INIT. In this case the BISTEN trigger is set (and BISTEN becomes inactive) after two clock cycles.

If there were no violation symbols during BIST, the BISOK trigger is set on RDY transfer from LOW to HIGH at the end of BIST and active HIGH bit BISOK means that BIST had passed without errors.

- Time-out Counter

The 16-bit Time-out Counter (time-out period is equal to approximately 4 ms in our case) is incremented on CK_O clock signal from CY7B933 when DSTREAM or BISTEN are active during data transfer or BIST. This counter is reset after MRESET, RESET pulse from CSR, K27.3 character receiving after successful data transfer and setting BISTEN inactive. If Time-out Counter is not reset after normal termination of current operation, the TOUT Trigger is set in 4 ms. The separated condition bits of time-out sources (TOUT_DSTR and TOUT_BIST) are available in CSR.

If the violation symbol was received during DSTREAM or BIST (RVS signal from CY7B933 was active) the corresponding bit to CSR (RVS_DSTR or RVS_BIST) is set.

Short CY7B933 Description

For a detailed description of the HOTLink devices, refer to the CYPRESS data sheets. Here the devices are described only briefly. The HOTLink Receiver accepts the serial bit stream at its differential line receiver, and, using a completely integrated PLL clock synchronizer recovers the timing information necessary for data reconstruction.

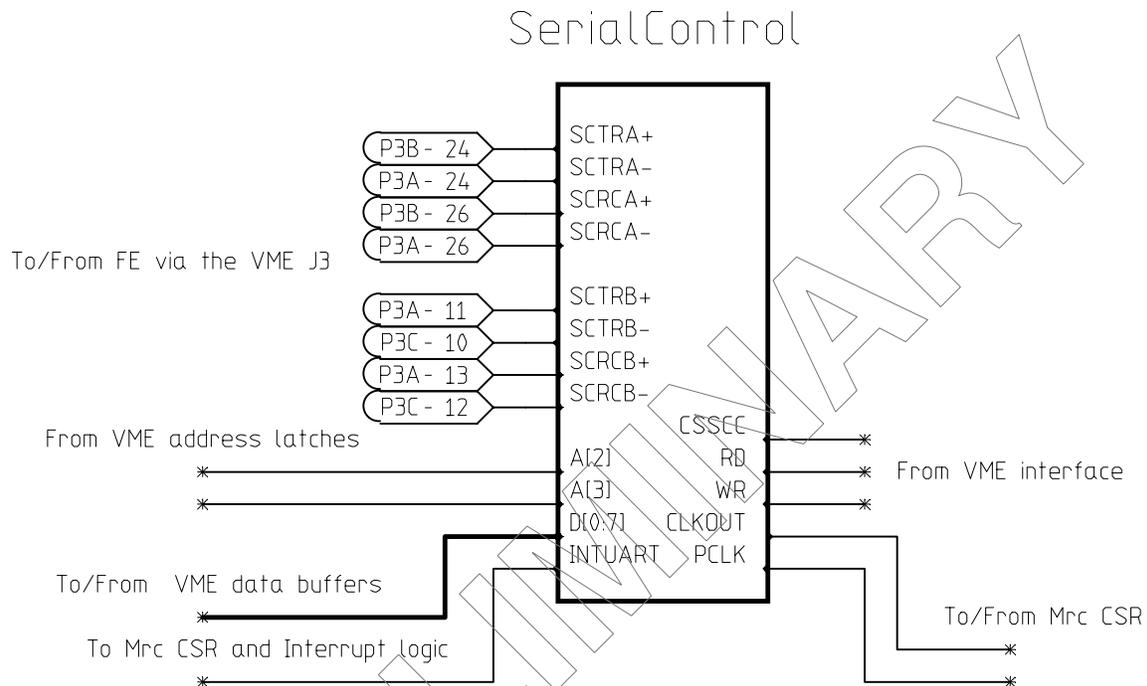
To align the incoming bit stream to the intended byte boundaries, the bit counter in Clock Sync block must be initialized. The Framing logic in CY7B933 Receiver checks the incoming bit stream for the unique pattern that defines the byte boundaries. The Framing logic in the Receiver is controlled by the Re-frame Enable (RF) input signal.

When RF is held high, the CY7B933 looks for the symbol defined as “Special Character Comma” (K28.5) or SYNC symbol. Once K28.5 is found, the free running bit counter in the Clock Sync block is synchronously reset to its initial state, thus “framing” the data to the correct byte boundaries. The bit stream is deserialized, decoded, and checked for transmission errors.

When RF held low, the re-framing logic is disabled. The incoming data stream is then continuously deserialized and decoded using byte boundaries set by the internal byte counter. The recovered byte is presented in parallel form at a byte rate (16 MHz). Bit errors in the data stream will not cause alias SYNC characters to re-frame the data erroneously.

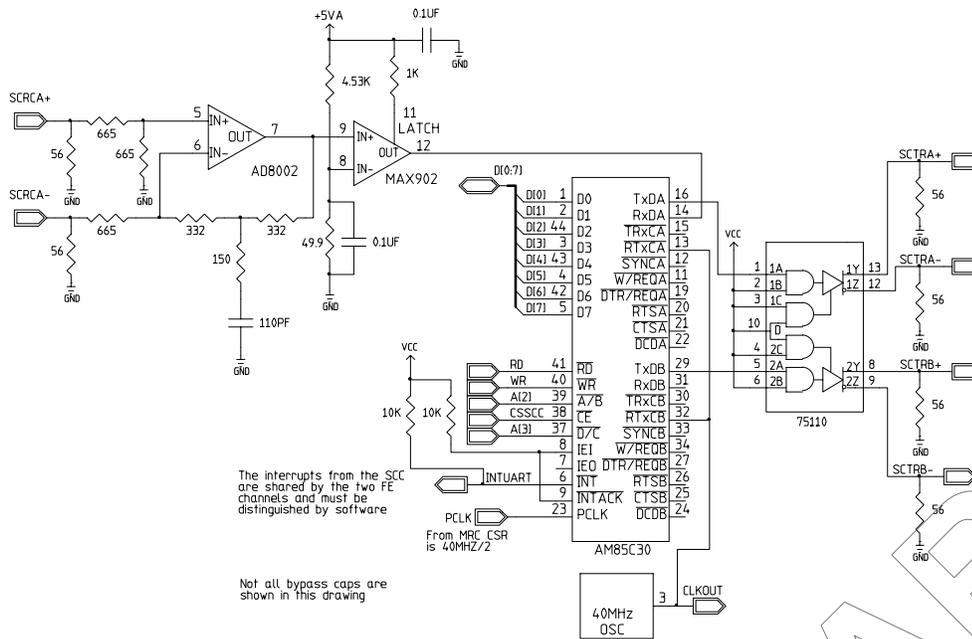
SERIAL COMMUNICATION CONTROLLER (SCC)

The Dual-channel SCC is implemented with an AM85C30 and is intended for direct communications between the VME Processor in muon crates and the DSPs in the FE. This connection is a secondary path for exchanging data between FE and MRC in testing and diagnostic operation modes. During normal operation, the 1553 data link will be used to communicate with the FE without going through the MRC. The following functional block shows the SCC section of the MRC.



The logic within the SCC Block is almost solely implemented with one AM85C30. As seen in the following schematic block there is little support logic needed. The signals to and from the FE are differential and pass through the J3 VME connector where they are split on the backplane into separate connectors for each channel. Some of the logic for the sending and receiving of these signals is shown in the simplified schematic block below. The 75110 chips are used to drive the SCTRA+, SCTRA-, SCTR B+, and SCTR B- signals to the FE. The AD8002 chips are used to receive the differential signals SCRC A+, SCRC A-, SCRC B+, and SCRC B- signals from the FE modules. These serial connections to the FE will run hundreds of feet at rates up to 2.5 Mbits per second. To achieve these rates the bi-phase encoding will be used by the AD85C30. This requires that we provide an external clock. That clock comes from a 40 MHz crystal oscillator. This oscillator also feeds a clock out to the CSR register where it is divided by two and then sent back to the serial interface where it is used as the PCLK.

The addressing and control for the serial interface comes from the VME interface.



Description of the AM85C30

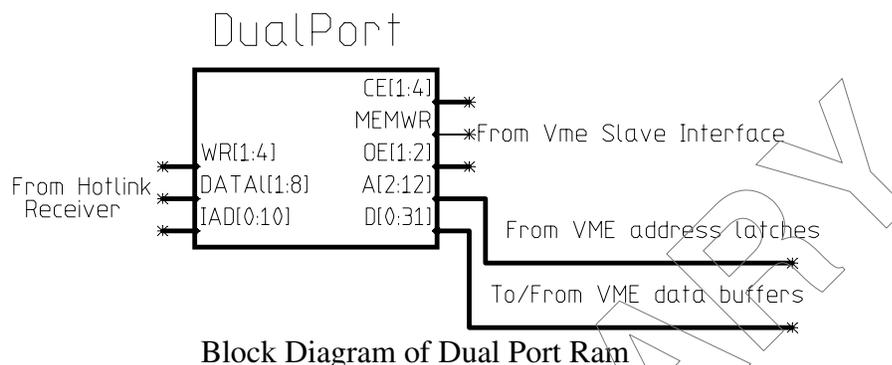
The AM85C30 is an enhanced serial communications controller designed for use with any conventional 8- and 16-bit microprocessor bus although it is only 8 bits wide. The device contains two independent, full duplex channels, two baud rate generators, a digital phase-locked loop for each channel, character counters for each channel and a 3-byte receive data FIFO for each channel.

Each channel of the AM85C30 has fifteen write registers and eight read registers. Only four data registers are directly selected by a high on D/C, to indicate data and the appropriate levels on the RD, WR, and A/B pins. All other internal registers are accessed indirectly using the address pointer in WR0. The appropriate code to select the address of the desired register is first written to the WR0 and then the selected register is accessed with a read or write. The WR0 is automatically cleared after this access so that WR0 now points to WR0 and RR0. A or B channel can be selected with the A/B input. The Transmit Data Register and Receive Data Register are accessed directly using the separate D//C pin and the A/B pin, without the need for accessing WR0.

There are six sources of interrupts in each channel of the SCC: Receive, Transmit, and External/Status, for each channel. The internal interrupt daisy chain is arranged in the order of priority within each channel with channel A having the highest priority. Both channels share the interrupt output, therefore software must pole the device to distinguish which channel is the source.

DUAL PORT RAM

The Dual Port RAM holds data for one event from the each FE. Each FE RAM has a maximum size of 8k x 32 bits and is implemented with 8k x 8 bit Dual-Port Static RAM chips. The bytes of data from CY7B933 (HOTLink) are written sequentially to the port A of memory chips under the control of an EPLD. The port B of these chips is available for writing and reading from VME. Each FE interface channel is independent and has it's own set of 4 Dual-Port RAM chips and control EPLD.



The Dual Port Ram is controlled by the VME control chip and the HOTLink control chip. When a VME cycle occurs, the VME interface will read or write the right side of the Dual Port RAM, using the address lines A[2:12], and control lines OE[1:2], CE[1:4], and MEMWR. Data will pass through the Data Buffer in the byte ordering shown in the data path drawings and byte format drawings. The HOTLink controller chip interface will control the left side of the Dual Port RAM. The HOTLink interface can only write the RAM. The HOTLink chip itself is only eight bit wide so the order of writes to the memory chips is controlled by the incrementing address counter inside the HOTLink control chip.

The current sequence is 3,4,1,2 This means the internal MRC data bus bits D[16:23] are written first. Next D[24:31] are written. Then D[0:7] are written. Last D[8:15] are written.

This results in the correct ordering of bytes for 16 bit VME reads. The first word from the FE being read out on the even address first byte zero and the second word from the FE being read on the second byte of this first even 16 bit word. The next address read would be odd, that is A1 = '1'. This will read the third word written from the FE in the zero byte and the fourth word will be in the second byte.

Dual Port data format (16 bit LOW A1='0')

VME	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
RAM	D23	D22	D21	D20	D19	D18	D17	D16	D31	D30	D29	D28	D27	D26	D25	D24

First word (byte 3) from FE

Second word (byte 4) from FE

Dual Port data format (16 bit HIGH A1='1')

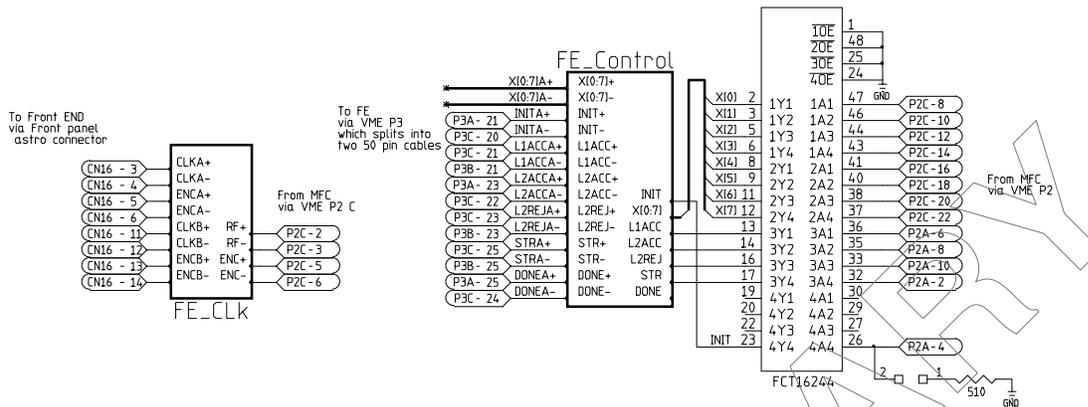
VME	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
RAM	D07	D06	D05	D04	D03	D02	D01	D00	D15	D14	D13	D12	D11	D10	D09	D08

Third word (byte 1) from FE

Fourth word (byte 2) from FE

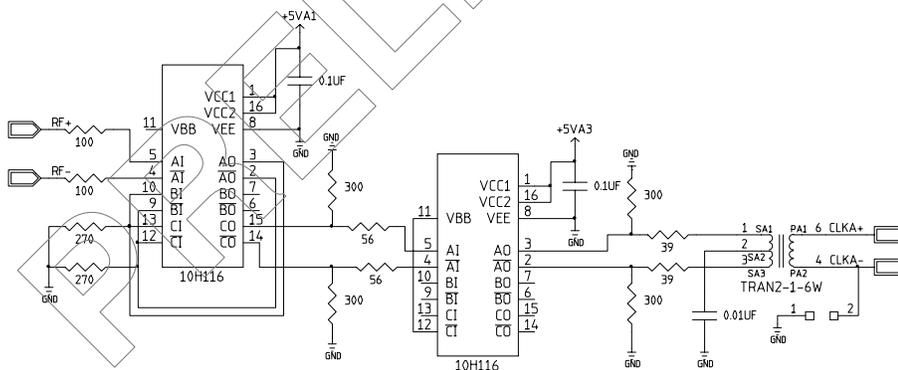
COMMUNICATIONS BETWEEN MRC AND MUON FANOUT CARD

There will be one Muon Fan-out Card and 11 to 13 MRCs in each muon crate. Each MRC receives 15 signals from and transmits five signals to the fan-out card (see Table I).



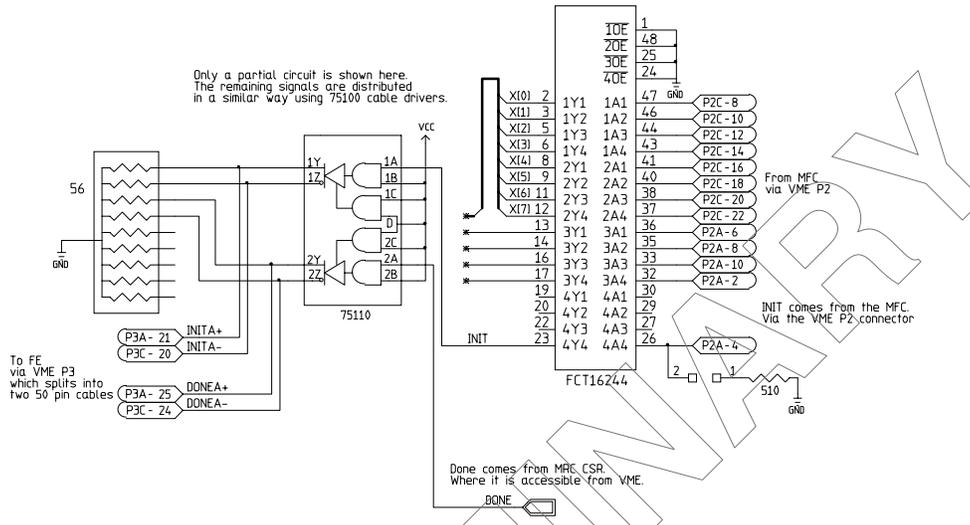
FAST PECL SIGNALS FROM FANOUT

Two fast signals from fan-out card, RF and ENC are transmitted to MRCs using differential PECL lines. PECL differential transmitters are used in the fan-out card and MC10H116 differential line receivers/transmitters are used in MRCs for these signals. The center tap of the transformer is bypassed to ground with a .01μF capacitor.



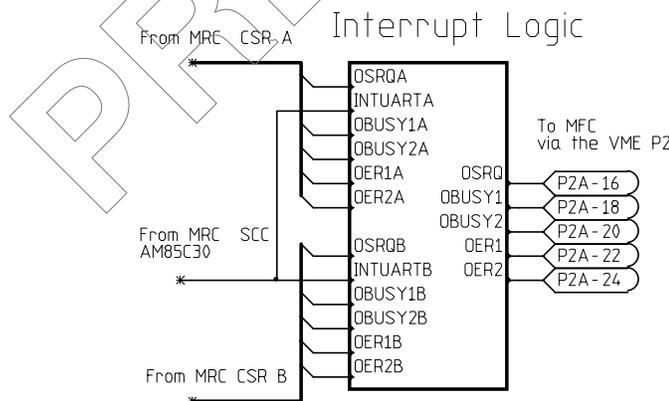
TTL SIGNALS FROM FANOUT

The other signals from fan-out to MRCs (INIT, L1ACC, STR, L2ACC, L2REJ and Xing<0-7>) are transmitted in TTL levels. 74FCT16244 16 bit latches are used as receivers and 75110 cable drivers are transmitters for these signals. The figure below shows a subset of the logic. Signals are received from J2 and then transmitted differentially to the J3 connector with 56 ohm pull downs to ground. The signal DONE comes from the CSR register.

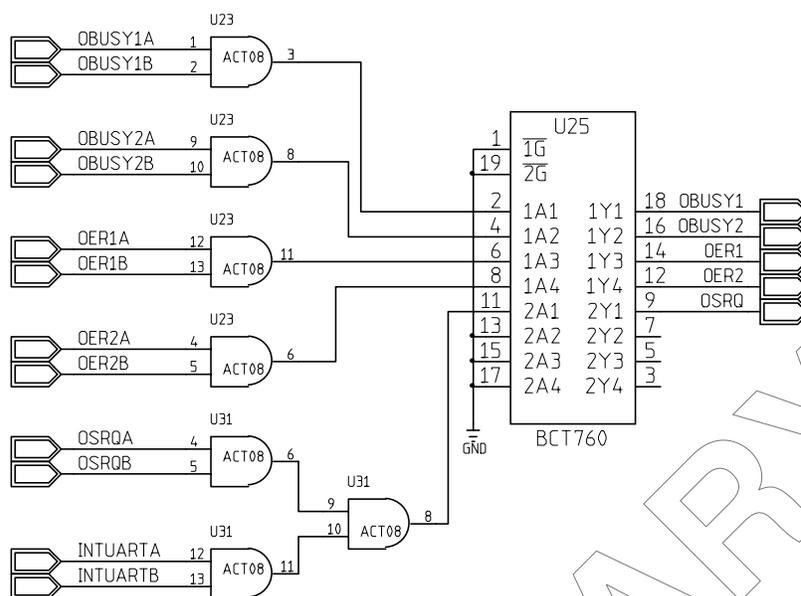


SIGNALS TO FANOUT

Each MRC can transmit five signals to Fan-out Card: BUSY1, BUSY2, ERROR1, ERROR2 and SRQ. Each output signal from the MRC notifies the fan-out card about particular MRC internal condition (interrupts from UART s, BEG_DATA and END_DATA HOTLink Control Logic signals) and can cause an interrupt of fan-out Interrupt Controller.



All output signals driven with 74BCT760 buffers on the MRCs are open collector outputs are wire-ORed on the backplane with the same signals of other MRCs in the crate.



Schematic of MRC Interrupt logic

Table I. Interconnections in VME crate.

Number	Signal	Source	Destination	Type	Transmitter	Receiver
1	RF 53 MHz	MFC	MRCs	PECL	SY100ELT22	MC10H116
2	ENC	MFC	MRCs	PECL	SY100ELT22	MC10H116
3	INIT	MFC	MRCs	TTL	SN75121	75110
4	L1 ACC	MFC	MRCs	TTL	SN75121	75110
5	Done	MFC	MRCs	TTL	SN75121	75110
6	L2 ACC	MFC	MRCs	TTL	SN75121	75110
7	L2 REJ	MFC	MRCs	TTL	SN75121	75110
8-15	Crossing #	MFC	MRCs	TTL	SN75121	75110
16	ERROR1	MRCs	MFC	TTL OC	74BCT760 (OC)	FCT16244
17	ERROR 2	MRCs	MFC	TTL OC	74BCT760 (OC)	FCT16244
18	BUSY 1	MRCs	MFC	TTL OC	74BCT760 (OC)	FCT16244
19	BUSY 2	MRCs	MFC	TTL OC	74BCT760 (OC)	FCT16244
20	SRQ	MRCs	MFC	TTL OC	74BCT760 (OC)	FCT16244
21	STR	MFC	MRCs	TTL	SN75121	75110

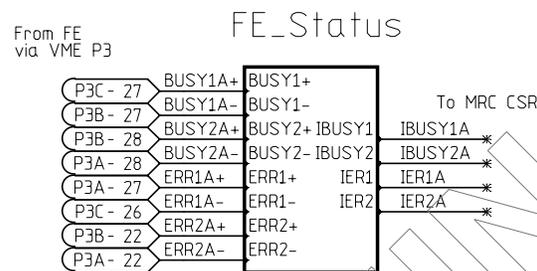
COMMUNICATION BETWEEN MRC AND FRONT END BOARDS

There are 21 communication signals between one section of the MRC and each of two Front End Sections (see **Table II** and **Table III**).

16 of these signals (RF, ENC, INIT, L1ACC, L2ACC, L2REJ, DONE and UART transmit) are outputs for MRC and inputs for FE; five signals (L3DATA, ERROR1, BUSY1, BUSY2 and UART receive) are inputs for MRC and outputs for FE boards.

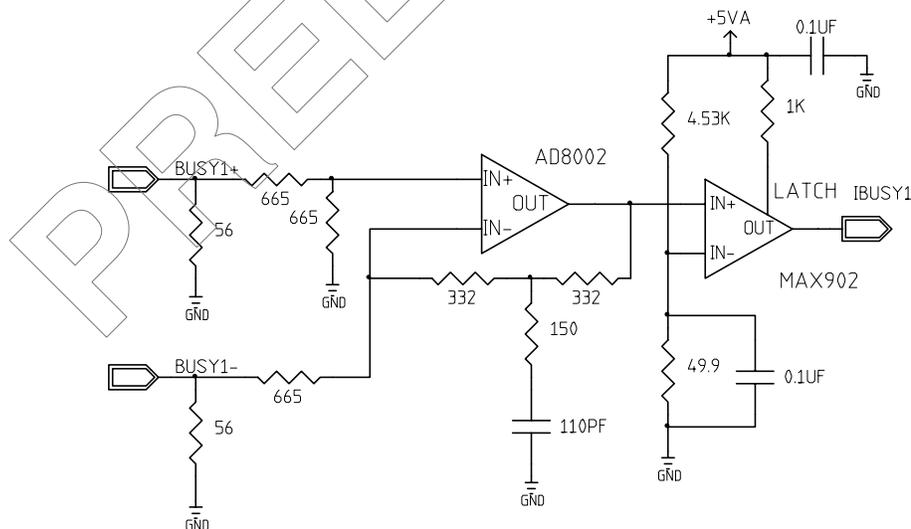
FAST SIGNALS TO FE FROM MRC

Two fast signals (RF or 53MHz, ENC or Encoded GAP/Sync) are transmitted via AMP and ASTRO ribbon coaxial cables. These signals are transmitted by MC10H116 drivers and are transformer coupled to convert differential outputs to single ended signal.



FE Status Receiver Functional Block.

Receivers for ERROR1, BUSY1, BUSY2 and UARTREC signals are based on AD8002 Current Feedback Amplifier and MAX902 Voltage Comparator.



Example FE Status Receiver Circuit.

SIGNALS TO MRC FROM FE

The L3DATA is transformer coupled on the MRC to a CLC014 differential receiver. The CLC014 drives the HOTLink Receiver CY7B933. L3DATA arrives at the MRC on AMP ribbon coaxial cable.

All other signals (INIT, L1ACC, STRB, L2ACC, L2REJ and Xing<0-7>) are transmitted to FE using 75110A High Speed Current Drivers.

Table II. Interconnections between FE and MRC (Twisted pairs)

Number	Signal	Source	Destination	Type	Transmitter	Receiver
1	INIT	MRC	FE	tw. Pair	75110A	AD8002
2	L1 ACC	MRC	FE	tw. Pair	75110A	AD8002
3	L2 ACC	MRC	FE	tw. Pair	75110A	AD8002
4	L2 REJ	MRC	FE	tw. Pair	75110A	AD8002
5-12	Crossing #	MRC	FE	tw. Pair	75110A	AD8002
13	DONE	MRC	FE	tw. Pair	75110A	AD8002
14	UART Tx	MRC	FE	tw. Pair	75110A	AD8002
15	UART Rx	FE	MRC	tw. Pair	75110A	AD8002
16	ERROR 1	FE	MRC	tw. Pair	75110A	AD8002
17	ERROR 2	FE	MRC	tw. Pair	75110A	AD8002
18	BUSY 1	FE	MRC	tw. Pair	75110A	AD8002
19	BUSY 2	FE	MRC	tw. Pair	75110A	AD8002
20	STRB	MRC	FE	tw. pair	75110A	AD8002

Table III. Interconnections between FE and MRC (AMP and ASTRO ribbon coaxial cables)

Number	Signal	Source	Destination	Type	Transmitter	Receiver
1	RF 53 Mhz	MRC	FE	coaxial	CLC006	CLC014
2	ENC	MRC	FE	coaxial	CLC006	CLC014
3	L3 DATA	FE	MRC	coaxial	CLC006	CLC014
4	L2 TRIG *)	FE	L2	coaxial	CLC006	CLC014

Note: L2 TRIG signal is not connected to the MRC

The high-speed connections to the FE are made on micro-coax. The MRC sends and receives signals from to FE crates. The connector on the MRC has signals for two units and must be split into two cables to feed two front-ends. The pin-outs for the connectors are shown below.

AMP 103167-5 16 PIN HEADER CONNECTOR MOUNTED ON MRC BOARD

Pin	Signal
1	L3DATAA+
2	L3DATAA-
3	RFA+
4	RFA-
5	ENCA+
6	ENCA-
7	NC
8	NC
9	L3DATAB+
10	L3DATAB-
11	RFB+
12	RFB-
13	ENCB+
14	ENCB-
15	NC
16	NC

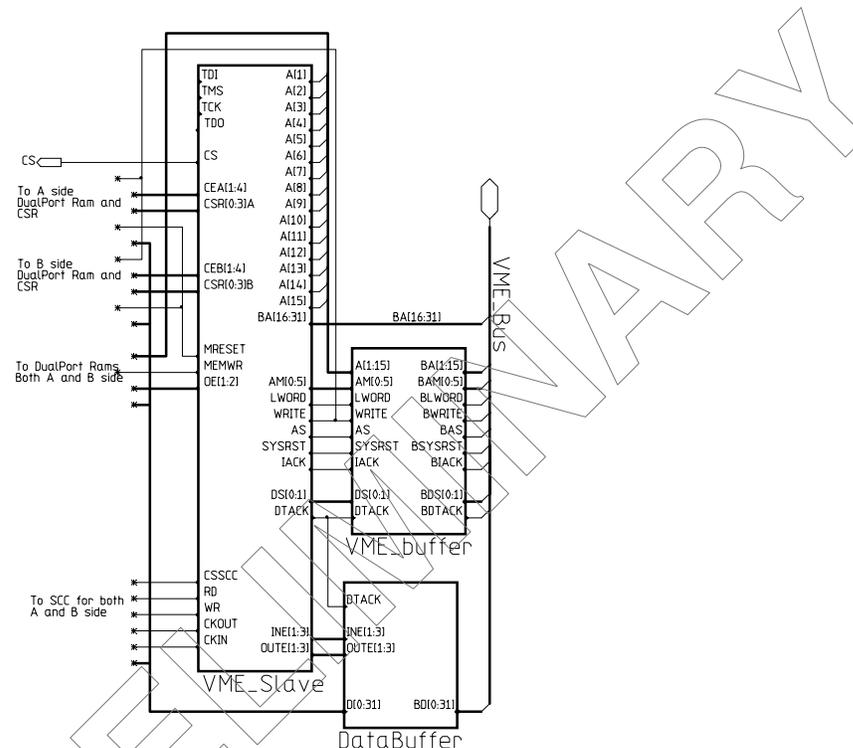
AMP 103167-1 8 PIN HEADER CONNECTOR MOUNTED ON FE BOARD

Pin	Signal
1	L3DATA+
2	L3DATA-
3	RF+
4	RF-
5	ENC+
6	ENC-
7	L2DATA+
8	L2DATA-

VME INTERFACE

The MRC has a 32-bit VME Slave Interface consisting of:

- VME BUFFER for VME address and control signals;
- VME BA[16:31] address decoder in VME SLAVE ;
- VME 32-bit Data Bus Receivers/Transmitters;
- VME SLAVE command decoder.



Block Diagram of VME INTERFACE.

A memory map of all RAM buffers and I/O ports in MRC is given in Table IV. It is possible to select Base address via DIP switches on MRC board (A16-A23 address bits, address lines A24-A31 are not used). A step of selecting Base address is 64 Kbyte. Most of the decoding is done in the VME SLAVE logic. The Dual Port RAMs use A[2:12] and the serial controller has A2,A3 as inputs. DTACK is returned by the VME SLAVE logic. There is no difference between the timing of any DS to DTACK cycle.

74FCT16244 chips are used as input buffers and 74FCT16500 as Data Bus Receivers/Transmitters. The VME address and control is buffered but not latched. It always tracks the VME bus. The only latching is of the decoded address inside the VME SLAVE. The VME data bus receiver does not latch the data but the transmitter latches output data with DTACK. The VME SLAVE will respond to BSYSRESET by performing a MRESET on the MRC. The MRC monitors IACK but never issues any interrupt to the VME. The MRC interrupt logic is simple wire-OR logic on the J2 connector and is

received by the MFC not the VME crate master. The MRC can only drive the standard VME data lines and the DTACK signal. All other standard VME signals are inputs. The VME controller chip also has a CLKIN (40MHZ) from the serial logic section and CKOUT (20MHZ.) to the serial logic.

The VME address and command decoder for both sections of MRC is based on single ALTERA EMP7128s chip.

Table IV. MRC Memory Map.

All addresses start from Base Address ($N * 64K$, $N=0...255$). In the following table the base address is assumed to be 220000.

Address	Length (bytes)	Assigned
220000...221FFF	8K	Dual-Port RAM Section A
224000	0	Reset SCC AM85C30
224010	4	CSR Section A
228000...229FFF	8K	Dual-Port RAM Section B
22C000	1	SCC Channel B; access to Control registers
22C004	1	SCC Channel A; access to Control registers
22C008	1	SCC Channel B; direct access to Data registers
22C00C	1	SCC Channel A; direct access to Data registers
22C010	4	CSR Section B

DATA BUFFER PATH

The Data Buffer path is determined by the control lines from the VME SLAVE interface. These lines INE[1:3], and OUTE[1:3] control the flow of data in and out of the MRC.

CSR and Dual Port data format (16 bit LOW)

vme	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
csr	D23	D22	D21	D20	D19	D18	D17	D16	D31	D30	D29	D28	D27	D26	D25	D24

CSR and Dual Port data format (16 bit HIGH)

vme	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
csr	D07	D06	D05	D04	D03	D02	D01	D00	D15	D14	D13	D12	D11	D10	D09	D08

Dual Port data format (32 bit even address)

vme	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
Ram	D07	D06	D05	D04	D03	D02	D01	D00	D15	D14	D13	D12	D11	D10	D09	D08

vme	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
Ram	D23	D22	D21	D20	D19	D18	D17	D16	D31	D30	D29	D28	D27	D26	D25	D24

AMD Am85C30 Serial Communication Controller data format

vme	D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
scc	D07	D06	D05	D04	D03	D02	D01	D00	X	X	X	X	X	X	X	X

32 BIT CONTROL/STATUS REGISTER

There is one 32-bit Control/Status Register (CSR) in each MRC section (Table V). It consists of:

- BUSY1, BUSY2, and ERROR1 bits indicating conditions of corresponding signals from FE, and ERROR2 bit (as a logical OR of FE signal ERROR2 and error sources in MRC itself (OVF, RVS and TOUT signals from HOTLink receivers with corresponding mask bits))
- Mask BUSY1_M, BUSY2_M, ERROR1_M, ERROR2_M and SRQ_M bits for corresponding signals. If they are set to zero the corresponding signals are disabled.
- Test bits ERROR1_T, ERROR2_T, SRQ_T, and DONE_T bits for setting corresponding signals by software.
- RESET bit for resetting ERROR bits (TOUT, RVS and OVF) in CSR itself and in HOTLink Control Logic
- REF/REFD bit forces a CY7B933 Re-frame Mode and is used to read back Re-frame status.
- DONE bit reads DONE signal being sent to FE and DONE_R resets the DONE bit.
- CONN bit indicating (when HIGH) that connection with HOTLink Transmitter in FE board is valid (LOW means that connection failures)
- SRQ bit reads SRQ being sent to MFC
- SRQ_R bit for resetting SRQ flip-flop
- DSTREAM bit indicating (when HIGH) that Data Transfer from FE board is in progress
- DSTR_EN is used to enable and disable the data steam (dual port memory writes).
- CSR_A_B indicates that this is A channel or B channel of the MRC.
- BIST bit for setting HOTLink Built-In Self-Test (BIST) and BISOK bit for indicating BIST status
- TOUT_DSTR, TOUT_BIST, TOUT_REFR, RVS_DSTR, RVS_BIST, RVS_GLB, and OVF_DSTR bits indicating the error status of different (TOUT, RVS, OVF) sources during different modes of Data Transfer (DSTR), Re-frame (RFR) and Built-In Self-Test (BIST)
- INTSCC bit indicating the Interrupt Request from SCC (Serial Communication Controller)

CSR for each section is based on separate ALTERA EPM128S chip (see below).

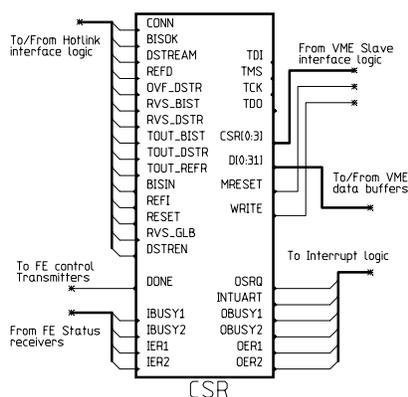


Table V. Muon Readout card Status/Control register.

VME bit#	Read/Write	WRITE		READ	
		NAME	REMARKS	NAME	REMARKS
0	R	-	-	TOUT_DSTR	Time-out during Data Transfer
1	R	-	-	RVS_DSTR	RVS during Data Transfer
2	R	-	-	OVF_DSTR	OVF during Data Transfer
3	R	-	-	RVS_BIST	RVS during Self-Test
4	R	-	-	TOUT_BIST	Time-out during Self-Test
5	R	-	-	TOUT_REFR	Time-out during Re-frame
6	R	-	-	RVS_GLB	RVS outside of data transfer
7	R	-	-	INTSCC	Interrupt from SCC
8	R	-	-	CONN	MRC-FE Connection
9	R	-	-	DSTREAM	CY7B933 Data Transfer Status ("1" when DSTREAM exists)
10	R			DONE	
11	R			SRQ	SRQ Status
12	R	-	-	BUSY1	FE signal
13	R	-	-	BUSY2	FE signal
14	R	-	-	ERROR1	FE signal + Set Register
15	R	-	-	ERROR2	Error2 Sources OR * Mask Register
16	R/W	ERROR1_T	Error1 test bit	ERROR1_T	Error1 test bit
17	R/W	ERROR2_T	Error2 test bit	ERROR2_T	Error2 test bit
18	R/W	SRQ_T	SRQ test bit	SRQ_T	SRQ test bit
19	R/W	DONE_T	DONE test bit	DONE_T	DONE test bit
20	R/W	REF	Reframe HOTLink	REFD	HOTLink has re-framed
21	R/W	BIST	Set BIST Mode	BISOK	BIST Status from CY7B933 Control Logic
22	W	DONE_R	DONE reset bit (write 1)	-	-
23	W	SRQ_R	SRQ reset bit (write 1)	-	-
24	R/W	DSTR_EN	HOTLink Enable		HOTLink Enable
25	R	-	-	CSR_A_B	CSRA=0 CSRB=1
26	W	RESET	Reset TOUT, RVS, OVF Bits and CY7B933 Control Logic	-	-
27	R/W	SRQ_M	SRQ Mask bit	SRQ_M	SRQ Mask bit
28	R/W	BUSY1_M	Busy1 Mask bit	BUSY1_M	Busy1 Mask bit
29	R/W	BUSY2_M	Busy2 Mask bit	BUSY2_M	Busy2 Mask bit
30	R/W	ERROR1_M	Error1 Mask bit	ERROR1_M	Error1 Mask bit
31	R/W	ERROR2_M	Error2 Mask bit	ERROR2_M	Error2 Mask bit

MECHANICAL PARAMETERS AND FRONT PANEL

The MRC is realized as one-slot VME 9U module on PCB 14.4'' x 11'' size. There are 16 LED on the front panel (seven for each channel) indicating the following conditions:

- Lost connection between FE board and MRC (DISCONN, red);
- Data Transfer from FE board is in progress (DSTREAM, green);
- ERROR1 is present (ERROR1, red);
- ERROR2 is present (ERROR2, red);
- BUSY1 is present (BUSY1, green);
- BUSY2 is present (BUSY2, green);
- SRQ is present (SRQ, green).
- +5 and -5,2 power supply are on. (yellow)

There is also 16-pin AMP connector for coaxial cables on the front panel.

PRELIMINARY

D0 Muon Upgrade Backplane

J7 and J8 Connectors Pin Assignment

Pin	Signal	Pin	Signal
1	Xing0+	2	Xing0-
3	Xing1+	4	Xing1-
5	Xing2+	6	Xing2-
7	Xing3+	8	Xing3-
9	Xing4+	10	Xing4-
11	Xing5+	12	Xing5-
13	Xing6+	14	Xing6-
15	Xing7+	16	Xing7-
17	INIT+	18	INIT-
19	L1ACC+	20	L1ACC-
21	ERR2+	22	ERR2-
23	L2ACC+	24	L2ACC-
25	L2REJ+	26	L2REJ-
27	SCCTR+	28	SCCTR-
29	DONE+	30	DONE-
31	STRB+	32	STRB-
33	SCCRC+	34	SCCRC-
35	ERR1+	36	ERR1-
37	BUSY1+	38	BUSY1-
39	BUSY2+	40	BUSY2-
41	GND	42	GND
43	GND	44	GND
45	GND	46	GND
47	GND	48	GND
49	GND	50	GND

Notes

1. J7 is referred to Section A of MRC; J8 is referred to Section B of MRC.
2. 10 pins (41-50) of J8 are connected to GND at the backplane; 10 pins (41-50) of J7 are connected to GND within VME module.
3. TxDAT or SCCTR denotes MRC's UART transmitter output; RxDAT or SCCRC denotes MRC's UART receiver input.

D0 MUON BACKPLANE J1 CONNECTOR

Pin	A	B	C
1	D00	BBSY/	D08
2	D01	BCLR/	D09
3	D02	ACFAIL/	D10
4	D03	BG0IN/	D11
5	D04	BG0OUT/	D12
6	D05	BG1IN/	D13
7	D06	BG1OUT/	D14
8	D07	BG2IN/	D15
9	GND	BG2OUT/	GND
10	SYSCLK	BG3IN/	SYSFAIL/
11	GND	BG3OUT/	BERR/
12	DS1/	BR0/	SYSRESET/
13	DS0/	BR1/	LWORD/
14	WRITE/	BR2/	AM5
15	GND	BR3/	A23
16	DTACK/	AM0	A22
17	GND	AM1	A21
18	AS/	AM2	A20
19	GND	AM3	A19
20	IACK/	GND	A18
21	IACKIN/	SERCLK	A17
22	IACKOUT/	SERDAT	A16
23	AM4	GND	A15
24	A07	IRQ7/	A14
25	A06	IRQ6/	A13
26	A05	IRQ5/	A12
27	A04	IRQ4/	A11
28	A03	IRQ3/	A10
29	A02	IRQ2/	A09
30	A01	IRQ1/	A08
31	-12V	+5VSTDBY	+12V
32	+5V	+5V	+5V

D0 MUON BACKPLANE J2 CONNECTOR

Pin	A	B	C
1	GND	+5V	GND
2	STR	GND	RF+
3	GND	RESERVED	RF-
4	INIT	A24	GND
5	GND	A25	ENC+
6	L1ACC	A26	ENC-
7	GND	A27	GND
8	L2ACC	A28	X0
9	GND	A29	GND
10	L2REJ	A30	X1
11	GND	A31	GND
12	RESERVED	GND	X2
13	GND	+5V	GND
14	RESERVED	D16	X3
15	GND	D17	GND
16	/SRQ	D18	X4
17	GND	D19	GND
18	/BUSY1	D20	X5
19	GND	D21	GND
20	/BUSY2	D22	X6
21	GND	D23	GND
22	/ERR1	GND	X7
23	GND	D24	GND
24	/ERR2	D25	RESERVED
25	GND	D26	GND
26		D27	
27		D28	
28		D29	
29		D30	
30		D31	
31		GND	
32		+5V	

Note: ENC and RF are differential ECL level signals

D0 MUON BACKPLANE J3 CONNECTOR

Pin	A	B	C
1	GND	GND	GND
2	X0B- (J8:2)	X0B+ (J8:1)	X1B- (J8:4)
3	X1B+ (J8:3)	X2B- (J8:6)	X2B+ (J8:5)
4	X3B- (J8:8)	X3B+ (J8:7)	X4B- (J8:10)
5	X4B+ (J8:9)	X5B- (J8:12)	X5B+ (J8:11)
6	X6B- (J8:14)	X6B+ (J8:13)	X7B- (J8:16)
7	X7B+ (J8:15)	INITB- (J8:18)	INITB+ (J8:17)
8	L1ACCB- (J8:20)	L1ACCB+ (J8:19)	ERR2B- (J8:22)
9	ERR2B+ (J8:21)	L2ACCB- (J8:24)	L2ACCB+ (J8:23)
10	L2REJB- (J8:26)	L2REJB+ (J8:25)	SCCTRB- (J8:28)
11	SCCTRB+ (J8:27)	DONEB- (J8:30)	DONEB+ (J8:29)
12	STRB- (J8:32)	STRB+ (J8:31)	SCCRCB- (J8:34)
13	SCCRCB+ (J8:33)	ERR1B- (J8:36)	ERR1B+ (J8:35)
14	BUSY1B- (J8:38)	BUSY1B+ (J8:37)	BUSY2B- (J8:40)
15	BUSY2B+ (J8:39)	X0A- (J7:2)	X0A+ (J7:1)
16	X1A- (J7:4)	X1A+ (J7:3)	X2A- (J7:6)
17	X2A+ (J7:5)	X3A- (J7:8)	X3A+ (J7:7)
18	X4A- (J7:10)	X4A+ (J7:9)	X5A- (J7:12)
19	X5A+ (J7:11)	X6A- (J7:14)	X6A+ (J7:13)
20	X7A- (J7:16)	X7A+ (J7:15)	INITA- (J7:18)
21	INITA+ (J7:17)	L1ACCA- (J7:20)	L1ACCA+ (J7:19)
22	ERR2A- (J7:22)	ERR2A+ (J7:21)	L2ACCA- (J7:24)
23	L2ACCA+ (J7:23)	L2REJA- (J7:26)	L2REJA+ (J7:25)
24	SCCTRA- (J7:28)	SCCTRA+ (J7:27)	DONEA- (J7:30)
25	DONEA+ (J7:29)	STRA- (J7:32)	STRA+ (J7:31)
26	SCCRCA- (J7:34)	SCCRCA+ (J7:33)	ERR1A- (J7:36)
27	ERR1A+ (J7:35)	BUSY1A- (J7:38)	BUSY1A+ (J7:37)
28	BUSY2A- (J7:40)	BUSY2A+ (J7:39)	GND
29	GND	GND	GND
30	GND	GND	GND
31	GND	GND	GND
32	-5V	-5 V	-5 V