

## Fermilab Engineering Note

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**Subject:** Front-End Board User's Guide

# Front-End Board User's Guide

## 1. Introduction

The Front-End Board (FEB) is designed to process wire and pad signals generated by D0 muon proportional drift tubes (PDT). Wire signals are used to provide PDT Level 1 trigger information and for drift time and delta time measurements. Pad signals are used for accurate longitudinal coordinate measurements. The wire is a negative current source in a range of 0.5..50  $\mu\text{A}$ . The pad is a positive current source in a range of 0.2..20  $\mu\text{A}$ . Wire signals travel within the aluminum body of the PDT, which, with the wire, constitutes a wave-guide of about 330  $\Omega$  impedance. Two neighboring cells in one layer of the PDT have a lumped 20 ns delay jumper connecting the two far ends of the wires. A signal originating at the near end of one tube will take about 60 ns to propagate to the near end of the other. Induced charge from the wire signal is collected on two pad electrodes with about 1200 pF capacitance each. Each PDT cell has a service board to bring high voltage to the wire and pads, and to pick up the signals. Single ended wire signals are converted to differential by a wide-band coupling transformer. Each cell has two pad electrodes, A and B, connected to the FEB separately. According to the current naming convention the pad electrode connected to a pin closest to the wire pin is called pad B.

## 2. FEB block-diagram

A block-diagram of the Front-End Board is shown in Figure 1. Each board includes 24 Wire Amplifier/Discriminators and 48 Pad Amplifiers and Integrators. Depending on the number of PDT cells, 3 or 4 FEBs and one Control Board (CB) can be mounted on each PDT. All the wire discriminators on one FEB have a common threshold voltage controlled by the analog voltage provided by the CB. There are also two test pulsers connected via a resistor network to the wire and pad amplifier inputs. The test pulsers generate exponential signals approximating the wire and pad signals. The CB also controls the amplitude and synchronization of these signals. The FEB has a channel enable register, which allows the enabling or disabling of any wire discriminator on the board. Combined with the test pulsers, this feature allows for remote testing of most of the functions of the FEB. The FEB has six TDC ASICs (Toshiba TMCTEG3) and 24 10-bit ADCs (Texas Instruments TLC876) continuously digitizing the arrival times and induced pad charges respectively. The digitized data is stored in digital pipelines for about 4  $\mu\text{s}$ , which is the Level 1 trigger decision time. If a trigger accept is generated, the appropriate portion of the time history from the pipelines is transferred to the Level 1 FIFOs. From there information is read out under control of the CB. The FEB also receives its timing signals via the CB interface.

## 3. Wire signal processing

Wire signal is discriminated by the Wire Amplifier and Discriminator (WAD). A two-stage amplifier (UPC1663G and HFA1135) provides a gain of 100 mV/ $\mu\text{A}$  at the discriminator input. The amplifier has a differential input that rejects common mode noise. The transformer coupling also helps to reject low frequency noise. The amplifier has a rise time of 12 ns and an input noise level of  $\sim 75$  nA (RMS) for the bandwidth of interest. This allows the FEB to operate with a

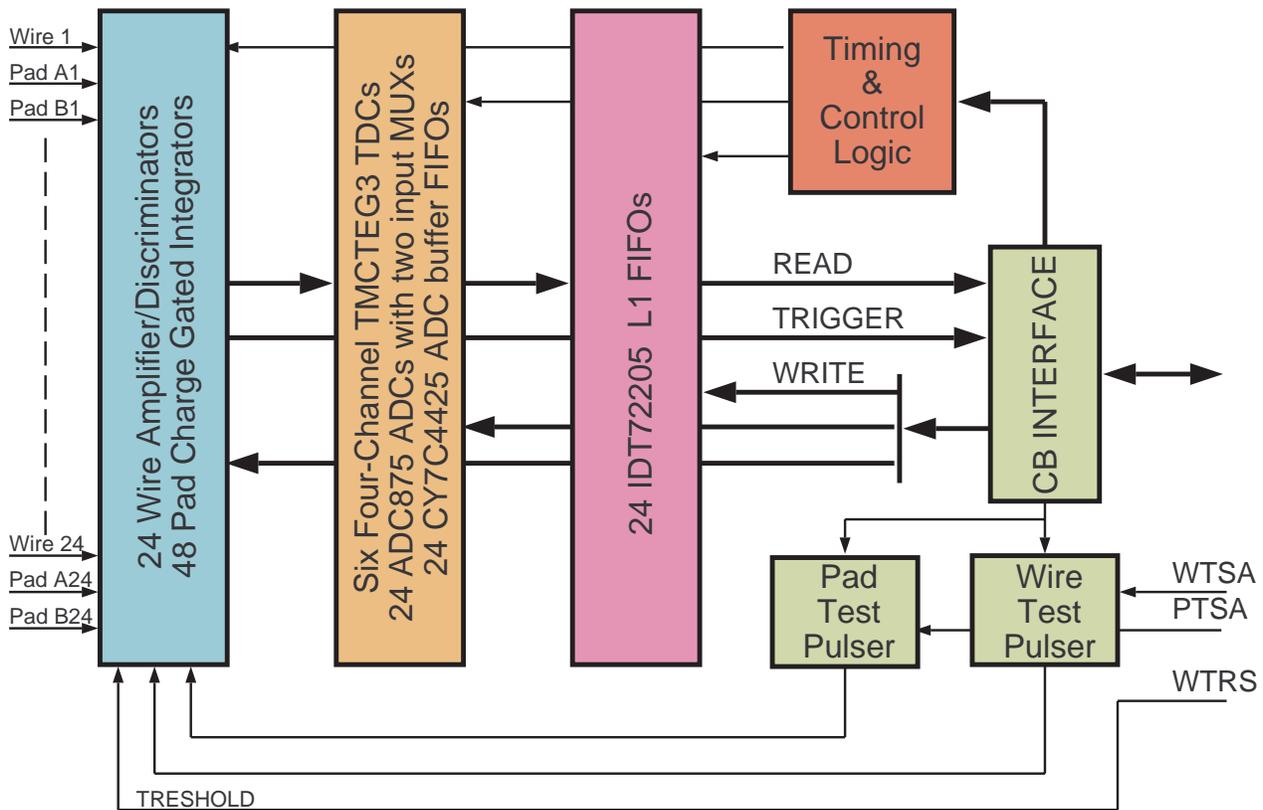


Figure 1. Block-diagram of 24-channel muon PDT Front-End Board.

discriminator threshold as low as  $0.5 \mu\text{A}$ . An HFA1135 has an internal limiting feature, which is used to reduce the recovery time of the amplifier when overdriven by high level input signals. These limits are set to  $+3\text{V}$  and to  $-1\text{V}$  respectively. A discriminator based on the Maxim MAX913 comparator with capacitive feedback (to set the minimum output pulse width at  $22 \text{ ns}$ ) is used. A  $19 \text{ ns}$  minimum width is required by the FEB logic to latch in the discriminator signal by a  $53 \text{ MHz}$  clock. The minimum double pulse resolution of the discriminator is about  $55 \text{ ns}$ . The comparator has complementary outputs to match the differential inputs of the TMC chip. This arrangement has the additional benefit of less feedback to the amplifier input than single ended outputs.

A wire signal travels both directions from the point where particle crosses the tube. The signal arrives first at the near end of the tube in which the track occurred. It also crosses the jumper and travels the full length of the adjacent tube and appears at its near end. There is always a minimum  $20 \text{ ns}$  delay between arrival of the two signals at near ends. To determine first arrival, a simple two D-type flip-flop separator circuit, clocked by the wire signals with cross-connected Q-bar outputs to D inputs is used. Both flip-flops are reset  $60 \text{ ns}$  after the output signal is generated. This circuit will produce valid result only with one track crossing two paired PDT cells. In the rare case of two particles crossing paired cells, and generating wire signals within the time resolution of the separator ( $60 \text{ ns}$ ), the latest signal will be suppressed and no trigger signal will be generated for that wire.

Time measurements are implemented using a four-channel TDC chip (TMCTEG3 developed for the SSC by KEK). The TMC chip provides five bits of interpolator data and a hit flag bit for each channel. The data is stored in an internal  $128$ -deep memory with independently programmable read and write pointers. The chip operates at a  $53.2 \text{ MHz}$  frequency, which provides a  $1.2 \text{ ns}$  bin resolution and  $4.8 \mu\text{s}$  digital delay for the Level 1 decision time. This makes possible a deadtimeless synchronous data readout. The block-diagram of the digital time measurements is shown in Figure 2

#### 4. Pad signal processing

The integrator preamplifier uses an RF bipolar input transistor (NEC NE856) and has an input impedance of about  $20\Omega$ . The average charge collected from the pads is about  $2\text{ pC}$ . Sections of a Burr-Brown OPA660 operational transconductance amplifier and buffer are used as the integrator current source and voltage buffer respectively. The integrator has a CMOS switch (74LV4066) externally connected in parallel to the integrating capacitor. The discharge time of the integrator capacitor is less than  $20\text{ ns}$ , which allows the use of a reset pulse  $\sim 50\text{ ns}$  wide. High impedance BiFET input amplifier (Analog Devices AD712) provides DC zeroing at the integrator output.

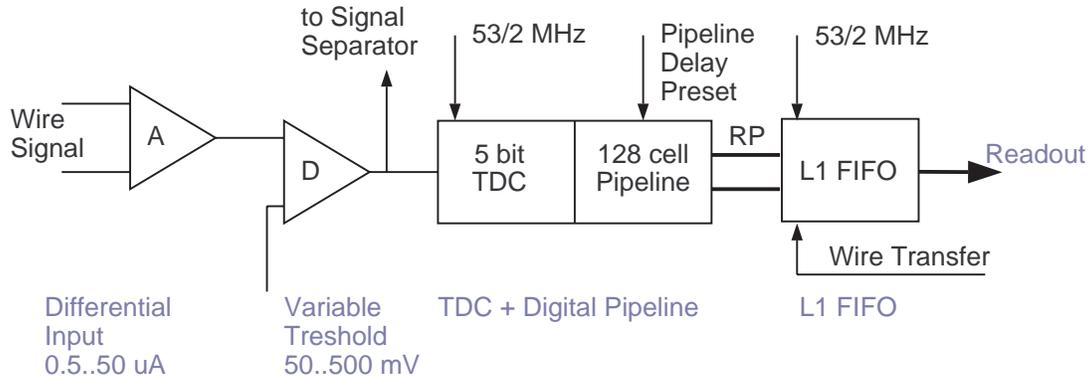


Figure 2. Wire signal processing.

Each pad channel is triggered by its corresponding separator output. This results in a sampling interval that is fixed with respect to the pad signal. The analog multiplexer runs at a  $53/8\text{ MHz}$  clock frequency synchronously with the ADC clock. The multiplexer is based on the same type of CMOS analog switch (Philips 74LV4066) used to discharge the integrator capacitor. A 64-cell pipeline follows an ADC digitizing integrator signal. The delay between the sampling point and corresponding data out of the pipelined ADC is three and a half clock cycles, which allows baseline sampling without any external delays. The ADC and memory buffer are continuously clocked at  $53/4\text{ MHz}$ . The ADC sequencer, triggered by the asynchronous separator output, generates flag bits synchronously with the ADC clock to mark the baseline and peak samples. These flag bits are used for zero suppression when data is transferred from the ADC buffer memory to the next level of buffering. After the ADC has sampled the integrator output the integrator is reset thus reducing its recovery time to  $50\text{ ns}$ . The ADC buffer memory is a FIFO with external logic that allows the difference between the read and write pointers to be programmable. Level 1 triggers are formed while the data is clocking through the buffer. The length of the buffer is adjusted so that the data emerges approximately in time with the arrival of the L1 trigger accepts. Two ADC buffer memories are multiplexed at the L1 FIFO input at  $53/2\text{ MHz}$ . The block-diagram of the pad data processing is shown in Figure 3.

#### 5. Deadtimeless readout

The principle advantage of the FEB data processing is its storage of digitized data in circular buffers pending a trigger decision, with no data loss. For the sake of simplicity, all the components of the Front-End Board and Control Board are synchronized to sub-harmonics of  $53\text{ MHz}$ . The TMC chip has its own 128 deep buffer controlled by its read and write pointers. The difference in the pointer settings allows the data to be delayed for the necessary trigger decision time. Five bits of data from the read pointer output are combined with five TMC output bits in order to extend its range to span the full drift time. According to the current specification, accelerator bunches come every  $3\frac{1}{2}$  ticks of the TMC clock and there is an odd number of bunches (1113) per turn. This makes it necessary to correct the TMC data in order to resolve the ambiguities between bunches occurring at the beginning or in the middle of a TMC clock cycle. Since all the events in the D0 DAQ are identified by the crossing and turn numbers there is no problem in applying such a correction to the data.

For ADC data an external memory buffer is used, which runs in a manner similar to the TMC internal buffer. Because of the lower bandwidth of the pad channel, a  $53/4$  MHz frequency is used for its synchronization. During multiplexing at the L1 FIFO input the ADC data is written into the FIFO at  $53/2$  MHz. Because of the long integration time, pad information is not sensitive to the bimodal jitter of the bunch crossing with respect to the ADC clock. Pad integrator signals are multiplexed at the ADC input, and hence there is a possibility of transferring only a portion of the event pad data to the L1 FIFO. Because of the specified minimum interval between two L1 accepts of  $2.6 \mu\text{s}$ , data transfers to L1 FIFOs do not generate any dead time.

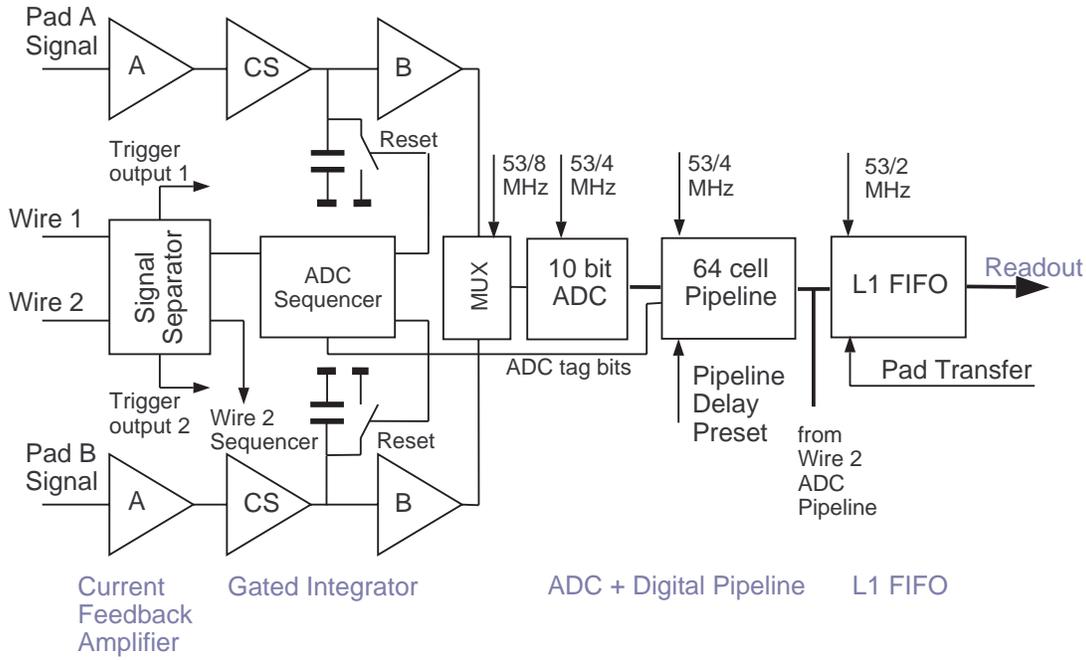


Figure 3. Pad signal processing.

Level 1 and Level 2 decisions come from the D0 trigger framework down to the front ends located in the collision hall. In order to facilitate synchronization and correctly identify the crossing at which a trigger has occurred, the trigger framework provides an eight bit crossing number to the front-end electronics. This number is compared to a local crossing counter value, which is stored in a buffer memory of the same type as those used within the TMCs and attached to the ADCs. The timing of the transfer signals that store data in the L1 FIFOs must be set to select the exact crossing caused generation of the L1 trigger. The CB controls the timing adjustments of the transfer signals, the pipeline delay setting is controlled by the FEB.

The duration of the data transfer to the Level 1 FIFOs is programmed within the CB's Level 1 logic and is approximately equal to the maximum drift time for TMC data. For the ADC data, because of the rise time of the integrator signal, analog multiplexing and one clock cycle uncertainty in the arrival time of the asynchronous pad signal, the data transfer takes about  $1.0 \mu\text{s}$  longer. A zero suppression is based on the flag bits previously appended to the data stream, only valid hits are stored in L1 FIFOs. An event boundary marker word is written to the Level 1 FIFOs at the end of each event, so several events can be stored in the memory.

## 6. Front-End Board data formats

Pad and wire information is transferred via an 18-bit data bus from the L1 FIFO memories located on the FEBs. The number of words transferred depends on the number of hits digitized for the particular event and thus varies. Each FIFO memory has to be read out for each event. The FEB readout logic transfers data words from the TMC and ADC pipelines upon receiving wire transfer and pad transfer signals from the Control Board. Valid hit data words transferred to the L1 FIFOs have bit 17 set to one. Bit 17 is set to zero in the event separator word that is added at the end of each transfer. If there





from the particular FIFO depends on the number of hits recorded. During the wire data readout, the first three data words have the Event Separator bit set to zero. These words represent six TMC readout pointers stored at the first transition of the wire transfer signal (see section 6).

The FEB generates error signal (ERR1) at the following conditions:

- Wire transfer or pad transfer signal received while INIT signal is high
- Any of the L1 FIFO Full Flags are set

Table I. FEB control bus address map.

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment
01	PTEN	WTEN	TGT5	TGT4	TGT3	TGT2	TGT1	TGT0	Trigger Gate
02	CE8	CE7	CE6	CE5	CE4	CE3	CE2	CE1	Channel ENBL
03	CE16	CE15	CE14	CE13	CE12	CE11	CE10	CE9	Channel ENBL
04	CE24	CE23	CE22	CE21	CE20	CE19	CE18	CE17	Channel ENBL
05	EF8	EF7	EF6	EF5	EF4	EF3	EF2	EF1	L1 FIFO EFs
06	EF16	EF15	EF14	EF13	EF12	EF11	EF10	EF9	L1 FIFO EFs
07	EF24	EF23	EF22	EF21	EF20	EF19	EF18	EF17	L1 FIFO EFs
08	BF8	BF7	BF6	BF5	BF4	BF3	BF2	BF1	ADC FIFO EFs
09	BF16	BF15	BF14	BF13	BF12	BF11	BF10	BF9	ADC FIFO EFs
0A	BF24	BF23	BF22	BF21	BF20	BF19	BF18	BF17	ADC FIFO EFs
0B	X	ETST	X	FCEN	PEN	WEN	PRUN	TRUN	RUN Control
0C	FF8	FF7	FF6	FF5	FF4	FF3	FF2	FF1	L1 FIFO FFs
0D	FF16	FF15	FF14	FF13	FF12	FF11	FF10	FF9	L1 FIFO FFs
0E	FF24	FF23	FF22	FF21	FF20	FF19	FF18	FF17	L1 FIFO FFs
0F	X	X	AD5	AD4	AD3	AD2	AD1	AD0	ADC Pipeline
10	Shift	MTS	NRPS	ENRP	X	TCH	TCH0	F/R*	TMC1 CRS0
11	X	RP6	RP5	RP4	RP3	RP2	RP1	RP0	TMC1 CSR1
12	X	WP6	WP5	WP4	WP3	WP2	WP1	WP0	TMC1 CSR2
13	SOUT	SIN	TD5	TD4	TD3	TD2	TD1	TD0	TMC1 CSR3
20	Shift	MTS	NRPS	ENRP	X	TCH	TCH0	F/R*	TMC2 CRS0
21	X	RP6	RP5	RP4	RP3	RP2	RP1	RP0	TMC2 CSR1
22	X	WP6	WP5	WP4	WP3	WP2	WP1	WP0	TMC2 CSR2
23	SOUT	SIN	TD5	TD4	TD3	TD2	TD1	TD0	TMC2 CSR3
30	Shift	MTS	NRPS	ENRP	X	TCH	TCH0	F/R*	TMC3 CRS0
31	X	RP6	RP5	RP4	RP3	RP2	RP1	RP0	TMC3 CSR1
32	X	WP6	WP5	WP4	WP3	WP2	WP1	WP0	TMC3 CSR2
33	SOUT	SIN	TD5	TD4	TD3	TD2	TD1	TD0	TMC3 CSR3
40	Shift	MTS	NRPS	ENRP	X	TCH	TCH0	F/R*	TMC4 CRS0
41	X	RP6	RP5	RP4	RP3	RP2	RP1	RP0	TMC4 CSR1
42	X	WP6	WP5	WP4	WP3	WP2	WP1	WP0	TMC4 CSR2
43	SOUT	SIN	TD5	TD4	TD3	TD2	TD1	TD0	TMC4 CSR3
50	Shift	MTS	NRPS	ENRP	X	TCH	TCH0	F/R*	TMC5 CRS0
51	X	RP6	RP5	RP4	RP3	RP2	RP1	RP0	TMC5 CSR1
52	X	WP6	WP5	WP4	WP3	WP2	WP1	WP0	TMC5 CSR2
53	SOUT	SIN	TD5	TD4	TD3	TD2	TD1	TD0	TMC5 CSR3
60	Shift	MTS	NRPS	ENRP	X	TCH	TCH0	F/R*	TMC6 CRS0
61	X	RP6	RP5	RP4	RP3	RP2	RP1	RP0	TMC6 CSR1
62	X	WP6	WP5	WP4	WP3	WP2	WP1	WP0	TMC6 CSR2
63	SOUT	SIN	TD5	TD4	TD3	TD2	TD1	TD0	TMC6 CSR3

Note: Address values are in hexadecimal notation.



- Integrator gain	240 mV/pC
▪ Time digitizer	
- Bin width @ 53/2 MHz	1.18 ns
- Time resolution @40 MHz (RMS)	250 ps *
- Integral non-linearity	<80 ps *
- Differential non-linearity	<60 ps *
▪ Charge digitizer	
- ADC resolution	10 bit
- Sampling frequency	53/4 MHz
- Base to Peak sampling interval	600 ns
- ADC level shifter gain	x2
- Integral non-linearity	± 1 LSB *
- Differential non-linearity	± 0.4 LSB *
- Pad charge dynamic range	0..3 pC
▪ Trigger logic & data buffering	
- Maximum drift time readout interval @53/2 MHz	1186 ns
- Trigger pulse duration range @53 MHz	38..1186 ns
- Wire signal separator resolution	< 1 ns
- Separator double pulse resolution	< 80 ns
- Digital pipeline depth (ADC and TMC)	4.8 μs
- ADC pipeline step @53/4 MHz	75 ns
- TMC pipeline step @53/2 MHz	37.7 ns
▪ Data readout and control	
- Number of wire channels	24
- Number of pad channels	48
- Level 1 FIFO event depth	> 16
- Data readout signal levels	LVDS
- Control signal levels	TTL
- Readout frequency	12.5 MHz
- Readout algorithm	fixed address sequence
▪ Physical dimensions	
- Width	21.6"
- Depth	14.0"
- Height	1.25"

▪ Power consumption for fully stuffed board (partially stuffed board)		
+5V digital		1.6 A (1.25A)
+5.5V analog		2.2 A (0.95A)
-5.5V analog		1.3 A (0.60A)

Notes: \*) indicates a chip specification parameter

### 9. Mechanical specifications and I/O connectors

A top view of the FEB is shown in Figure 5. The board dimensions are 21.60 by 14.00 inches. There are eight mounting holes around the board. These holes are used to screw on bottom and top aluminum covers. The covers provide mechanical protection and electrical shielding of the board. It is necessary to guarantee a low impedance connection between the bottom cover and a PDT body to insure low noise operation of the FEB. There are several jumpers on the FEB implemented for debugging purposes. The default positions of the jumpers are following:

▪ Jumpers JP1,JP7.....JP29 (24 ea)	-	“Mux”
▪ Jumper JP6	-	“on”
▪ Jumpers JP5,JP31,JP35,JP39,JP43,JP47 (6 ea)	-	closed
▪ remaining jumpers	-	open

The FEB has six input connectors (P1..P6), two high density connectors (P7,P8) and a power supply connector (P11). Pin header P9 is a JTAG interface and pin header P10 is a diagnostic data port. A 100 pin high density connector provides fast data readout signals, control bus signals and other specific timing and control signals (see Table III, Table IV and Table V). All readout and timing signals are use LVDS differential drivers and receivers to minimize feedback to the FEB inputs. The control bus has series-terminated TTL drivers. The readout clock frequency is 12.5 MHz and the control bus data rate is 10 Mbytes/s. One 50 pin high density connector is used for 24 trigger output signals generated by the digital one-shots (see Table VII). These signals also have LVDS levels. The Control Board provides three analog levels to set a common threshold of all wire discriminators and amplitudes of wire and pad test pulses. There is one trigger OR signal (on the P8 connector), which is generated by the FEB logic. This signal is a 24 fold OR of all the trigger outputs and is used by the CB to form an internal trigger simulating a L1 Accept. The power supply connector uses the same pinouts as the existing PDT cables. The FEB requires separate + 5 V power supply with isolated ground for digital circuitry and +/- 5.5 V analog power supplies for analog portion of the board. The pinouts for the FEB connectors are listed in the following tables.

There are four yellow LED indicators, one for each power supply voltage, located at the edge of the board. The other four LEDs are used to indicate PRUN (green), TRUN (green), ERR1 (red) and TRGOR (green) signal respectively. PRUN and TRUN have are on for normal operation of the FEB. ERR1 light indicates serious synchronization error; the board cannot be run in this condition. The TRGOR light is a trigger OR indicator.

There are two modifications of the FEB: fully stuffed and partially stuffed. The partially stuffed board has only channel #5 and channel #17 instrumented with the ADCs and charge integrators circuitry. The rest of the channels are instrumented with the TMCs for time measurements only.

The FEB can be run without forced air-cooling. Care should be taken to allow unobstructed convectional air-cooling. The normal operating ambient temperature is 25 degrees Celsius.

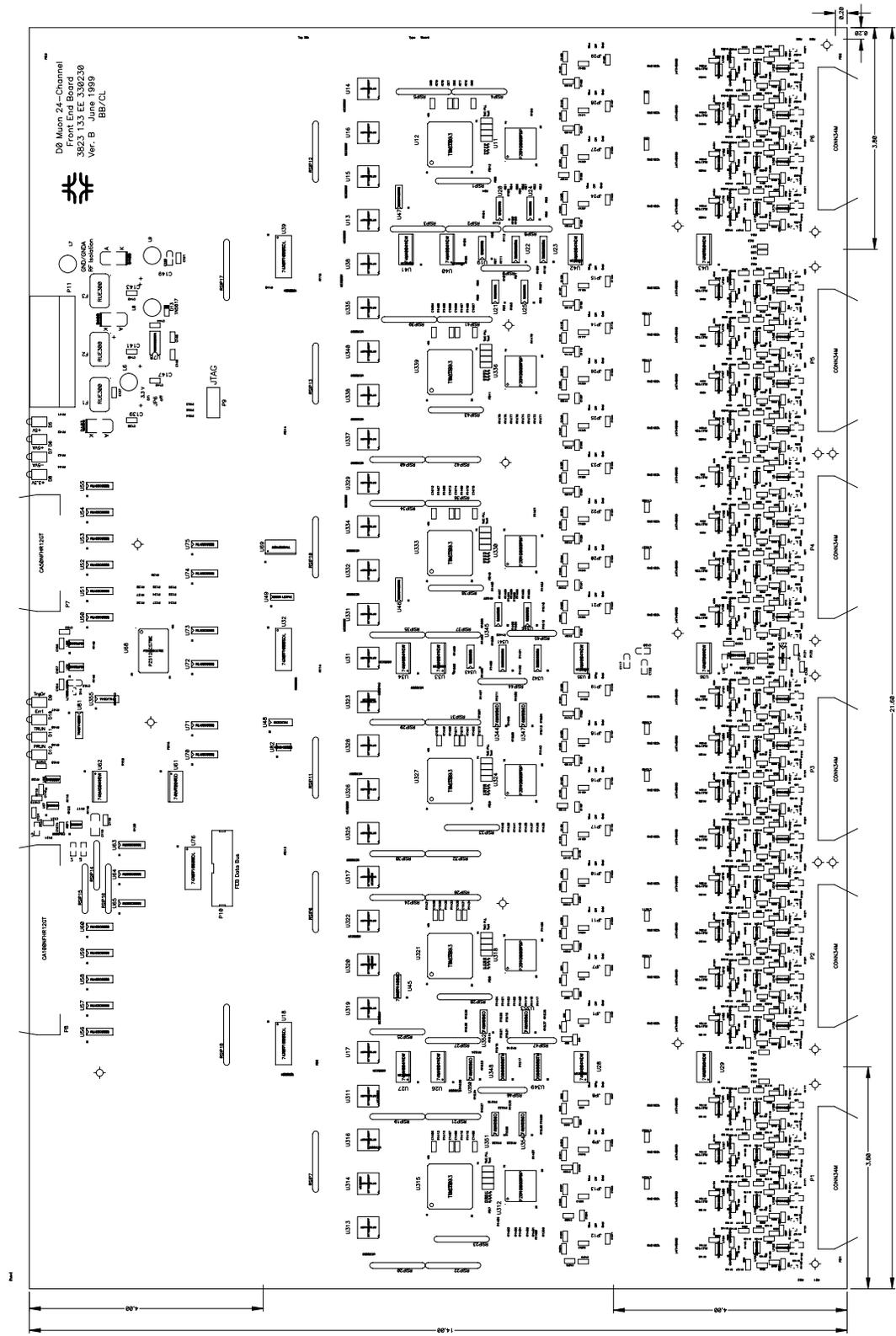


Figure 5. FEB layout and dimensions.

Table II. Input signals (P1..P6)

Pin	Signal name	Description	Comment
1,2	GND	Shield	
3	GND	Return path	GND in 3 deck board
4	P41B	Pad 4B	GND in 3 deck board
5	W41+	Wire 4 positive	GND in 3 deck board
6	W41-	Wire 4 negative	GND in 3 deck board
7	GND	Return path	GND in 3 deck board
8	P41A	Pad 4A	GND in 3 deck board
9,10	GND	Shield	
11	GND	Return path	
12	P31B	Pad 3B	
13	W31+	Wire 3 positive	
14	W31-	Wire 3 negative	
15	GND	Return path	
16	P31A	Pad 3A	
17,18	GND	Shield	
19	GND	Return path	
20	P21B	Pad 2B	
21	W21+	Wire 2 positive	
22	W21-	Wire 2 negative	
23	GND	Return path	
24	P21A	Pad 2A	
25,26	GND	Shield	
27	GND	Return path	
28	P11B	Pad 1B	
29	W11+	Wire 1 positive	
30	W11-	Wire 1 negative	
31	GND	Return path	
32	P11A	Pad 1A	
33,34	GND	Shield	

Table III. Differential LVDS signals (P8)

Pin number	Number of wires	Signal name	Description	Direction
1 to 36	36	DB00 to DB17	Readout Data (18 bits)	FEB => CB
69,70	2	TrgOR	24 channel Trigger OR	FEB => CB
71,72	2	Read/Write	Data Direction Control	CB => FEB
73,74	2	RdClk	Read Clock	CB => FEB
75,76	2	BdSel	Board Select	CB => FEB
77,78	2	Strb	Control Bus Data Strobe	CB => FEB
79,80	2	CBClk	Return Read Clock for CB	FEB => CB
81,82	2	Wire/Pad	Wire/Pad Data Indicator	CB => FEB
83,84	2	IRST	Initialization (INIT)	CB => FEB
85,86	2	WEVT	Wire event transfer signal	CB => FEB
87,88	2	PEVT	Pad event transfer signal	CB => FEB
89,90	2	53 MHz	RF Clock	CB => FEB
91,92	2	TRST	First Crossing Signal	CB => FEB
93,94	2	TEST	Test Signal	CB => FEB

Note: All odd pins are positive true signals.

Table IV. Single ended CMOS/TTL signals (P8)

Pin number	Number of wires	Signal name	Description	Direction
37	1	ERR1	Error 1 signal	FEB => CB
38	1	GND	Return path	
39	1	CB00	Control Data bit 0	CB <=> FEB
40	1	GND	Return path	
41	1	CB01	Control Data bit 1	CB <=> FEB
42	1	GND	Return path	
43	1	CB02	Control Data bit 2	CB <=> FEB
44	1	GND	Return path	
45	1	CB03	Control Data bit 3	CB <=> FEB
46	1	GND	Return path	
47	1	CB04	Control Data bit 4	CB <=> FEB
48	1	GND	Return path	
49	1	CB05	Control Data bit 5	CB <=> FEB
50	1	GND	Return path	
51	1	CB06	Control Data bit 6	CB <=> FEB
52	1	GND	Return path	
53	1	CB07	Control Data bit 7	CB <=> FEB
54	1	GND	Return path	
55	1	AD00	Control Address Line 00	CB => FEB
56	1	GND	Return path	
57	1	AD01	Control Address Line 01	CB => FEB
58	1	GND	Return path	
59	1	AD02	Control Address Line 02	CB => FEB
60	1	GND	Return path	
61	1	AD03	Control Address Line 03	CB => FEB
62	1	GND	Return path	
63	1	AD04	Control Address Line 04	CB => FEB
64	1	GND	Return path	
65	1	AD05	Control Address Line 05	CB => FEB
66	1	GND	Return path	
67	1	AD06	Control Address Line 06	CB => FEB
68	1	GND	Return path	

Note: All TTL signals are of positive true logic.

Table V. Single ended analog signals (P8)

Pin number	Number of wires	Signal name	Description	Direction
95	1	WTRS	Wire Threshold (analog)	CB => FEB
96	1	GND	Signal return path	
97	1	WTSA	Wire Test Signal Amplitude	CB => FEB
98	1	GND	Signal return path	
99	1	PTSA	Pad Test Signal Amplitude	CB => FEB
100	1	GND	Signal return path	

Note: All analog signals are 0 to + 4096 mV @ 1 K load.

Table VI. Differential LVDS signals (P7)

Pin Number	Number of wires	Signal name	Description	Direction
1,2	2	Trg01	Trigger Output 1	FEB => CB
3,4	2	Trg02	Trigger Output 2	FEB => CB
5,6	2	Trg03	Trigger Output 3	FEB => CB
7,8	2	Trg04	Trigger Output 4	FEB => CB
9,10	2	Trg05	Trigger Output 5	FEB => CB
11,12	2	Trg06	Trigger Output 6	FEB => CB
13,14	2	Trg07	Trigger Output 7	FEB => CB
15,16	2	Trg08	Trigger Output 8	FEB => CB
17,18	2	Trg09	Trigger Output 9	FEB => CB
19,20	2	Trg10	Trigger Output 10	FEB => CB
21,22	2	Trg11	Trigger Output 11	FEB => CB
23,24	2	Trg12	Trigger Output 12	FEB => CB
25,26	2	Trg13	Trigger Output 13	FEB => CB
27,28	2	Trg14	Trigger Output 14	FEB => CB
29,30	2	Trg15	Trigger Output 15	FEB => CB
31,32	2	Trg16	Trigger Output 16	FEB => CB
33,34	2	Trg17	Trigger Output 17	FEB => CB
35,36	2	Trg18	Trigger Output 18	FEB => CB
37,38	2	Trg19	Trigger Output 19	FEB => CB
39,40	2	Trg20	Trigger Output 20	FEB => CB
41,42	2	Trg21	Trigger Output 21	FEB => CB
43,44	2	Trg22	Trigger Output 22	FEB => CB
45,46	2	Trg23	Trigger Output 23	FEB => CB
47,48	2	Trg24	Trigger Output 24	FEB => CB
49,50	2	GND	Return path	

Note: All odd pins are positive true signals.

Table VII. Power supply cable (P11).

Pin number	Number of wires	Signal name	Comment
1,2	2	+5V	Digital
3,4	2	GND	
5,6	2	-5V	Digital
7,8	2	GND	
9	1	+5VA	Analog
10	1	GND A	
11	1	-5VA	Analog
12	1	GND A	

Note: GND and GND A are isolated at the source.

## 10. References

- [1] "PDT 24-channel Front End Board," Schematic drawing #3823-133-EE-330230, D0 flat files.
- [2] A.Khohlov, et al. "Muon System Electronics Upgrade," Technical Design Report, July 22, 1997, D0 Note #3299, August 1997.
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