

FEB Tester User's Guide

Introduction

The Front-End Board (FEB) Tester module is a tool for extensive computer controlled testing of 8- and 24-channel PDT Front End Boards. The FEB Tester is a single width 9U x 280mm Euroboard module with standard J1/J2 VME backplane connectors. Electrically, the FEB Tester complies with the VME standard IEEE 1014-1987 with a few minor exceptions. The FEB Tester is an A24:D16 slave. The FEB Tester requires +/- 5 volt and +/- 12 volt power supplies. The non-standard -5 volt power plane of the module is connected to pins A32, B32 and C32 on the P3 connector. This requires using a custom muon readout crate backplane or a separate power supply connected via the P3 pins described above.

The FEB Tester has four yellow LED's indicating power supply voltages and two green LED's to indicate a decoded VME command, and an external test signal. Two LEMO connectors are used for external synchronization of an oscilloscope with a test signal (TEST) and a readout sequence (EVENT), respectively. The FEB Tester also has a 50 pin and a 100 pin high-density connector for standard FEB connections and a 34 pin 3M connector to connect to an external adapter board.

The adapter board has CMOS channel switches and provides four sets of test signals for one FEB input connector. Channel masks allow any combination of the pad and wire signals on any of four channels.

Specification

1. Mechanical	9U x 280 mm Euroboard
2. VME Interface	VME slave A24:D16
3. Power supplies	+/- 5V, +/- 12V
4. FEB interface levels	LVDS/TTL
5. Adapter board interface levels	Analog/TTL
6. Synchronization signal levels	NIM, 12 mA/50 ohms
7. Time base frequency	53.1047 MHz
8. Readout frequency	12.5 MHz

FEB Tester Block-Diagram

A block-diagram of the FEB Tester is shown in Figure 1. The tester has two internal quartz oscillators, which determine the time base and readout frequencies. The Timing Generator is a Philips CPLD based sequencer, programmed to generate a standard set of timing signals synchronized to the 53/7 bunch frequency. The sequencer runs continuously after power-up. The test signal can be generated on every beam rotation period (159 bunches) or after any number of beam rotations, depending on the contents of the CSR1 register. The lower 11 bits of the register determine the lowest test pulse frequency as 23 Hz. The readout sequence is started by a delayed test pulse, but is re-synchronized to the 25 MHz oscillator. The actual readout speed is 12.5 MHz.

Because of technical limitations, the FEB Tester can only read either pad or wire data, but not both simultaneously. The data is stored in the FIFO memory validated by data bit 17, as is described in the FEB specification. An exception is the Read Pointer value, which is read out unconditionally. Only one event can be placed in memory at one time. FIFO empty and FIFO full flags are provided for diagnostic purposes. The FEB Tester has a counter that limits the number of FEB Level 1 FIFOs to be readout. This feature can be used for debugging purposes when some FEB Level 1 FIFOs are not readable. The FEB transfer signals are generated with a

programmable delay in 132 ns steps relative to the test pulse. The width of the wire transfer signal is fixed at about 500 ns and the width of the pad transfer is about 1000 ns. A six bit register is used to set the transfer signal delay, which determines the maximum delay of about 8000 ns. The readout starts with a fixed delay of 10 μ s after the test pulse is generated.

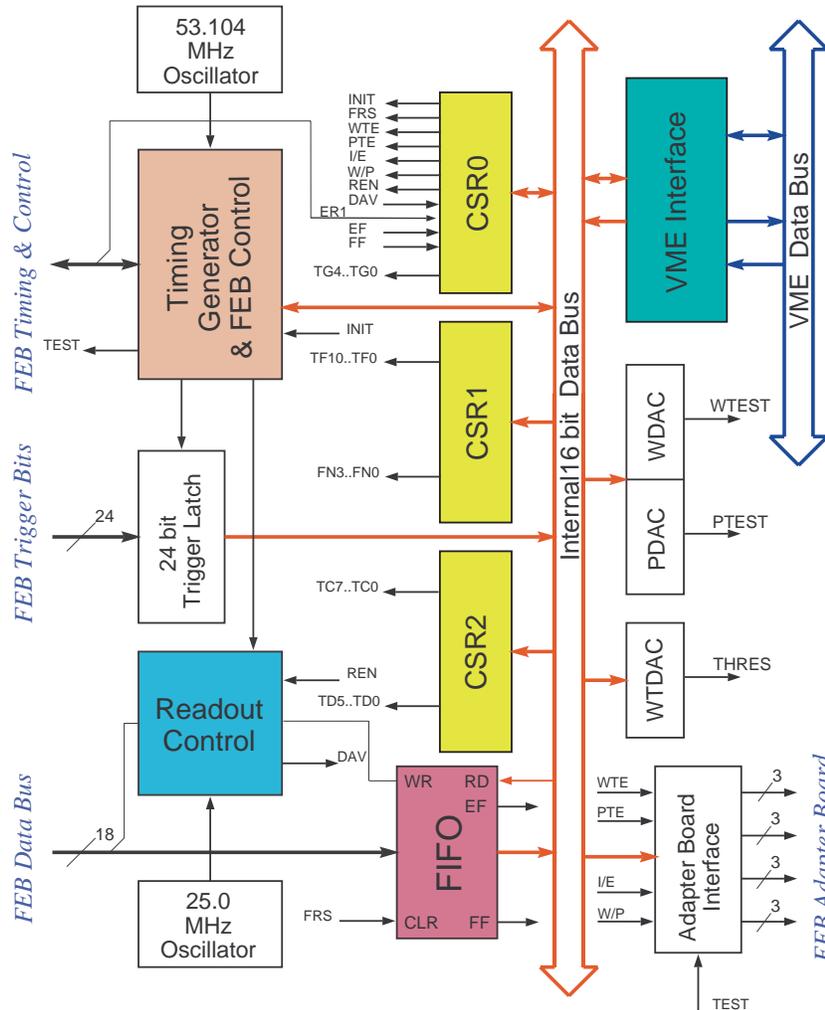


Figure 1. FEB Tester Block-Diagram.

The FEB Tester provides all the necessary signals to set up and run one FEB board. Three analog signals are generated by 8-bit DAC's to control the threshold and wire and pad test pulse amplitudes. The latter two DAC's control both the external FEB analog levels and the tester internal test pulse amplitudes. In the internal test mode, the test pulse received via the 100 pin connector is used to fire the FEB channels selected by the FEB Channel Enable register. When the on-board FEB test generators are disabled, the external adapter board can be used to fire any channels on one FEB input connector. The adapter board has channel switches that allow any combination of the pad and wire channels to be tested simultaneously. This feature can be used for detailed studies of the individual FEB channels.

A 24-bit latch is implemented to test the FEB trigger signals. The latch strobe signal is delayed relative to the test signal by approximately 500 ns. When the FEB trigger gates are set to less than that value, no signals are latched in. Increasing the gate value in the FEB settings allows a "delay curve" type measurement. A trigger OR signal duration is measured with 18.9 ns accuracy every time a test pulse is generated. The value is stored in a 5-bit counter and is readable via

CSR0. An individual trigger signal can be measured this way if all the other FEB channels are disabled by the channel mask.

A pseudo-random time measurement is implemented using a re-synchronization of the test signal by a sub-harmonic of the 25 MHz oscillator. This feature can be used for the TMC differential linearity tests.

An Error 1 bit is implemented in the CSR0 register for the final version of the FEB. The 8-channel prototype FEB doesn't have this signal.

VME Address Map

The FEB Tester uses 256 addresses for control and status registers. Two 8-bit wide switches on the board (S1 and S2) set the base address of the module. The FEB Tester translates the VME commands with address value less than \$D0 (hex) directly to the FEB control bus. Addresses between \$D0 and \$F0 are used for the FEB Tester internal status/control registers. The FEB address map is shown in Table 1.

Table 1. FEB registers VME address map.

Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Comment
02	PTEN	WTEN	TGT5	TGT4	TGT3	TGT2	TGT1	TGT0	Trigger Gate and Test
04	CE8	CE7	CE6	CE5	CE4	CE3	CE2	CE1	Channel 1-8 ENBL
06	CE16	CE15	CE14	CE13	CE12	CE11	CE10	CE9	Channel 9-16 ENBL
08	CE24	CE23	CE22	CE21	CE20	CE19	CE18	CE17	Channel 17-24 ENBL
0A	WF8	WF7	WF6	WF5	WF4	WF3	WF2	WF1	Wire FIFO 1-8 EFs
0C	WF16	WF15	WF14	WF13	WF12	WF11	WF10	WF9	Wire FIFO 9-16 EFs
0E	WF24	WF23	WF22	WF21	WF20	WF19	WF18	WF17	Wire FIFO 17-24 EFs
10	BF8	BF7	BF6	BF5	BF4	BF3	BF2	BF1	ADC FIFO 1-8 EFs
12	BF16	BF15	BF14	BF13	BF12	BF11	BF10	BF9	ADC FIFO 9-16 EFs
14	BF24	BF23	BF22	BF21	BF20	BF19	BF18	BF17	ADC FIFO 17-24 EFs
16	X	X	X	X	PEN	WEN	PRUN	TRUN	RUN Control register
18	AT8	AT7	AT6	AT5	AT4	AT3	AT2	AT1	ADC 1-8 Test ENBL
1A	AT16	AT15	AT14	AT13	AT12	AT11	AT10	AT9	ADC 9-16 Test ENBL
1C	AT24	AT23	AT22	AT21	AT20	AT19	AT18	AT17	ADC 17-24 Test ENBL
1E	X	X	AD5	AD4	AD3	AD2	AD1	AD0	ADC Pipeline Control
20	Shift	MTS	NRPS	ENRP	X	TCH	TCH0	F/R*	TMC1 CRS0
22	X	RP6	RP5	RP4	RP3	RP2	RP1	RP0	TMC1 CSR1
24	X	WP6	WP5	WP4	WP3	WP2	WP1	WP0	TMC1 CSR2
26	SOUT	SIN	TD5	TD4	TD3	TD2	TD1	TD0	TMC1 CSR3
40	Shift	MTS	NRPS	ENRP	X	TCH	TCH0	F/R*	TMC2 CRS0
42	X	RP6	RP5	RP4	RP3	RP2	RP1	RP0	TMC2 CSR1
44	X	WP6	WP5	WP4	WP3	WP2	WP1	WP0	TMC2 CSR2
46	SOUT	SIN	TD5	TD4	TD3	TD2	TD1	TD0	TMC2 CSR3
60	Shift	MTS	NRPS	ENRP	X	TCH	TCH0	F/R*	TMC3 CRS0
62	X	RP6	RP5	RP4	RP3	RP2	RP1	RP0	TMC3 CSR1
64	X	WP6	WP5	WP4	WP3	WP2	WP1	WP0	TMC3 CSR2
66	SOUT	SIN	TD5	TD4	TD3	TD2	TD1	TD0	TMC3 CSR3
80	Shift	MTS	NRPS	ENRP	X	TCH	TCH0	F/R*	TMC4 CRS0
82	X	RP6	RP5	RP4	RP3	RP2	RP1	RP0	TMC4 CSR1
84	X	WP6	WP5	WP4	WP3	WP2	WP1	WP0	TMC4 CSR2
86	SOUT	SIN	TD5	TD4	TD3	TD2	TD1	TD0	TMC4 CSR3
A0	Shift	MTS	NRPS	ENRP	X	TCH	TCH0	F/R*	TMC5 CRS0
A2	X	RP6	RP5	RP4	RP3	RP2	RP1	RP0	TMC5 CSR1
A4	X	WP6	WP5	WP4	WP3	WP2	WP1	WP0	TMC5 CSR2
A6	SOUT	SIN	TD5	TD4	TD3	TD2	TD1	TD0	TMC5 CSR3
C0	Shift	MTS	NRPS	ENRP	X	TCH	TCH0	F/R*	TMC6 CRS0
C2	X	RP6	RP5	RP4	RP3	RP2	RP1	RP0	TMC6 CSR1
C4	X	WP6	WP5	WP4	WP3	WP2	WP1	WP0	TMC6 CSR2
C6	SOUT	SIN	TD5	TD4	TD3	TD2	TD1	TD0	TMC6 CSR3

Since the FEB uses an 8-bit wide control bus, only the lower eight bits are significant when accessing the FEB registers. Higher order bits of the VME data word are ignored. The above address map is valid for the 8-channel FEB prototype only. The final version of the FEB doesn't

have any ADC test features. Therefore, the addresses used for that purpose in the 8-channel prototype will be re-assigned for the Level 1 FIFO full flags.

FEB Tester internal registers map is shown in Table 2.

Table 2. FEB Tester internal registers VME address map.

Address	Access	# of bits	Description
D0	read-write	16	CSR0 control register
D2	write-only	16	CSR1 control register
D4	write-only	16	CSR2 control register
D6	write-only	16	Wire and Pad test signal DACs
D8	write-only	8	Wire threshold DAC
DA	write-only	16	Wire and Pad test signal mask registers
DC			Reserved
DE			Reserved
E0	write-only	16	Increment FIFO read pointer (data = \$0001)
E2			Reserved
E4			Reserved
E6			Reserved
E8	read-only	16	Trigger bits 0..15 register
EA	read-only	8	Trigger bits 16..23 register
EC	read-only	16	FIFO data bits 0..15
EE	read-only	8	FIFO data bits 16,17 and flags

FEB Tester internal registers

There is one read-write register, six write-only registers and four read-only registers in the FEB Tester. This paragraph describes the individual bits in FEB internal registers.

- CSR0 (\$D0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TG4	TG3	TG2	TG1	TG0	FF	EF	ER1	DAV	REN	P/W	I/E	PTE	WTE	INIT	FRS

- FRS - Reset FIFO (write 1 to reset FIFO)
- INIT - INIT signal level (0 – low, 1 – high)
- WTE - external Wire Test Enable
- PTE - external Pad Test Enable
- I/E - 0 – Internal FEB test, 1 – External tester test
- W/P - Wire (1) or Pad (0) data to be readout
- REN - Readout Enable
- DAV - Data is Available in the tester FIFO memory (read-only)
- ER1 - Error 1 bit from FEB (read-only)
- EF - FIFO Empty Flag (read-only, 0 - empty)
- FF - FIFO Full Flag (read-only, 0 - full)
- TG4..TG0 - Trigger OR signal duration in 18.9 nS units (read-only)

- CSR1 (\$D2)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NC	FN3	FN2	FN1	FN0	TF10	TF9	TF8	TF7	TF6	TF5	TF4	TF3	TF2	TF1	TF0

TF10..TF0 - Test pulse Frequency register (beam rotation number)

FN3..FN0 - Number of FIFOs to read register (max 12)

- CSR2 (\$D4)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RM	NC	TD5	TD4	TD3	TD2	TD1	TD0	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0

TC7..TC0 - Test pulse Crossing number

TD5..TD0 - data Transfer Delay in 132 nS units

RM - enable Random time Measurements

- WPDAC (\$D6)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PT7	PT6	PT5	PT4	PT3	PT2	PT1	PT0	WT7	WT6	WT5	WT4	WT3	WT2	WT1	WT0

WT7..WT0 - Wire Test pulse amplitude

PT7..PT0 - Pad Test pulse amplitude

- WTDAC (\$D8)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
NC	NC	NC	NC	NC	NC	NC	NC	NC	TR7	TR6	TR5	TR4	TR3	TR2	TR1	TR0

TR7..TR0 - wire Threshold level

- WPMSK (\$DA)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P4B	P4A	P3B	P3A	P2B	P2A	P1B	P1A	P4	P3	P2	P1	W4	W3	W2	W1

W4..W1 - Wire 1 to 4 external test pulse mask

P4..P1 - Pad 1 to 4 external test pulse mask

P4B..P1A - Pad A and Pad B select mask

- FIFORP (\$E0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	IRP

IRP - Increment FIFO Read Pointer (write \$0001)

- TGATE0 (\$E8)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TG15	TG14	TG13	TG12	TG11	TG10	TG9	TG8	TG7	TG6	TG5	TG4	TG3	TG2	TG1	TG0

TG15..TG0 - Trigger bits 15..0 register

- TGATE1 (\$EA)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NC	NC	NC	NC	NC	NC	NC	NC	TG23	TG22	TG21	TG20	TG19	TG18	TG17	TG16

TG23..TG16 - Trigger bits 23..16 register

- FDATA0 (\$EC)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FD15	FD14	FD13	FD12	FD11	FD10	FD9	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0

FD15..FD0 - FIFO data bits 15 to 0

- FDATA1 (\$EE)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NC	NC	NC	NC	NC	NC	NC	NC	FF	HF	AF	EF	0	0	FD17	FD16

FD17,FD16 - FIFO data bits 16,17 (bit 17- Data Valid, 0 – Event Separator, 1 – Data Valid)

EF - FIFO Empty Flag (0 - empty)

AF - FIFO Almost full Flag (1 – after reset, 0 – more than 32 words in FIFO)

HF - FIFO Half full Flag (0 – after reset, 1 – more than 128 words in FIFO)

FF - FIFO Full Flag (0 - full)

Initialization

After power-up, the FEB and the FEB Tester card require proper initialization. The initialization has to be done at every start-up of the program. Initialization can also be done at any time during testing.

FEB Tester Initialization

FEB Tester initialization sets up internal registers. There are default initialization values for the first FEB Tester initialization. Most of the FEB Tester parameters used for initialization can also be controlled from the command menu. The following is a list of the FEB Tester parameters and their default values.

Table 3. FEB Tester default parameters.

Address	Value (hex)	Units	Comment	Command
D0	X400	N/A	CSR0 register ¹⁾	Yes ²⁾
D2	6060	N/A	CSR1 register	Yes
D4	0D77	132 nS	CSR2 register	Yes
D6	8080	16 mV ³⁾	Wire and Pad Test pulse amplitude	Yes
D8	0080	16 mV ³⁾	Wire threshold level (relative)	Yes
DA	FFFF	N/A	Wire and Pad external test masks	Yes

Notes:

1. FRS write-only bit is used to reset FIFO memory.
2. Various CSR0 bits are used in different Menu Commands.

- The DAC full-scale output is 4096 mV.

Front End Board Initialization

The FEB initialization procedure starts with setting the INIT bit in CSR0 to one. This bit has to be reset to zero after initialization is complete. There are default initialization values for the first FEB initialization. Most of the FEB parameters used for initialization can also be controlled from the command menu. The following is a list of FEB parameters and their default values.

Table 4. FEB default parameters.

Address	Value (hex)	Units	Comment	Command
02	CF	18.8 nS	Trigger Gate width and Test Control	Yes
04	AA	N/A	Channel 1-8 Enable bits	Yes
06	AA	N/A	Channel 9-16 Enable bits	Yes
08	AA	N/A	Channel 17-24 Enable bits	Yes
16	00	N/A	Run Control Register ¹⁾	Yes
18	00	N/A	ADC 1-8 test Enable bits	Yes
1A	00	N/A	ADC 9-16 test Enable bits	Yes
1C	00	N/A	ADC 17-24 test Enable bits	Yes
1E	19	75.3 nS	ADC pipeline delay	Yes
22	38	37.7 nS	TMC1 read pointer	Yes ²⁾
24	0	37.7 nS	TMC1 write pointer	Yes ²⁾
42	38	37.7 nS	TMC2 read pointer	Yes ²⁾
44	0	37.7 nS	TMC2 write pointer	Yes ²⁾
62	38	37.7 nS	TMC3 read pointer	Yes ²⁾
64	0	37.7 nS	TMC3 write pointer	Yes ²⁾
82	38	37.7 nS	TMC4 read pointer	Yes ²⁾
84	0	37.7 nS	TMC4 write pointer	Yes ²⁾
A2	38	37.7 nS	TMC5 read pointer	Yes ²⁾
A4	0	37.7 nS	TMC5 write pointer	Yes ²⁾
C2	38	37.7 nS	TMC6 read pointer	Yes ²⁾
C4	0	37.7 nS	TMC6 write pointer	Yes ²⁾

Notes:

- The Run Control register has to be set to zero before setting up TMC read/write pointers. It has to be set to 0F at the end of initialization.
- INIT has to be set high and the Run Control register has to be set to 00 during pipeline registers setup.

FEB Tester Software

The FEB Tester software allows interactive access to all FEB and FEB Tester registers and generates fixed mode algorithms for automated testing. It runs on a MVME162 Motorola based processor and uses an Ethernet connection to a Unix host for program downloading and data storage. A standard terminal or PC has to be connected to the processor's RS-232 port. After start up the program generates the following screen (shown in blue Italic):

Choose an option:

- 1. Set parameters to default values*
- 2. List initialization parameters*
- 3. Initialize with current values*
- 4. Set Run Mode*
- 5. Set Pulser Frequency*
- 6. Change a Register on FEBTester*
- 7. Change a Register on the FEB*

- 8. Run data
- 9. Exit the program

Each command from this menu is described below.

1) *Set parameters to default values* sets the following values (hex):

- CSR0 = 5400, CSR1 = 6060, CSR2 = 0D77
- Trigger Gate & Test = CF
- Run Control Register = 0F
- ADC Pipeline Control = 19
- Channel Enable Registers (all) = AA
- TMC 1..6 Read pointer (all) = 38
- TMC 1..6 Write Pointer (all) = 00
- Pulser Frequency - 500 Hz
- Wire Threshold - 2048 mV
- Wire test pulse height - 2048 mV
- Pad test pulse height - 2048 mV

2) *List Initialization parameters* prints the following screen:

CSR0 = bc00 CSR1 = 6060 CSR2 = 0d77

tbits1 = ffff tbits0 = ffff

fdat1 = a3 fdat0 = ffff

Trig. Gate & Test = cf

Run Cntrl Reg. = 0f

ADC Pipeln Cntrl = 19

Channel Enable aa aa aa

L1 FIFO EF 00 00 00

ADC Pipeline EF ff ff ff

ADC Test Enable 00 00 00

TMCTDC CSR0 RP WP CSR3

1 ff 57 1f 7f

2 ff 57 1f 7f

3 9f 1f 1f 1f

4 9f 1f 1f 1f

5 9f 1f 1f 1f

6 9f 1f 1f 1f

Hit Return for more parameters, m for menu

Pulser Frequency 500 Hz.

Wire Threshold 2048 mVolts

Wire test pulse height 2048 mVolts

3) *Initialize with current values* initializes the FEB with the values displayed in the previous command. Any value can be changed using commands 5 to 7 of the menu.

4) *Set Run Mode* prints the following screen:

Choose Run Option:

- 1. Wire Internal*
- 2. Wire External*
- 3. Pad Internal*
- 4. Pad External*

and, after selection is made asks for two more selections:

Would you like to write a file? (y or (n)) n

Would you like random times ? (y or (n)) n

At this point, the program is ready to receive events of the selected type. As the menu suggests, events can be printed on the screen or stored in a file on the host computer for further analysis.

5) *Set Pulser Frequency* sets the frequency in the range 100 Hz..1kHz. Any other test frequency values between 23 Hz and 24 kHz can be set by accessing the CSR1 register directly.

6) *Change a Register* on FEBTester allows access to the FEBTester registers through the following menu:

Which Tester Board register would you like to change?

- 1. CSR0 control register*
- 2. CSR1 control register*
- 3. CSR2 control register*
- 4. Wire test signal DAC*
- 5. Pad test signal DAC*
- 6. Wire threshold DAC*
- 7. Wire and Pad test signal mask registers*
- 8. previous menu*

The desired value has to be entered in hex according to the bit description of this manual.

7) *Change a Register on the FEB* allows access to the FEB registers through the following menu:

Which FEB register would you like to change?

- 1. Trigger Gate and Test*
- 2. Channel Enable*
- 3. RUN control*
- 4. ADC Test Enable*
- 5. ADC Pipeline Control*
- 6. TMC Control*
- 7. previous menu*

These values have to be entered in hex as well.

8) *Run data starts* data taking with the selected event type. The program asks for settings of the data taking as following:

Mode is Wire Internal

How many events would you like ?

10

Chose print option:

- 1. Print all data available*
- 2. Print only non-zero data*
- 3. Print only summary*

A sample of the wire internal data event and summary display is shown below:

trigger bits ffff00

Trig-OR width 10 counts (Hex)

fdat b10404

ch # 02 fdat b325c0 coarse time 09 hi-time bits 0e time1 ae

ch # 04 fdat b32580 coarse time 09 hi-time bits 0c time1 ac

ch # 06 fdat b32520 coarse time 09 hi-time bits 09 time1 a9

ch # 08 fdat b32520 coarse time 09 hi-time bits 09 time1 a9

fifo count (hex) 12

ch # 02 mean 174.00 RMS 0.47
ch # 04 mean 173.70 RMS 0.67
ch # 06 mean 169.10 RMS 0.31
ch # 08 mean 169.70 RMS 0.48

Trig-OR width mean 302.40 (nanoseconds)

value 18 entries 10

Hit Return for Menu

9) *Exit the program* – allows you to exit the program.

The FEB Tester software described in this section is still under development. The next step is to design automatic routines to run specific checks through all 24 channels without operator intervention. A new version of software and a new manual will be released after the full size prototype Front End Board is available for testing.

References

1. A.Khohlov, et al., "Muon System Electronics Upgrade", Technical design report, D0 Note #3299, August 1997, Fermilab
2. D0 Muon Electronics web page, http://www-d0.fnal.gov/muon_electronics/index.html