

1 Introduction

The first design, developed by Anton Smith¹, is quite robust, and it has a straightforward architecture. It was tested for most of the values showed in his Technical Design Report by August this year. Then the interaction and the cabling involved in the chain Sequencer-AFE, using 1553², added more latency than expected, so a new design with very few variations came up.

The latest design does not have the fine-tuning that the previous one, which prevents for having an 8 nanoseconds adjustment steps. Instead of that, it has only a 19 nanoseconds scale.

2 Changes from the previous design

The basic change is related to the tuning-scale of the delay. Also, the previous version uses a description by default of the 16 to 1 multiplexors, which has some problems in the routing and implementation processes.

2.1 Scale

The scale has been changed looking for an answer about the problems with the facing clocks used for NRZ and NRZ prime.

The new design does not use the Less Significant Bits of the byte that puts the information into the Sequencer. It modifies the scale steps for the delay tuning.

2.2 Multiplexors definition

Mike Utes helped us to review the previous design. The logic was properly arranged, and the functionality tested in the simulator.

However, the compiler from Altera does not offer an accuracy routing performance. The selected PLD³, Altera MAX family, has some problems in the modules that the fabricant provides for developing. The compiler assigns any kind of buffer (Logic Cell or line without it) when a 'soft' component is defined.

Mike Utes assigned a fix value for it, Logic Cell, and the compiler routed in the same way all of the outputs.

¹ Summer Project. Anton Smith.

² 1553: Protocol of communication

³ EPM7128STC100-10

3 Test Results

The test was performed, setting up a chain 1553-Seq-AFE-PC. The first try involved the CFT GUI⁴ used in CTS⁵, which showed some problems in the facing clocks. After the first modification, it was used again with no changes in the results.

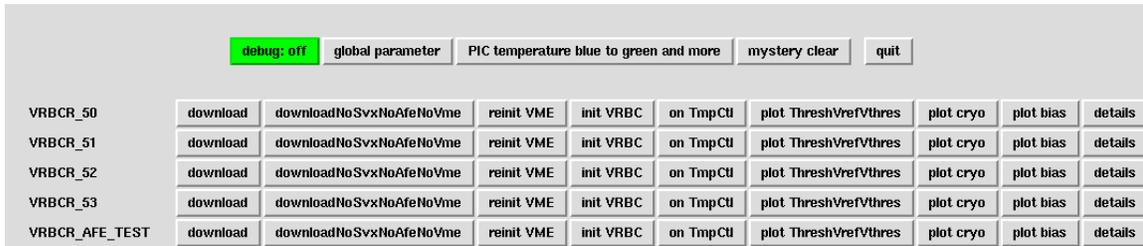


Figure 1 CFT GUI

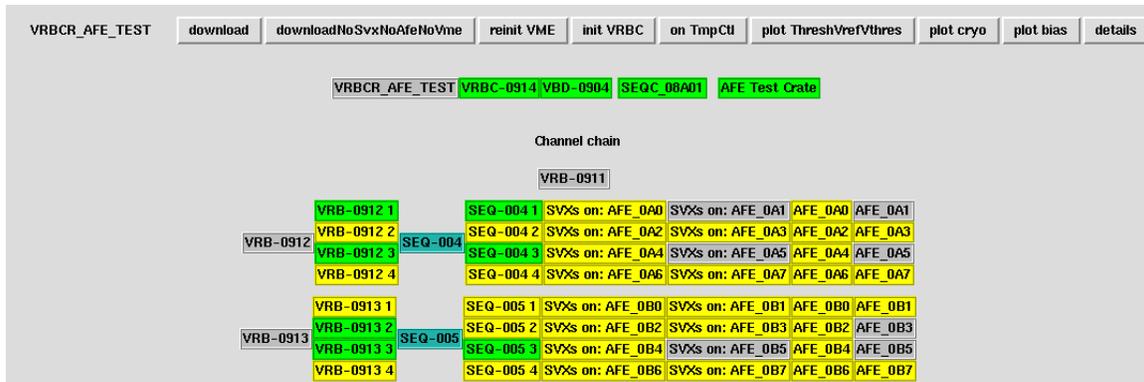


Figure 2 CFT GUI for CTS Crate

The second try was based in the Spread Sheet⁶ used by Mike Utes. This configuration required one PC and a Bit3⁷ board. The design was working for all of the values but no for one. Then, the problem was solved changed the Mux definition.

The easiest way for looking the AFE output was attaching a probe to the Beginning Of Turn (BOT), which is available via test output pins.

⁴ GUI: Graphic User Interface.

⁵ CTS: Combined Test Stand

⁶ Sequencer Spread Sheet: Developed in Excel. It uses the PC Ethernet port for sending information to a separated RT 1553 module.

⁷ Bit3-SBS Technologies

The Combined Test Stand (CTS) is configured in such a way that it is possible to simulate the whole chain of electronics, from the collision point to the final stage in Level 3 decision.

The AFE Crate is located at the left of CT, giving accessibility to two racks of 8 AFE each. The AFE represented in orange are named crate A and the magenta ones are crate B in the CFT GUI.

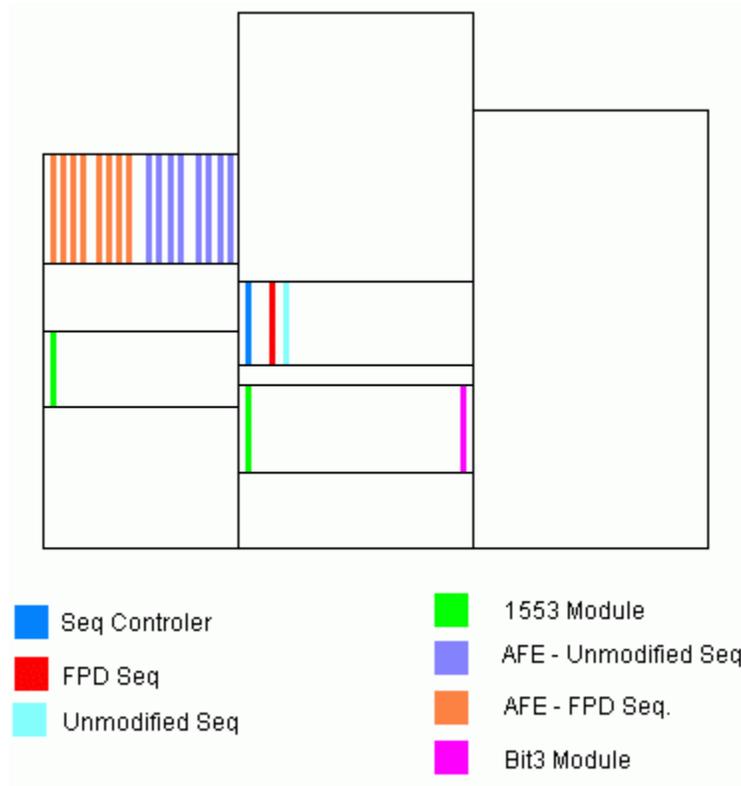


Figure 3 CTS Configuration

The following figures show the configuration used in the test. The reference signal was taken from the SCL⁸, which is the Sync Gap (yellow) with a period of 21microseconds. The green signal is coming from an AFE⁹ attached to one unmodified sequencer. The Purple one is obtained reading the output of an AFE linked to the FPD Sequencer Upper PLD delay, and the blue one used the output of the Lower PLD delay.

⁸ SCL: Serial Command Link

⁹ AFE: 8-MCM Analog Front End board.

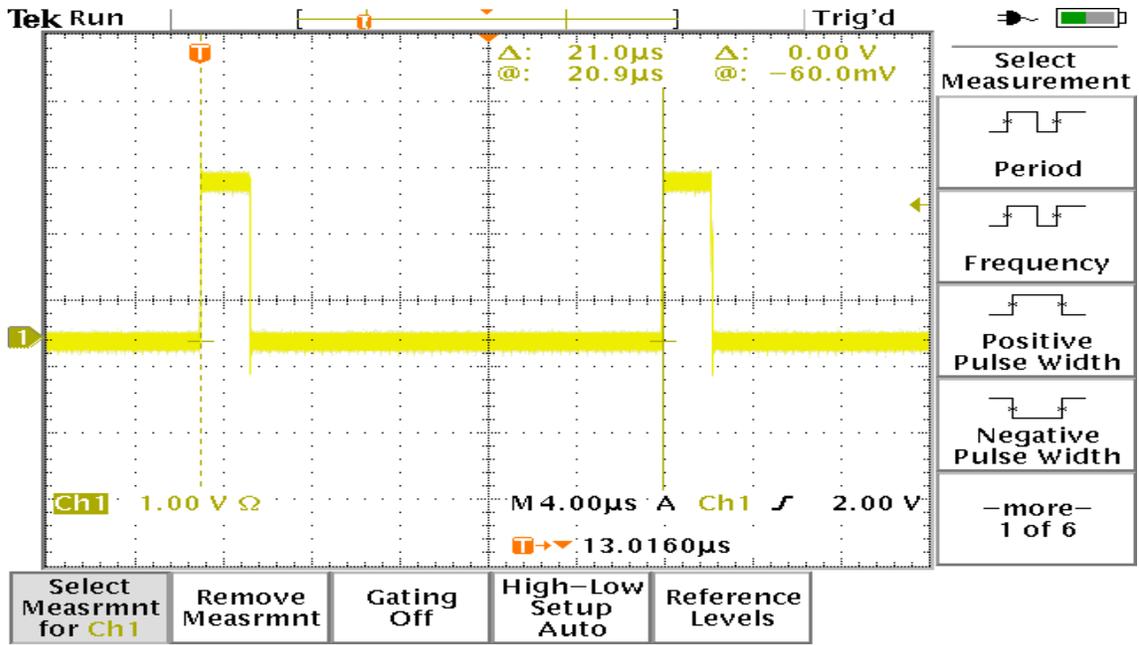


Figure 4 Sync Gap reference signal

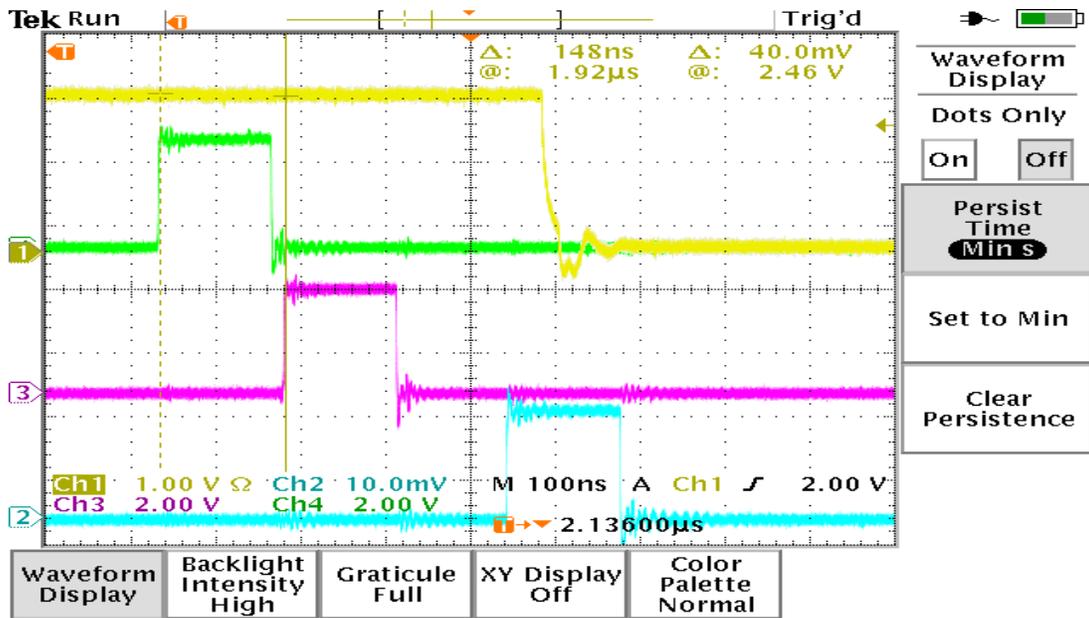


Figure 5 Delays compared to the Unmodified Sequencer signal

3.1 Table

The table obtained from the test performed in DAB3, with a PC attached directly to the Sequencer via 1553, is the following. These values have an error of +/- 10 nanoseconds.

Table 1 New delay values

Hex values		Dec values		Delay 1 Upper Sequencer PLD (ns)	Delay 2 Lower Sequencer PLD (ns)
00	00	0	0	184	410
04	04	4	4	202	426
08	08	8	8	220	446
0c	0c	12	12	240	462
10	10	16	16	260	482
14	14	20	20	274	502
18	18	24	24	296	520
1c	1c	28	28	316	540
20	20	32	32	334	558
24	24	36	36	352	578
28	28	40	40	372	598
2c	2c	44	44	390	614
30	30	48	48	408	630
34	34	52	52	428	652
38	38	56	56	446	670
3c	3c	60	60	466	690
3f	3f	63	63	466	690

Note: the values between 0 and 3 do not make any change in the obtained delay value. For example:

Table 2 Example of dialing

Expected Delay 1 (ns)	Hex value	Binary Value
466	3 C	0011 1100
466	3 D	0011 1101
466	3 E	0011 1110
466	3 F	0011 1111

3.2 Modified CFT GUI

Jadwiga Warchol and Victor Bodyagin have provided us with a FPD GUI, which has a tab for putting both delays (upper and lower).



Figure 6 Sequencer Menu - fpd_del 1 & fpd_del 2

4 DAQ Tests

4.1 Data Taker

Using a Logic Analyzer attached to one AFE board output was possible to see the signals coming out from one AFE board linked to FPD Sequencer.

Three signals must be looked for before assume that AFE is recognizing Sequencer signals; these signals are SVX clock ('clock' in the figure, color green), Level 1 Accept trigger ('l1accept' in blue), and Discriminator signal ('disc').

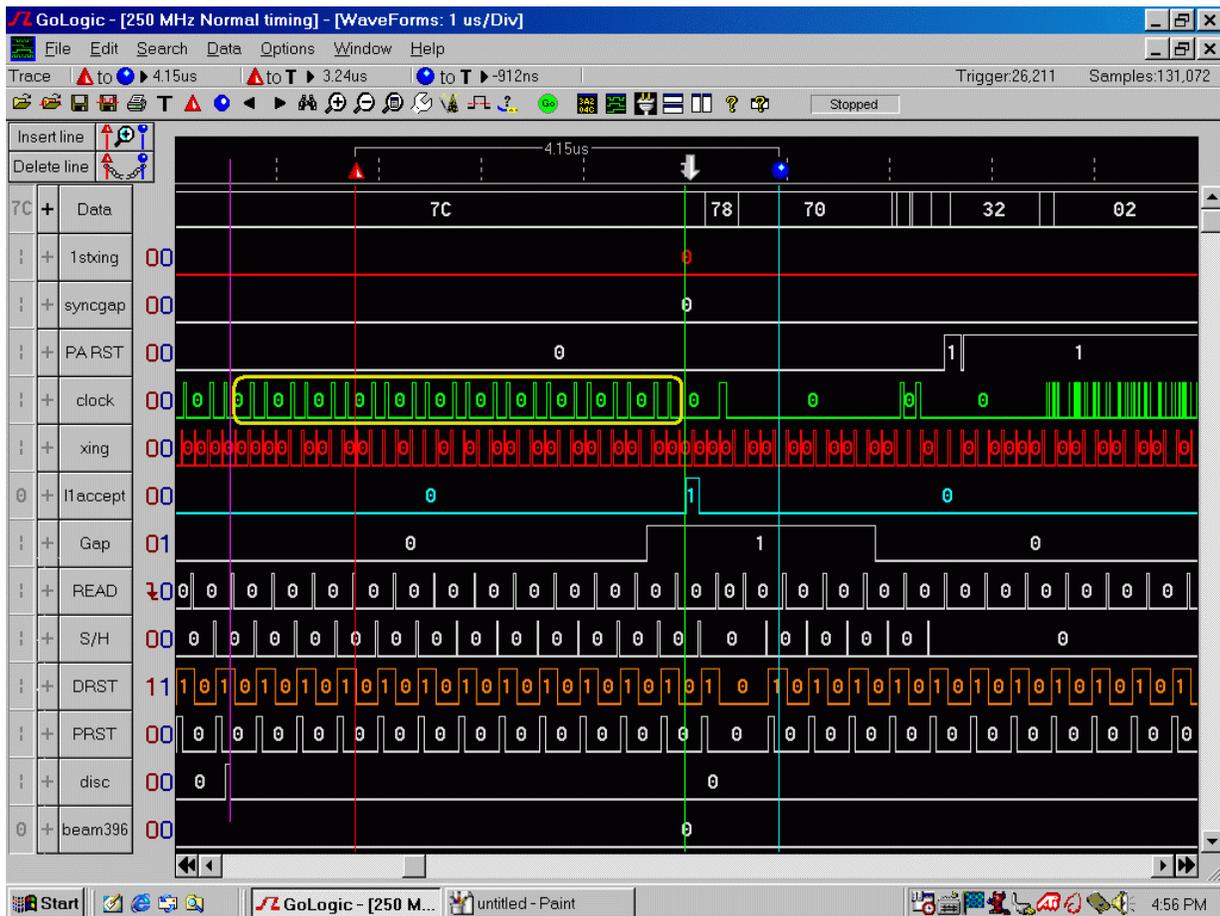


Figure 7 Logic Analyzer Waveform Output

Performing a count over the SVX clock, from the point in which L1 Accept appears to the point in which Discriminator signal is high, it have 22 clock cycles. In the above figure, the SVX clocks have been enclosed into a yellow globe. This count is showing 22 steps, which are the read capacitors.

Using the Data Taker is possible to read the VSVX¹⁰ output of AFE. Fred Borcharding has helped us to configure it in CTS.

Running a SDAQ, it is possible to have a good estimated value of the AFE outputs. After download some Voltage of Reference for the SVX, the 'CFT Online Calibration and Monitoring GUI' shows a set of histograms that can be used for analyzing how the AFE channels are set.

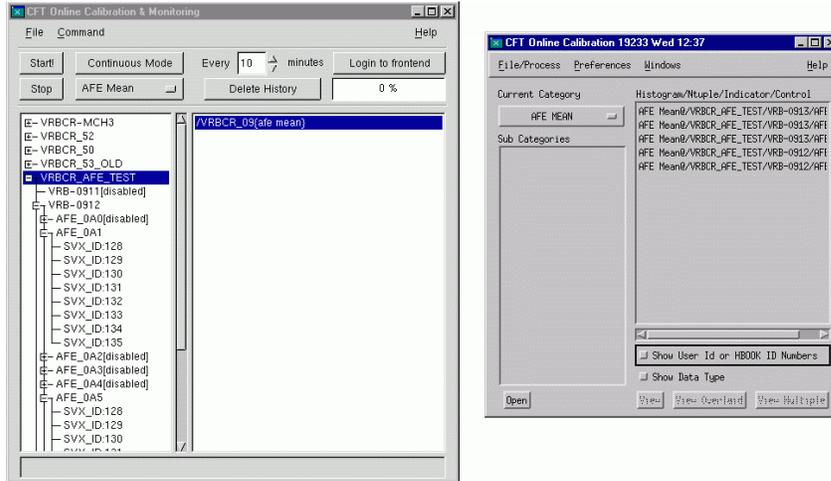


Figure 8 CFT GUI for Calibration and Monitoring – SDAQ

The following figure shows a set of AFE outputs using SDAQ. The upper graphs represents the 'AFE Voltage Ref. Mean' using FPD sequencer, and the lower ones show a set of AFE attached to an unmodified sequencer. Please, ignore the lowermost right graph, for it uses a different source, giving a different value in 'V-Ref. Mean'.

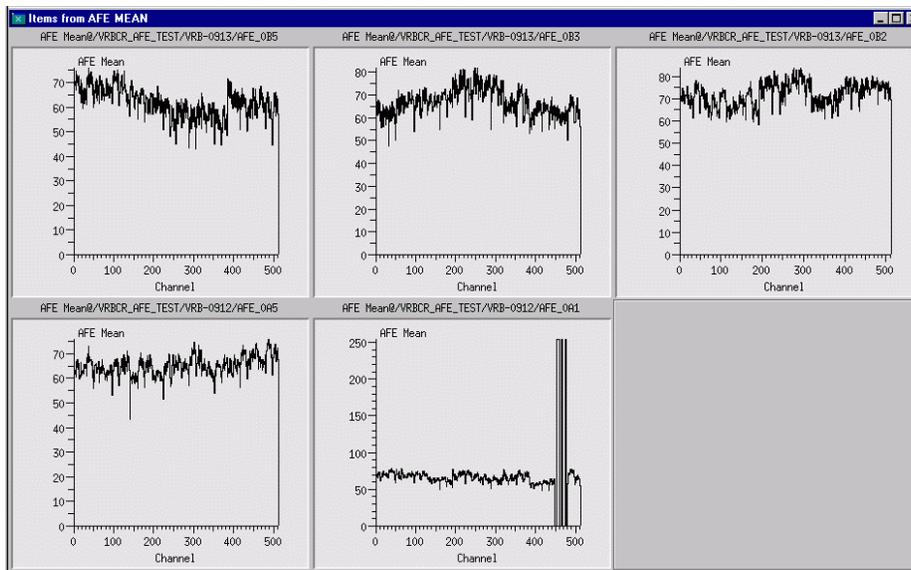


Figure 9 AFE Mean - SDAQ Run Selection

¹⁰ VSVX: Virtual SVX