

From: Brendan Casey <bcasey@fnal.gov>  
Sent: Tuesday, December 10, 2002 4:37 PM  
To: Andrew Brandt  
Subject: fpga code

Hi Andrew,

Here is the FPGA code. When you've identified someone to work on this put them in contact with me.

They will first need to learn verilog and have some basic knowledge of digital electronics. Understanding a flip-flop and a mux are enough to get started.

Some good verilog resorces are at  
<http://www.see.ed.ac.uk/~gerard/Teach/Verilog/index.html>

They will need to get a simulator. These can be very expensive however most companies usually offer educational discounts for factors of 10 below the base price. I am using SILOS from SIMUCAD. I dont know how much it was. They will need to shop around. There may even be something free on the web somewhere.

There are 4 Xilinx Spartan II XCS40PQ240-3 chips on the board that are connected to ATMEL AT17C512 EEPROMs but thats probably more information than is necessary.

The file to FPGA correspondence is

CHAN\_FPGA:  
twochannelsver14.v  
singlechannelver14.v  
rampointerver14.v

VTX\_FPGA:  
lm0ver10.v  
pick32ver9.v  
rank4ver9.v  
get32from8ver9.v

XCK\_FPGA:  
xckmodule\_13.0.0.v  
busyerrorinit\_13.0.0.v  
rampointer\_13.0.0.v

VME\_FPGA:  
vmemodulever\_13.0.0.v  
vmeaddress\_13.0.0.v