

Forward Proton Detector (FPD)

Level 1 – Implementation of the Trigger Equations Firmware Design

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for the FPD collaboration

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1 Introduction

The Forward Proton Detector makes use of CTT electronics to trigger and readout its scintillating fiber detectors.

One of the boards of the CTT reading chain has been denominated Digital Front End Boards (DFE) [3]. This board takes the information to obtain trigger terms, which will go to the Trigger Manager (TM).

FPD DFE, type Double Wide Daughter Board (DWDB), has three Xilinx FPGAs [2], which have a BGA (Ball Grid Array) [4] disposition for their pins.

All of the FPGAs devices share the Level 3 information bus. The JTAG configuration line goes from CPLD 1 to CPLD 2. As an example, we could consider Dipole design which will be located in the fourth device for the MB devices chain, but it would be the third one for DWDB.

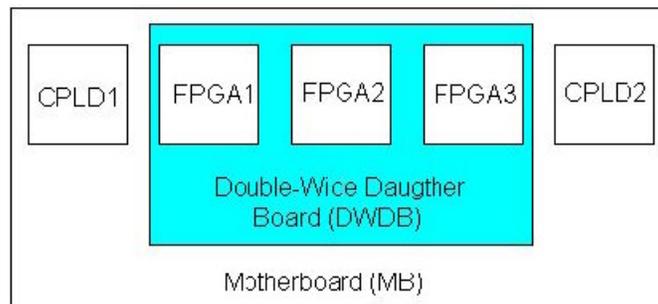


Figure 1 FPD DFE Board Disposition.

Each DFE offers four links, which can be used for communication using LVDS or FSCL links. Figure 2 shows those paths.

Note 1: Level 3 output is shared by all of the devices.

Note 2: MB has 10 LVDS links coming in, from which FPD design will use two, three or four. Depending of the detectors coming in.

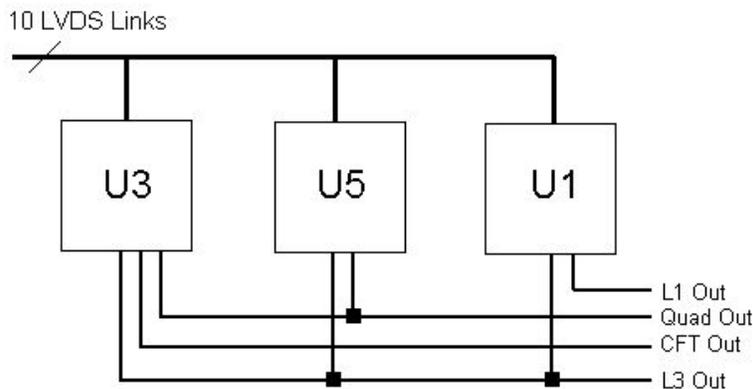


Figure 2 FPD DWDB devices disposition

Figure 3 shows a possible way to send the information to the Trigger Manager. U5 would take care of sending the information to the next level.

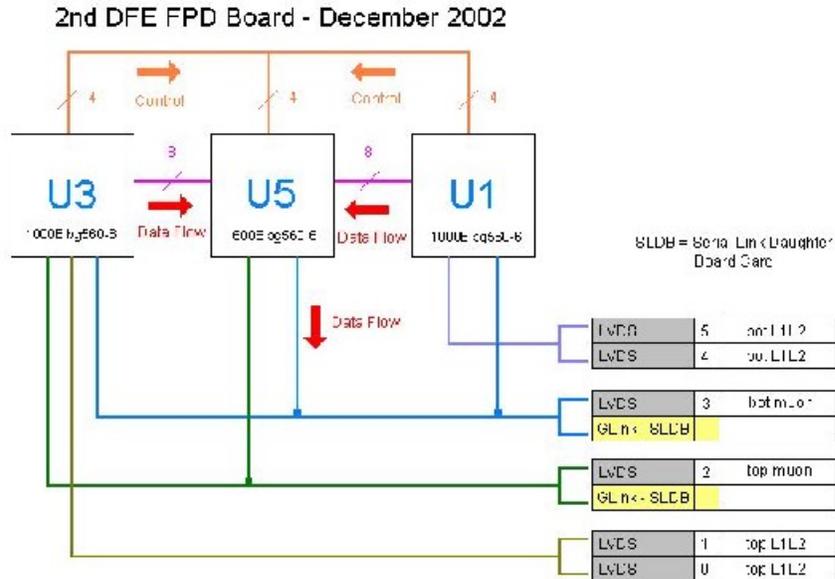


Figure 3 2nd FPD DFE board

2 Overview

All of the information to DFE is coming from the PW08 rack, which is located at the west platform in Collision Hall. This rack contains a crate with all of the AFE boards and sends the information through LVDS links. The distribution of the AFE boards can be found in Figure 4.

3 Protocols

3.1 Input

All of the information arriving to DFE comes from Analog Front End boards (AFE) located in PW08 into the Collision Hall.

AFE¹ board sends to DFE² seven 21-bit packets (147 bits) every 132 ns³, and this information is embedded in a seven 28-bit packets (196 bits) –every 132 ns –.

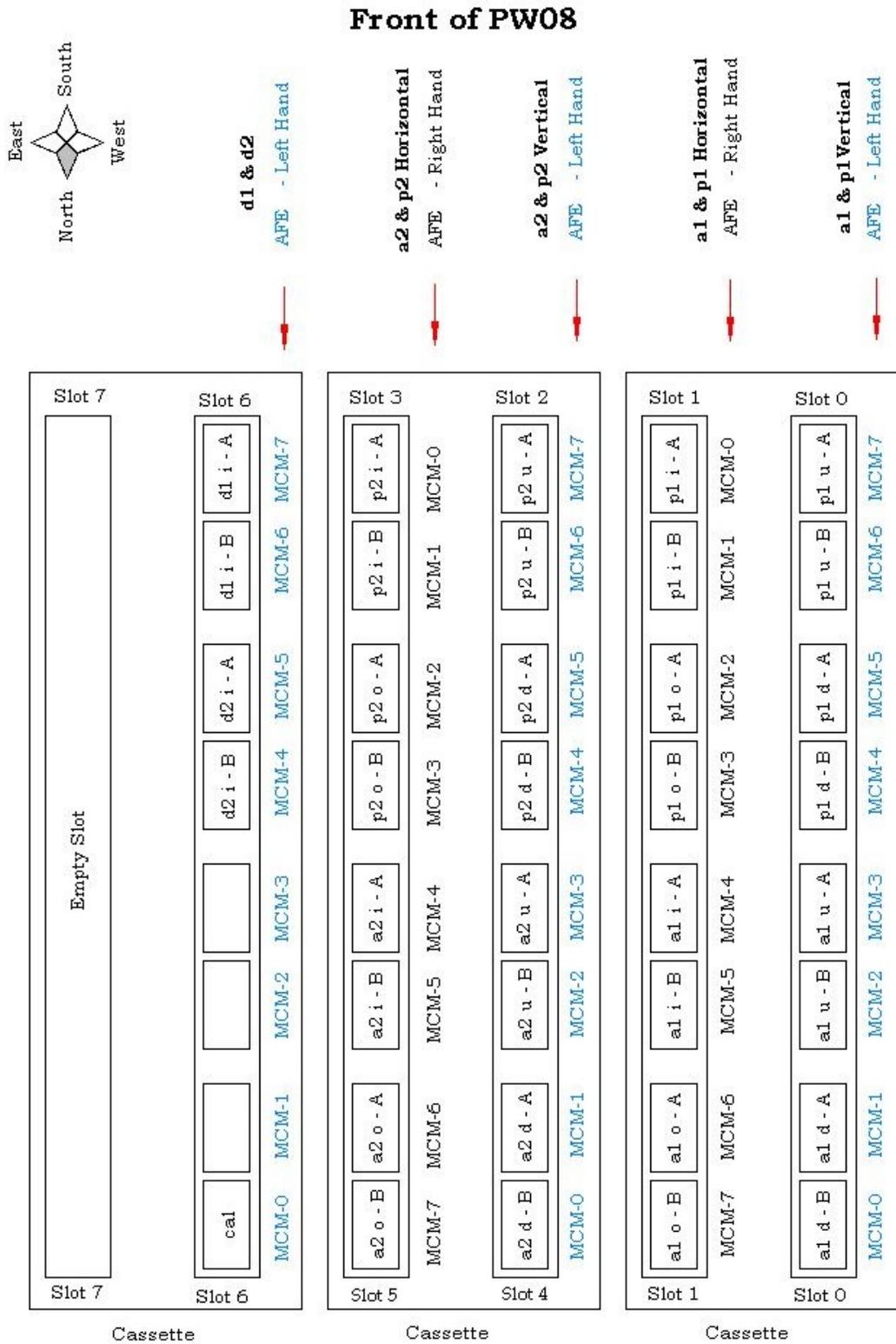
The general scheme shows (Figure 5) 6 independent bits (by MCM⁴), which help to bring information from sequencer. This information will be used in global control and synchronization. The information coming from each detector has been arranged as appears in Figure 5. Also, it is important to point out that bit number 00 has been reserved in order to indicate the end of each frame.

¹ AFE: Analog Front End board

² DFE: Digital Front End board

³ Anderson, John T. "Discriminator data path for CPS fibers in AFE boards." Document number: A1020718. July 18th, 2002.

⁴ MCM: Multi Chip Module



	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	00	
21-bit link																						
28-bit link																						
Frame 1	xd19	xd37	xd55	xd02	xd20	xd38	xd56	xd65	xd12	xd30	xd19	xd37	xd55	xd02	xd20	xd38	xd56	xd65	xd12	xd30	0	
Frame 2	xd01	xd54	xd27	xd18	xd09	xd00	xd36	xd45	xd63	xd10	xd01	xd54	xd27	xd18	xd09	xd00	xd36	xd45	xd63	xd10	0	
Frame 3	xd57	xd39	xd21	xd03	xd47	xd29	xd11	xd64	xd46	xd28	xd57	xd39	xd21	xd03	xd47	xd29	xd11	xd64	xd46	xd28	0	
Frame 4	xd42	xd24	xd68	xd50	xd32	xd14	xd67	xd49	xd22	xd04	xd42	xd24	xd68	xd50	xd32	xd14	xd67	xd49	xd22	xd04	0	
Frame 5	xd71	xd62	xd53	xd44	xd17	xd70	xd43	xd25	xd07	xd60	xd71	xd62	xd53	xd44	xd17	xd70	xd43	xd25	xd07	xd60	0	
Frame 6	xd33	xd51	xd69	xd16	xd34	xd52	xd61	xd08	xd26	xd35	xd33	xd51	xd69	xd16	xd34	xd52	xd61	xd08	xd26	xd35	0	
Frame 7	sqr1	sqr2	sqr3	sqr4	sqr5	sqr6	xd41	xd59	xd06	xd15	sqr1	sqr2	sqr3	sqr4	sqr5	sqr6	xd41	xd59	xd06	xd15	1	
Frame1(1)	1UP12	1UP15	1UP9	1U17	1U20	1UP18	1UP20	1V18	1VP18	1VP19	1XP12	1XP15	1X3	1X1	1X4	1X6	1X8	1X10	1X14	1X15	0	
Frame2(1)	1UP7	1UP1	1UP2	1UP3	1UP5	1UP4	1UP6	1UP11	1UP9	1UP13	1XP7	1XP1	1XP2	1XP3	1XP5	1XP4	1XP6	1XP11	1XP10	1XP13	0	
Frame3(1)	1VP17	1V17	1V19	1UP19	1UP17	1U18	1UP16	1UP14	1UP10	1UP8	1X13	1X9	1X11	1X7	1X5	1X2	1XP16	1XP14	1XP10	1XP8	0	
Frame4(1)	1U16	1U14	1U8	1U11	1U7	1U4	1U1	1U3	1VP20	1V20	1VP16	1VP14	1VP9	1VP11	1VP7	1VP4	1VP1	1VP3	1X16	1X12	0	
Frame5(1)	1S13	1S14	1S15	1S16	1S12	1S9	1S8	1S6	1S5	1S2	1V3	1V14	1V15	1V16	1V12	1V9	1V6	1V6	1V5	1V2	0	
Frame6(1)	1U10	1U13	1U12	1U16	1S3	1S1	1S4	1S7	1S11	1S10	1VP10	1VP13	1VP12	1VP15	1V3	1V1	1V4	1V7	1V11	1V10	0	
Frame7(1)							1U2	1U5	1U6	1U8							1VP2	1VP5	1VP6	1VP8	1	
Frame 1	xd19	xd37	xd55	xd02	xd20	xd38	xd56	xd65	xd12	xd30	xd19	xd37	xd55	xd02	xd20	xd38	xd56	xd65	xd12	xd30	0	
Frame 2	xd01	xd54	xd27	xd18	xd09	xd00	xd36	xd45	xd63	xd10	xd01	xd54	xd27	xd18	xd09	xd00	xd36	xd45	xd63	xd10	0	
Frame 3	xd57	xd39	xd21	xd03	xd47	xd29	xd11	xd64	xd46	xd28	xd57	xd39	xd21	xd03	xd47	xd29	xd11	xd64	xd46	xd28	0	
Frame 4	xd42	xd24	xd68	xd50	xd32	xd14	xd67	xd49	xd22	xd04	xd42	xd24	xd68	xd50	xd32	xd14	xd67	xd49	xd22	xd04	0	
Frame 5	xd71	xd62	xd53	xd44	xd17	xd70	xd43	xd25	xd07	xd60	xd71	xd62	xd53	xd44	xd17	xd70	xd43	xd25	xd07	xd60	0	
Frame 6	xd33	xd51	xd69	xd16	xd34	xd52	xd61	xd08	xd26	xd35	xd33	xd51	xd69	xd16	xd34	xd52	xd61	xd08	xd26	xd35	0	
Frame 7	sqr1	sqr2	sqr3	sqr4	sqr5	sqr6	xd41	xd59	xd06	xd15	sqr1	sqr2	sqr3	sqr4	sqr5	sqr6	xd41	xd59	xd06	xd15	1	
Frame1(2)	2UP9	2UP6	2U2	2U4	2U1	2UP3	2UP1	2V3	2VP3	2VP2	2XP5	2XP2	2X15	2X16	2X14	2X12	2X10	2X8	2X4	2X3	0	
Frame2(2)	2UP14	2UP20	2UP19	2UP18	2UP16	2UP17	2UP16	2UP10	2UP12	2UP8	2XP10	2XP1	2XP16	2XP14	2XP12	2XP13	2XP11	2XP6	2XP8	2XP4	0	
Frame3(2)	2VP4	2V4	2V2	2UP2	2UP4	2U3	2UP5	2UP7	2UP11	2UP13	2X5	2X9	2X7	2X11	2X13	2XP15	2XP1	2XP3	2XP7	2XP9	0	
Frame4(2)	2U5	2U7	2U12	2U10	2U14	2U17	2U20	2U18	2VP1	2V1	2VP5	2VP7	2VP12	2VP10	2VP14	2VP17	2VP20	2VP18	2X2	2X6	0	
Frame5(2)	2S4	2S3	2S2	2S1	2S5	2S8	2S9	2S11	2S12	2S15	2V6	2V7	2V6	2V5	2V9	2V12	2V13	2V15	2V16	2V19	0	
Frame6(2)	2U11	2U8	2U8	2U6	2S14	2S16	2S13	2S10	2S6	2S7	2VP11	2VP8	2VP9	2VP6	2V18	2V20	2VP7	2VP14	2V10	2V11	0	
Frame7(2)							2U19	2U16	2U15	2U13							2VP19	2VP16	2VP15	2VP13	1	

Figure 5 L1 Output. FPD-TM

3.2 Output

This protocol is still under development. It consists basically of the new terms that are required for Trigger purposes. As of, there are only two terms, High T and Low T. The final version likely will consist of four track bits (High ξ , low ξ , High t, Low t) plus some multiplicity bits used to veto on spray from halo or beam-gas interactions.

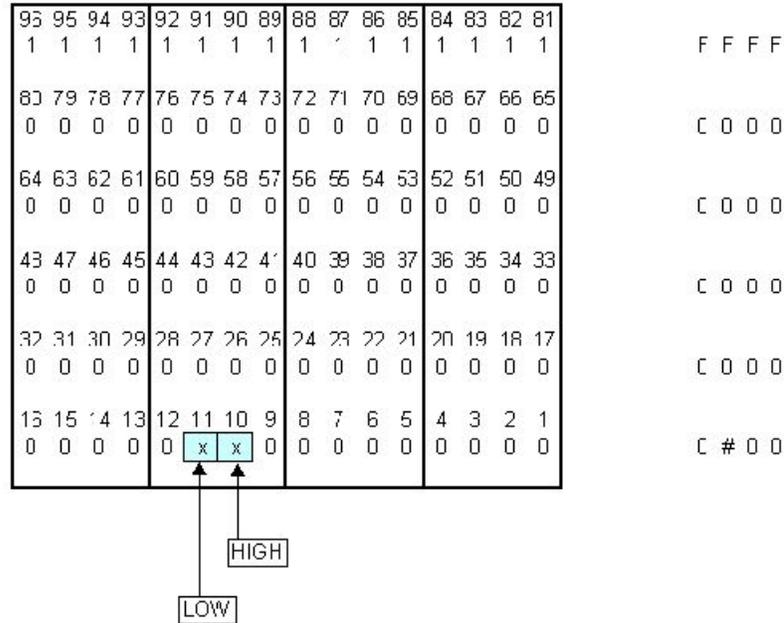


Figure 6 L1FPD output

4 Overview of L1 FPD

4.1 Coding structure

The main idea follows a structure in which there is a “trigger equations” body, generated by Wagner Carvalho⁵ and Mario Vaz⁶.

Attached to it, there are two more components, receiver and sender. The first one takes, stores, and synchronizes the signals (using the link clock) coming in by each LVDS link. It is important to point out that all of the information is stored in Dual RAM memories, and their information is retrieved using a global clock, avoiding the clock domain-overlapping problem.

After it passes the receiver, the information is presented to the body of calculation, which decides if trigger or veto should be send to the output.

As soon as any signal appears from the trigger equations body, it is formatted in a protocol of 96 bits (figure 6).

⁵ Carvalho, Wagner. (2001) Centro Brasileiro de Pesquisas Físicas Retrieved July 10, 2003 <<http://alpha1.lafex.cbpf.br/~wagner/l1equations.html>>

⁶ Vaz, Mario (2001). Centro Brasileiro de Pesquisas Físicas Retrieved July 10, 2003 <<http://d0br1.lafex.cbpf.br/~mario/FPD/FPDTL1.htm>>

Figure 7 shows the scheme described above.

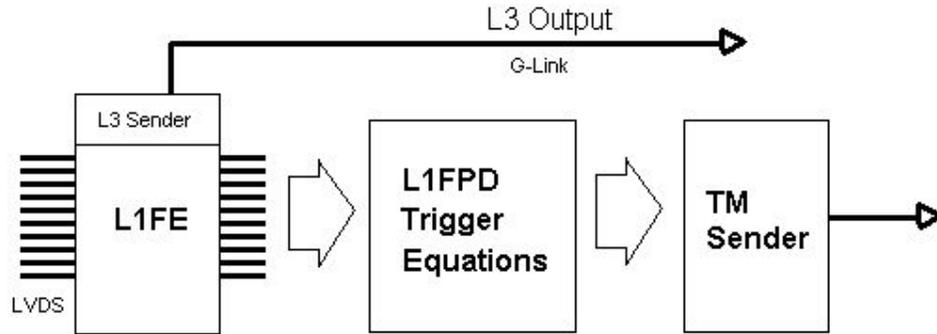


Figure 7 General Description of the firmware implementation

4.1.1 Basic Module

In order to use a pipelined structure based in a simple module, a couple of extra signals have been defined.

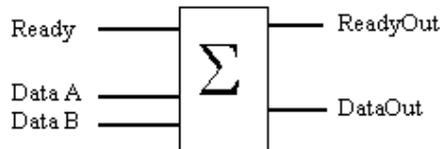


Figure 8 Basic Modules

This module uses a simple ready signal like a synchronization key. This signal comes from the L1FE module [6], and it is named EoR (End of Record). This kind of distribution provides an excellent use of the logical resources.

4.2 General Functional Structure

4.2.1 Receiver

This module has been designed according to get all of the inputs coming from LVDS links. They are only 2 for the device that contains the dipole equations, but it can change (2, 3 and 4) according to the number of detectors attached to it.

This module finds the "Beginning of Record (BOR)". The BOR signs had been generated in the very first frame (output of DFEA). However, since this design takes the information directly from AFE, we must use the last bit of each frame in order to determine which is the last one.

4.2.2 Body of Calculations

It does the information required for the next level of trigger. This part is divided in small modules that take the information arriving in buses of data.

4.2.2.1 Blocks arrangement

After the code has been generated, it is presented in a simple file. It requires to be split in small blocks, which will proportionate a better performance in terms of compiler results.

The following is just an example of the blocks arrangement for generating “dipole trigger” terms.

This configuration does not use *Fine Segments* to generate the output. This feature makes that the implementation can be easily in any FPGA or FPD DFE.

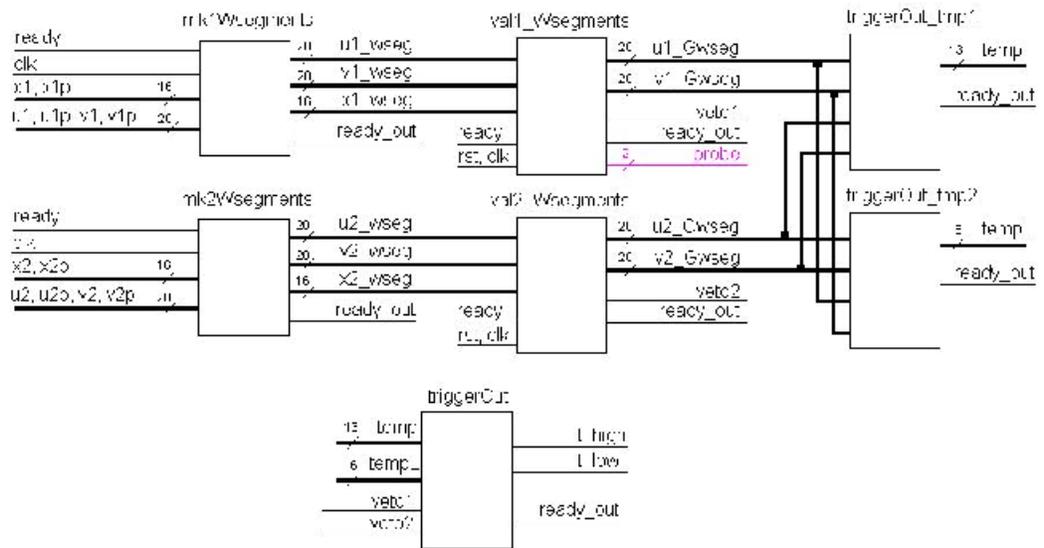


Figure 9 Block arrangement

4.2.3 Senders

4.2.3.1 Level 1

This module is going to be used only for testing purposes. It can be used with the Data-pattern generator (data-pump) in order to check if the information processed in the firmware design behaves according to the predicted outputs.

4.2.3.2 Level 3

This module is in charge to send the information properly formatted to the TM using FSCL paths. This module has been taken from CTTT firmware design.

5 L1 FPD Package Location and Organization

5.1 Packages

The VHD code requires three packages. They are, 'L1FEpack', 'L3pack', and 'FPD_pack'. The two firsts are used by L1FE in order to infer the basic features for the generic values in its code.

5.2 Folders

The basic required organization for implementation requests for implementation requests is as appears in the below figure. Note that the folders with the macros scripts (batch), and the source code (src) have a specific structure, which must be respected in order to use the macro resources. All of the folders must be on place without exception. It is important to point out that the packages files for L1FE and FPD must in the folder 'src' directly.

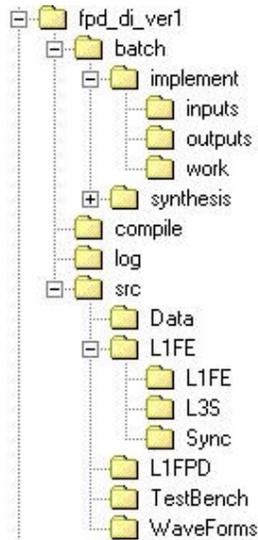


Figure 10 Folders arrangement

In order to do coding and the corresponding simulations, this structure requires to add some new folders, which will contain the VHDL Test Bench [\[14\]](#) and the Test Vectors Data.

6 L1 FPD VHDL Components

The below figure shows the general idea of the coding, so it is possible to differentiate three clear stages arranged according to their functionality. The module at the input called Level 1 Front End (L1FE) is basically a sophisticated receiver; the body of calculations contains the main entities for calculations.

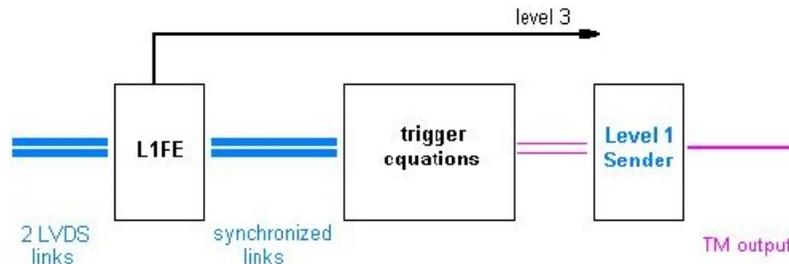


Figure 11 Basic structures

6.1 L1FE

This module [6] has three specific tasks

- Synchronization and de-skew
- Level 3 Sender
- End of Record marker

It takes 2 LVDS inputs; this value is a constant, which can be changed according to the user requirements, and its instantiation must be made in the top-level entity, in this case 'L1FPD.vhd'. The L1FE also contains a powerful Level 3 Sender that can fix the length and the depth into the FIFO (First Input – First Output) arrangement of data for specific study objective. In the L1FPD case, these values are set by default, so the length to the bus is fixed as the copy of 2 links coming from AFE, plus header, trailer and padding frames. Also, the depth for the FIFO is fixed to three events before 'L1 Accept' signal appears.

6.2 Body of calculations

The following description corresponds to the trigger equations implementation for Dipoles without *Fine Segment* definition.

6.2.1 L1FPD.vhd

This module is the top level. It contains the instantiations for all of the main modules, and their connections to each other, using signals.

6.2.2 L1CTOC_EoR.vhd

This module is in charged of stretching the 'EoR' signal generated by 'L1FE'. L1CTOC and its pipelined conception require having a signal a least 6 ticks long while L1FE produces a signal one tick long.

6.2.3 Mk1_Wsegments.vhd & Mk2_Wsegments.vhd

This file generates the wide segments values for the inputs coming from L1FE (receiver). It has been implemented for detector 1 and detector 2 respectively.

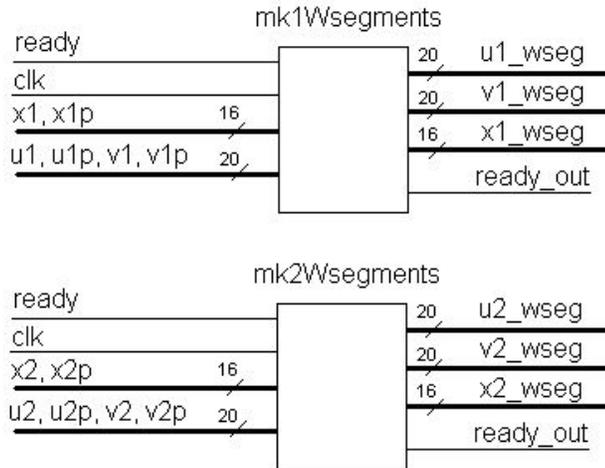


Figure 12 Wide segments

6.2.4 Val1_Wsegments.vhd & Val2_Wsegments.vhd

This module takes the information of the wide segments and validates them using X plane.

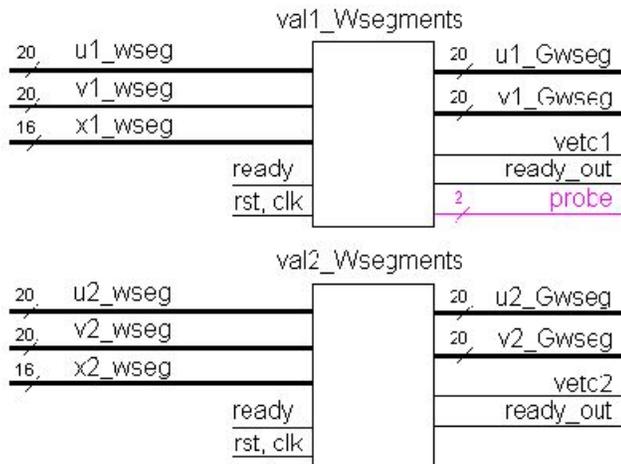


Figure 13 Validate Segments

Also, these modules generate the veto signal, which will be propagated to the Trigger Manager output.

The module that obtains the validated segments for detector 1 has an output of two wires, which has been wire up to the FPGA pin output (firmware definition) in order to have those signals available for scope studies outside of the device.

6.2.5 TriggerOut_tmp1.vhd & TriggerOut_tmp2.vhd

These modules determine if the validated segments can produce a trigger output.

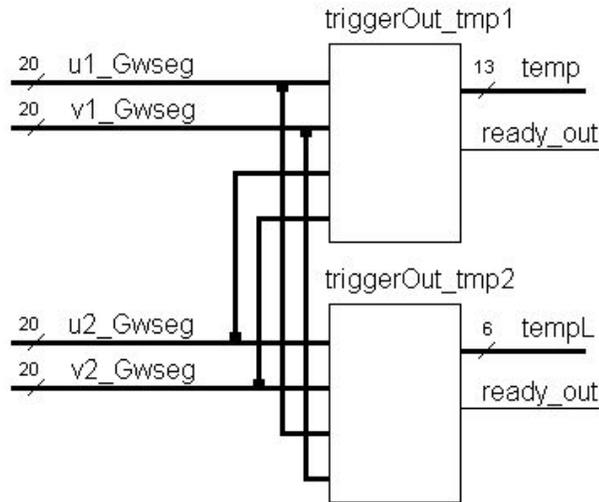


Figure 14 Trigger Out - Temporal signal

It is important to point out the difference in the output bus size between both modules. The first one has a 13 bit wide bus, and the other one presents a 6 bit wide bus to the next level.

6.2.6 TriggerOut.vhd

This module takes the information from the validation process and combines it with veto signals.

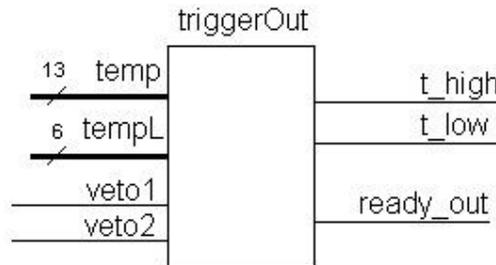


Figure 15 Trigger Output to TM

The result of this task must be passed to Trigger Manager after proper formatting.

6.3 L1 Sender

This module generates the vertical parity and formats the information according to the protocols in order to send it to the next stage CTTT.

It is a simple Finite State Machine, which does not use reset, so it has "software reset".

7 Configuration Parameters

The main values to be affected are in 'L1FE_pack', which correspond to the Number of links coming from DFEA, Number of links to be sent to Level 3, Number of Frames of each input, and the depth into the FIFO for Level 3 effects. However, this changes must be done in the top-level entity instantiation of the module.

At the L1FPD side, there is a value that must be configured in order to get eight different flavours of L1FPD. This value is in 'FPD_pack', and it can go from "000" to "111" (binary notation).

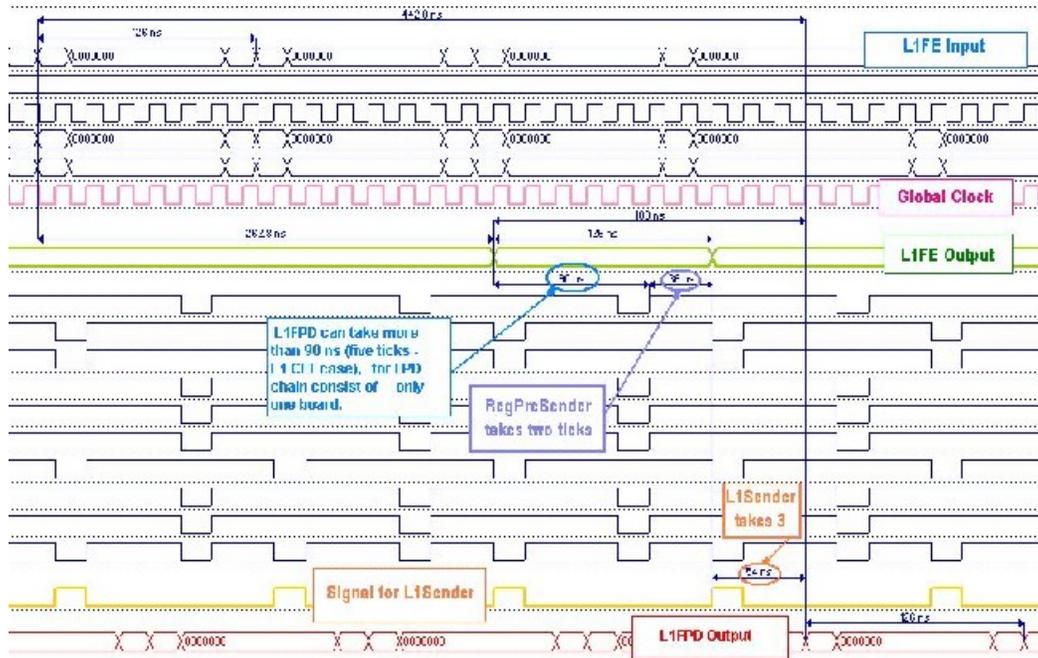
8 Scripts

This tool, wrote by Levan Babukhadia, allows more flexibility and precision in order to choose the synthesis and implementation requirements.

These scripts depends of the location of the files, so the user most change the path in which the files are for 'implement.bat' and 'synthesis.bat'. Also the same path must be placed in the file 'L1FPD.fes', which calls the files requires for synthesis and describes some of the requirements in such process.

9 Timing Simulations

9.1 Latency



9.2 Body of calculations latency

This calculation does not take account of L1FE.

10 1553 interaction

These features have been not implemented yet. No board has been placed into Collision Hall.

The communication is made by 1553 protocol of communication, which talks directly to the controller board (DFEC) [12] in DFE crate. Most of the information is propagated using interface software denominated DFEWare [13], which offers interactivity with the boards placed in such crate for d0online users.

The designs are downloaded using this interface. They must be in a proper format, so it must be generated by Xilinx PROM file formatter, which generated a *.HEX file.

Once the process makes the file, it must be agree with the following naming conventions.

FPD1_PW03_x_x_D0_v000.005

Board name Crate Slot Device Version

Figure 16 DFEWare convention

The above example is placing a file with Version “005”, into device D0, crate number ‘PW3x’, for FPD board. When the device is going to be used, it must use a blank generated file, which prevents signals hanging around.

11 Outlook

The L1FPD has been successfully tested for Fake tracks, A and A+B events. Also, its L3 Sender has been read over FIC [10] into L2 crate [11].

Some functions require be studied for implementation, and depth studies at the online and offline level are strongly recommended.

Also, the characterization of ‘L1 Accept’ signals arriving to design and different values of Firmware Revision Register for test mode must be tested.

12 Glossary

Table 1 Generic Board Names [\[15\]](#)

Term	Meaning
DFEA	Digital Front End – Analog
SWDB	Single Wide Double Board
MB	Motherboard
FPD	Central Tracker Octant Card
DWDB	Double Wide Daughter Board
AFE	Analog Front End
FIC	Fiber Input Converter Card
SCL	Serial Command Link
CTTT	Central Tracking Trigger System
DFEC	Digital Front End Controller

Table 2 Communications Protocols

Term	Meaning
LVDS	Low Voltage Differential Signalling
G-Link	HP G-link - Fiber optic based fast link
1553	Mil-Std-1553
FSCl	Fast Serial Copper Link

Table 3 Others

Term	Meaning
CPS	Central Pre-Shower
CFT	Central Fiber Tracker
FPGA	Field Programmable Gate Array
CPLD	Complex Programmable Logic Device
DFEWare	Software for communication via 1553

13 References

- [1] CTTT Group, "CTT technical design report," D0 Note 3551, Jan. 1999.
- [2] Xilinx, Virtex Data Sheet, Feb. 2002.
- [3] J. Olsen, " CFT/CPS sector and singlet naming convention. LVDS bus colors and motherboard input bus structure defined.," Dec. 2001.
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- [5] L. Babukhadia, " DØ Track and Preshower Trigger Level 1 Trigger Terms and Data Transfer Protocols V07-00", Apr. 29, 2002 "
- [6] L. Babukhadia, M. Martin, and S. Desai, "L1FE design (VHDL design)," D0 Note 3881, Jul. 2001.
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- [8] S. Rajan, Essential VHDL - RTL Synthesis Done Right,, pp. 21 - 50, 1998.
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- [16]

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