

### 1 Testing

The first approach is going to be implemented in a Xilinx Virtex 600 BG 560 device, which is provided for the Double Wide Daughter Board (DWDB).

This device is going to provide FPD with two convenient buses for debugging purposes. Two LVDS outputs carry the information coming from the device labeled as U1. Also, at this point, it is important to clarify that the implementation will require the corresponding Constraint File (UCF) for this device.

In the Combined Test Stand (CTS), which is the Central Fiber Tracker (CFT) test stand, it is going to be tested in Stand Alone mode. It requires the Data Pattern Generator Pump (DP) for sending the test vectors.

#### 1.1 DP to DWDB (Loop)

This loop lets to send the Test Vectors, using the LVDS inputs of the Mother Board (MB). It is important to point that the Link 2 is always required in order to obtain the Global Clock for the firmware into the Daughter Board.

This test is going to give important clues about the proper work of the trigger equations. However, this is not a real test because our board is not going to have “Level 1 – Level 2” indicator, but for the first try, the test vectors can have this information only for doing the trigger at the output of the board (input to DP).

#### 1.2 AFE, DWDB, and DP

This test involves the use of the AFE personality code, which until this moment is not determined.

### 2 VHDL Code

The implementation requires to use a signal “Beginning of Record” coming from the Level 1 Front End (L1FE). However, this signal is not available from AFE, so this module will require to be updated in order to agree with the input coming from AFE.

Also, the Sender drives L1CFT format, which needs to be updated to the proper format for Trigger Manager (TM).