

NOTE 3627

March 4, 1999

# NOTES ABOUT THE CFT DIGITAL BOARD AND ITS USES

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THE POSSIBILITY OF USING THE  
DIGITAL BOARD  
AS THE BASIS FOR THE DESIGN OF THE  
BROADCASTER  
AND THE SUBSTITUTION OF THE  
SERIAL COPPER LINK  
BY A  
LVDS LINK

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Tempus fugit

#### NOTE

The work presented here is the result of frequent conversations with members of the DØ Trigger Team. I must mentioned specifically A. Lucotte, Jameison Olsen and D. Toback,

## Introduction

It was known for long time that the Front End Boards containing analog and digital electronics for the CFT were to dense and dissipated a great deal of heat. This heat was very difficult to extract from the "crate" where the boards were located. A solution to the problem was to separate the analog and the digital parts. This solution was suggested by several people<sup>[1]</sup> and accepted by the group as a viable alternative to the original design. In the past week, Jameison Olsen and John Anderson suggested to use the new Digital Front End Board as the basis for the design of the Broadcaster Board. This DØ Note investigates the implications of such a design change.

If the DFE Board design is used in the Broadcaster, *why not used the same general design to implement the L1 Trigger Manager used by the CFT/CPS Axial and the FPS?* I propose that we do just that, and this DØ Note will present the pros and cons of such approach.

## The Digital Front end board

### First Approach

The original design of the Digital Front End Board (DFE) as presented by Jameison served two Analog Front End Boards (AFE). A conceptual block diagram of the DFE and the two AFE, which it serves, is shown in Fig. 1.

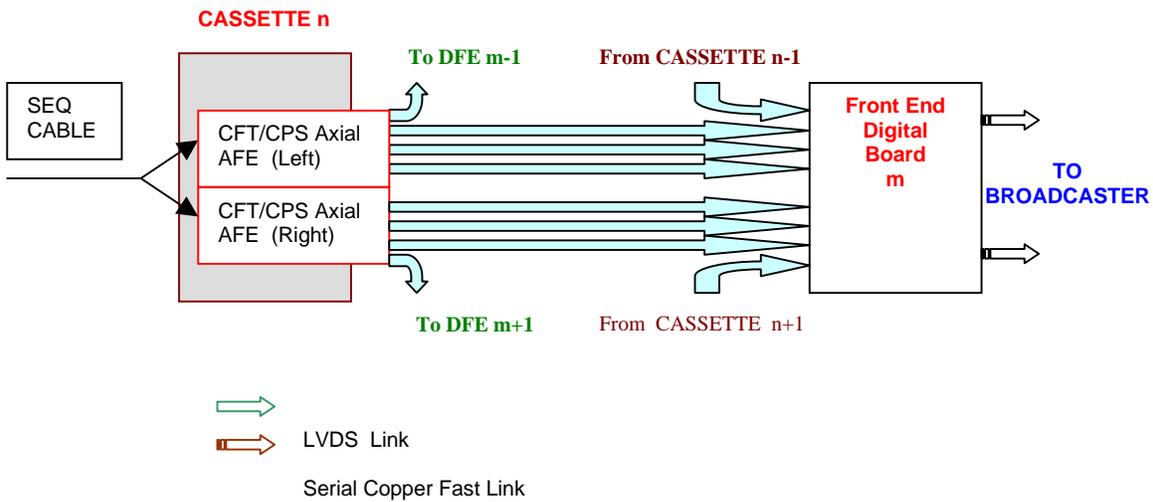
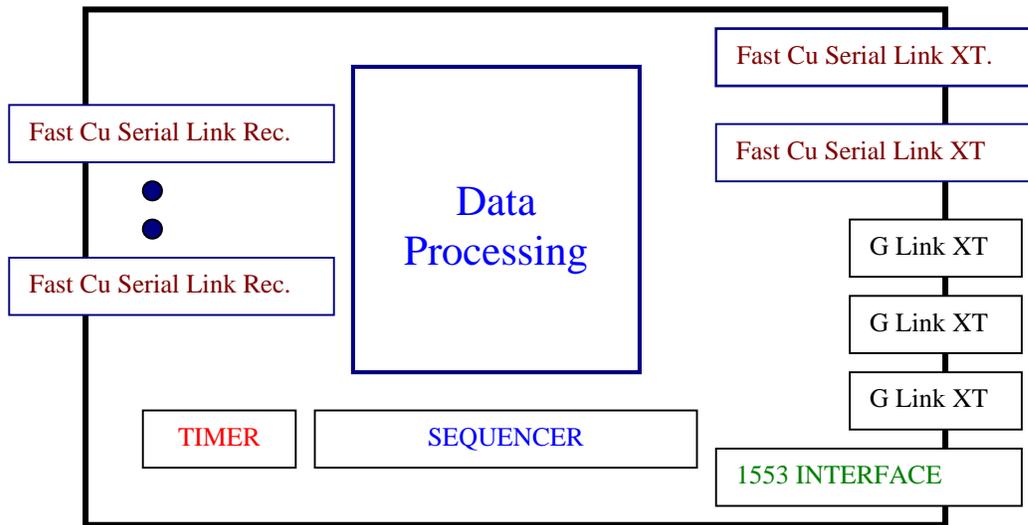


Fig. 1 Block diagram of the Front End electronics broken into separated PC Boards: one set to handle the analog signals and their conversion to digital and one set dedicated to digital signal processing.

## Using the DFE board as a broadcaster board

A functional block diagram of the Broadcaster was presented in the January Design Review. At that time, the possibility of utilizing the Digital Front End Board for its implementation was not yet considered. This Functional Block Diagram is presented in Fig. 2.



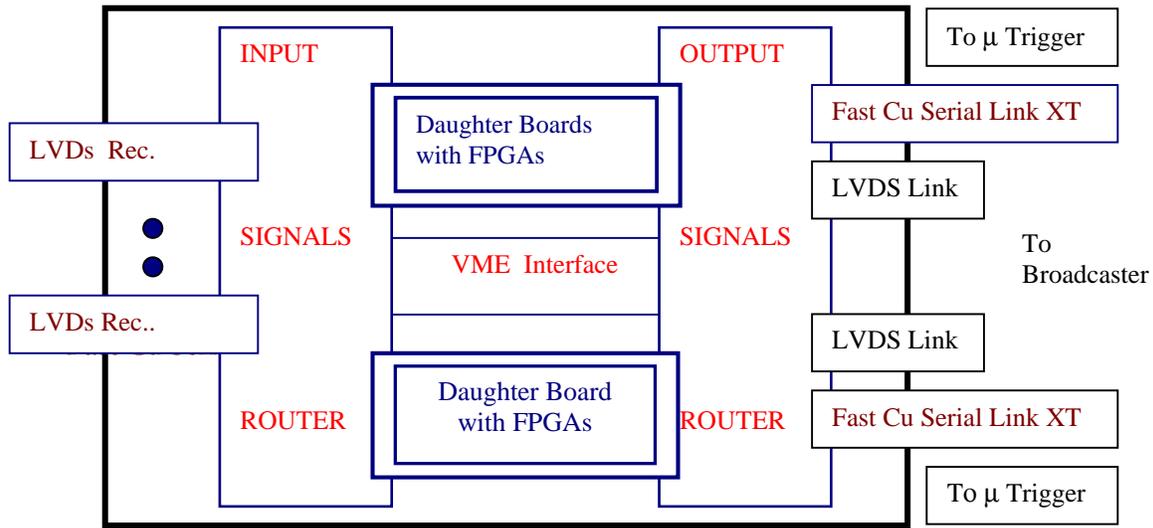
**FIG. 2.** Functional Block Diagram of the Broadcaster

The mayor difficulties in the implementation of this board was the great amount of area required by the I/O channels. The most demanding case is this of the Broadcaster serving the L1CFT and the L2CFTpp and L2CPS Axial. For this case the I/O channels are as follows:

- 10 Fast Copper Serial Links     Inputs from FE
- 2 Fast Copper Serial Link     Output to L1Trigger Manager (two are needed to provide the Pt sign information)
- 2 G Links Transmitters     Output to L2 FICs
- 1G Link Transmitter     Output to L3
- 1 1553 Interface     Back Plane Connection

The logic represented by the Functional Blocks “Data Processing”, “Sequencer” and “Timer” are implemented using high end FPGAs.

To follow Jameison Olsen and John Anderson suggestions the first thing needed was to make a comparison of the two designs. To this end I made a revision of the Broadcaster needs and of the possibilities of the original design of the Digital Front End Board as shown by Jameison. A Functional Block Diagram of this design is shown in Fig. 3.



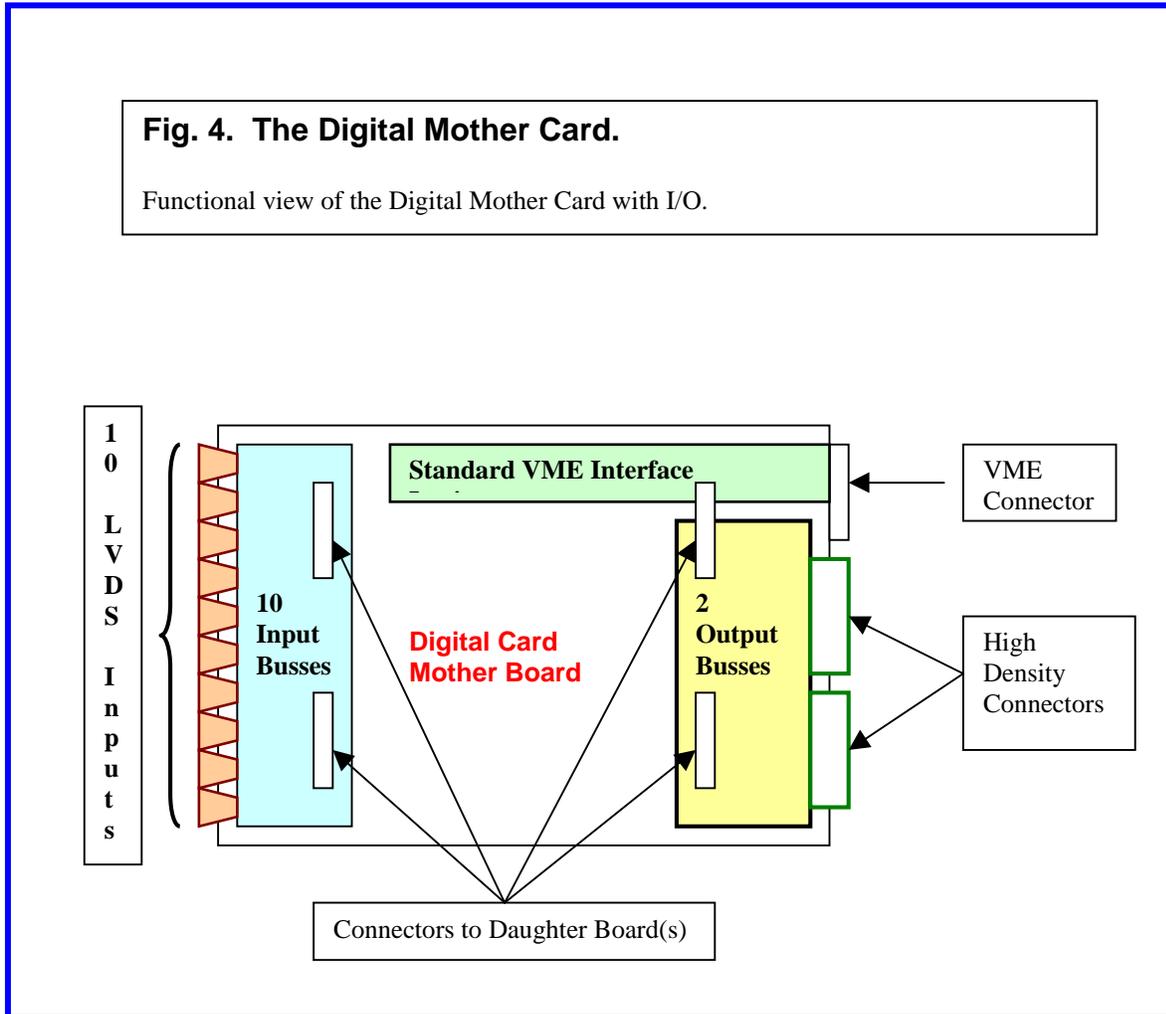
**Fig. 3.** Functional Block Diagram of the Original Digital Front End Board.

The design of these boards calls for two Daughter Boards to implement function specific logic while the common logic is implemented directly in the board. In the case of the Digital Front End Boards for the CFT/CPS Axial, each Daughter Board implements the Track Finding, Pt Sorting and Cluster Finding/Track Matching algorithms originally implemented in the digital portion of the FE Board. The breaking of the bulk of the logic into two separated Daughter Boards working in parallel is a logical result of the fact that one DFEB serves two adjacent Analog FE Boards as shown on Fig. 1.

Comparing Figures 2 and Fig. 3 it appears that there are enough similarities between them to suggest implementing the Broadcaster with a Digital Front End Board. The differences in algorithms being taken up by different firmware in the Daughter Boards and the 1553 interface substituted by a VME interface.. This is the suggestion made by Jameison Olsen and John Anderson. However, these changes are not sufficient; to make a Broadcaster Board from a Digital Front End Board it is necessary to make changes in the I/O of the board to satisfy the needs of the Broadcaster. First, it is needed to increase the number of input LVDS links from eight to ten. This possible and relatively simple. Unfortunately, to increase the number of output links from two Fast Copper Serial Links and two LVDS Links to two Fast Copper Links and three G Links is not possible.

To be able to use the Digital Front End Board as a Broadcaster Board it is necessary to review the total System Architecture of the CFT Trigger. Only a new Top-Down design could take full advantage of the possibilities opened by the Digital Front End. Furthermore, a new System Architecture design utilizing a variation of the Digital Front End Board as a Broadcaster

will assess the feasibility of such approach. This is the only way to see what type of changes are needed in the original design of the Digital Front End board to extend its original use. After several tries \* an unifying picture emerged. Modifying the Digital Front End board to accommodate 10 LVDS inputs and adding an extension board (the "Distribution Card") for the outputs we can create a truly flexible set of building blocks to implement the CFT Trigger System. The heart of these is a common Digital Mother Card (DMC) whose functional block diagram is shown in Fig. 4

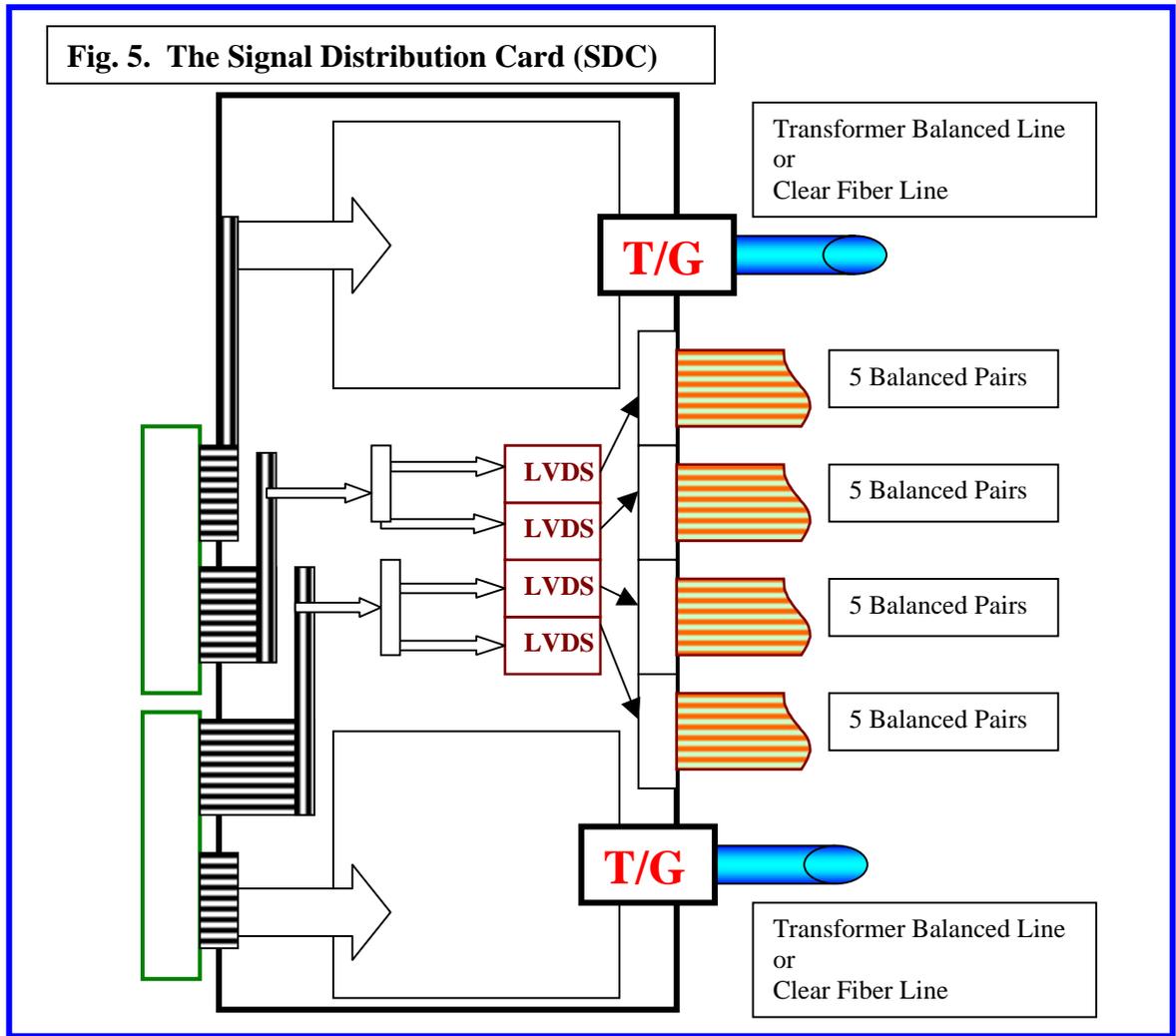


The DMC includes all and only these functions common to the different versions of Digital Cards:

- ❖ Ten (10) LVDS Receivers.
- ❖ An standard J1 connector to the Back Plane of the crate where the DMCs are housed. This serves to connect the Digital Boards to an standard VME card.

\* See DØ Note 3626 and my presentations to the CFT Engineering Review and the SACLAY Workshop.

- ❖ Two High Density connectors protruding beyond the crate's Back Plane used to connect to an special I/O card.
- ❖ Four special connectors to make the transition to the functionally specific Digital Daughter Cards (DDC).
- ❖ The necessary circuitry to route the input signals to the DDC via the special connectors.
- ❖ The necessary circuitry to route the Output signals from the DDCsI to the I/O card.
- ❖ The standard VME interface and required circuitry to program in situ the FPGAs used in the Digital Mother Card and the Digital Daughter Cards.



The Digital Mother Card sends information to the rest of the world via an intermediate card: the Signal Distribution Card (SDC). Its functional block diagram is shown in Fig.5. The Signal Distribution Card has two functionally identical circuits. Each one consists of:

One High Density Connector to bring signals from the Mother Board

- ❖ Two Busses
- ❖ One Transmitter using the XXXXX Protocol. This Transmitter serves either a Clear Fiber Connector (G Link) or a Transformer Balanced Copper Line (Fast Serial Copper Link)
- ❖ Two LVDS Transmitters
- ❖ Two 10 Pin Connectors, each serving a Flat Cable of 5 Balanced Pairs.

The four busses can carry independent signals or the same signals, the choice is made in the Daughter Boards.

It is possible to have only one design serving both the Transformer couple copper link and the clear fiber. In this case the difference between the two flavors of the SDC is minimal and related to the type of driver used. Obviously, one of the two halves of one SDC can be used to transmit signals via a Cu balanced line while the other can be dedicated to G Link type. To distinguish between the different combinations, we will use the following mnemonics:

- SDCC for a Signal Distribution Card with two Fast Serial Copper Links
- SDGG for a Signal Distribution Card with two G Links
- SDCG for a Signal Distribution Card with one Fast Serial Copper Link and one G Link.

## The Minimum Set of Building Blocks

The previous section shows that we have at our disposal some very powerful elementary blocks:

- A common mother card, the DMC
- Three flavors of the Signal Distribution Card
- Two flavors of Daughter Cards: a "Single Channel" daughter card (SCD), and a "Dual Channel" daughter card (DCD).

Using these, we can construct all the special boards that are needed for the CFT Trigger System. As I will show in the next section, the boards needed are:

- The Digital Front End Card (DFE), built with:
  - ❖ One Digital Mother Card (DMC)
  - ❖ Two Single Channel Daughter cards (SCD)

- ❖ One Signal distribution card with two Fast Serial Copper Links (SDCC)
- A Type 1 Broadcaster (B1GG) , built with:
  - ❖ One Digital Mother Card (DMC)
  - ❖ One Dual Channel Daughter card (DCD)
  - ❖ One Signal distribution card with two G Links (SDGG)
- A Type 2 Broadcaster (B2CG), built with:
  - ❖ One Digital Mother Card (DMC)
  - ❖ One Dual Channel Daughter card (DCD)
  - ❖ One Signal distribution card with one G Link and one Fast Serial Copper Link (SDGG)
- A Type 3 Broadcaster (B3GG), built with:
  - ❖ One Digital Mother Card (DMC)
  - ❖ Two Single Channel Daughter cards (SCD)
  - ❖ One Signal distribution card with two G Links (SDGG)

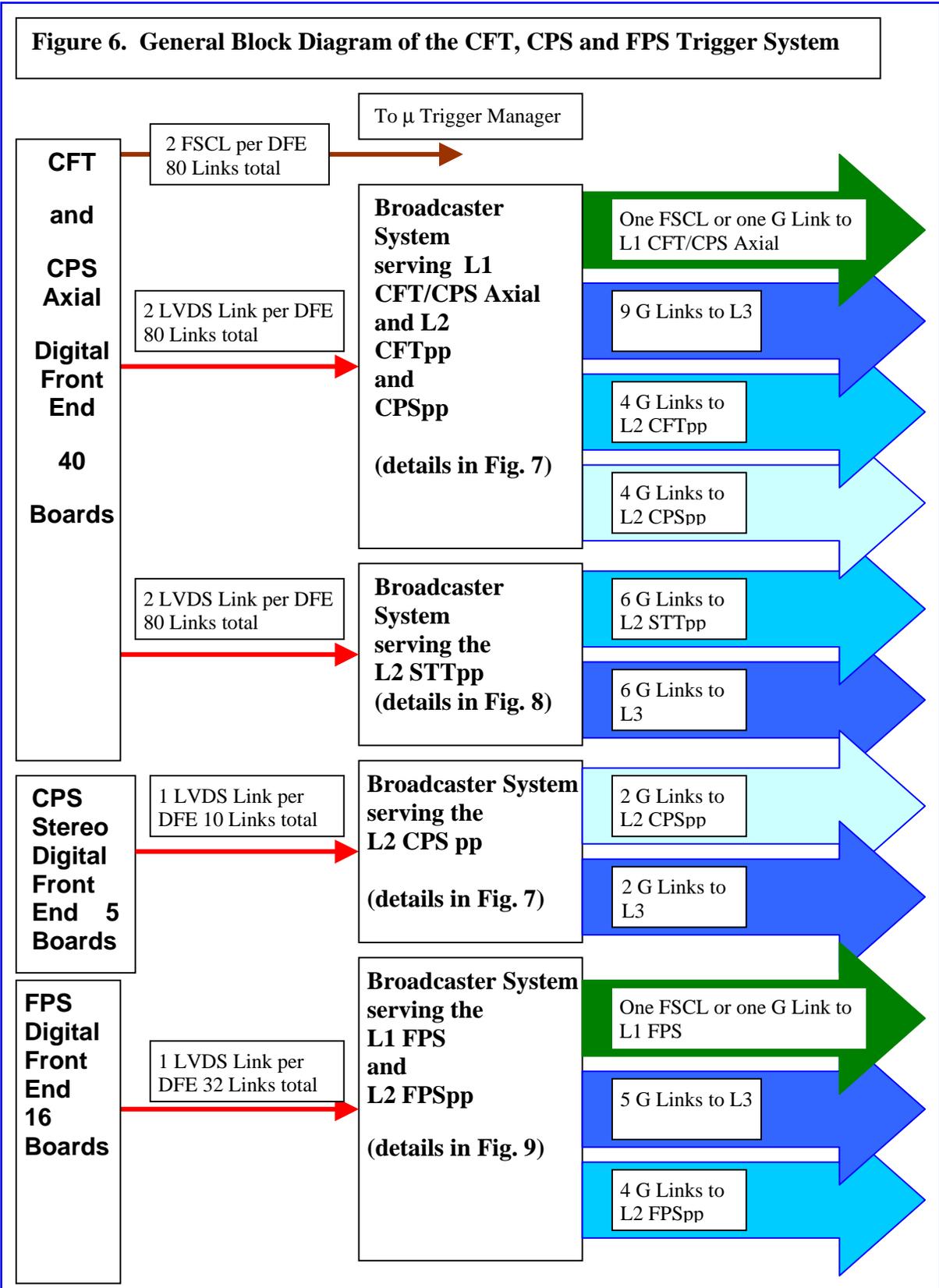
### **The System Architecture using the minimum set of Building Blocks**

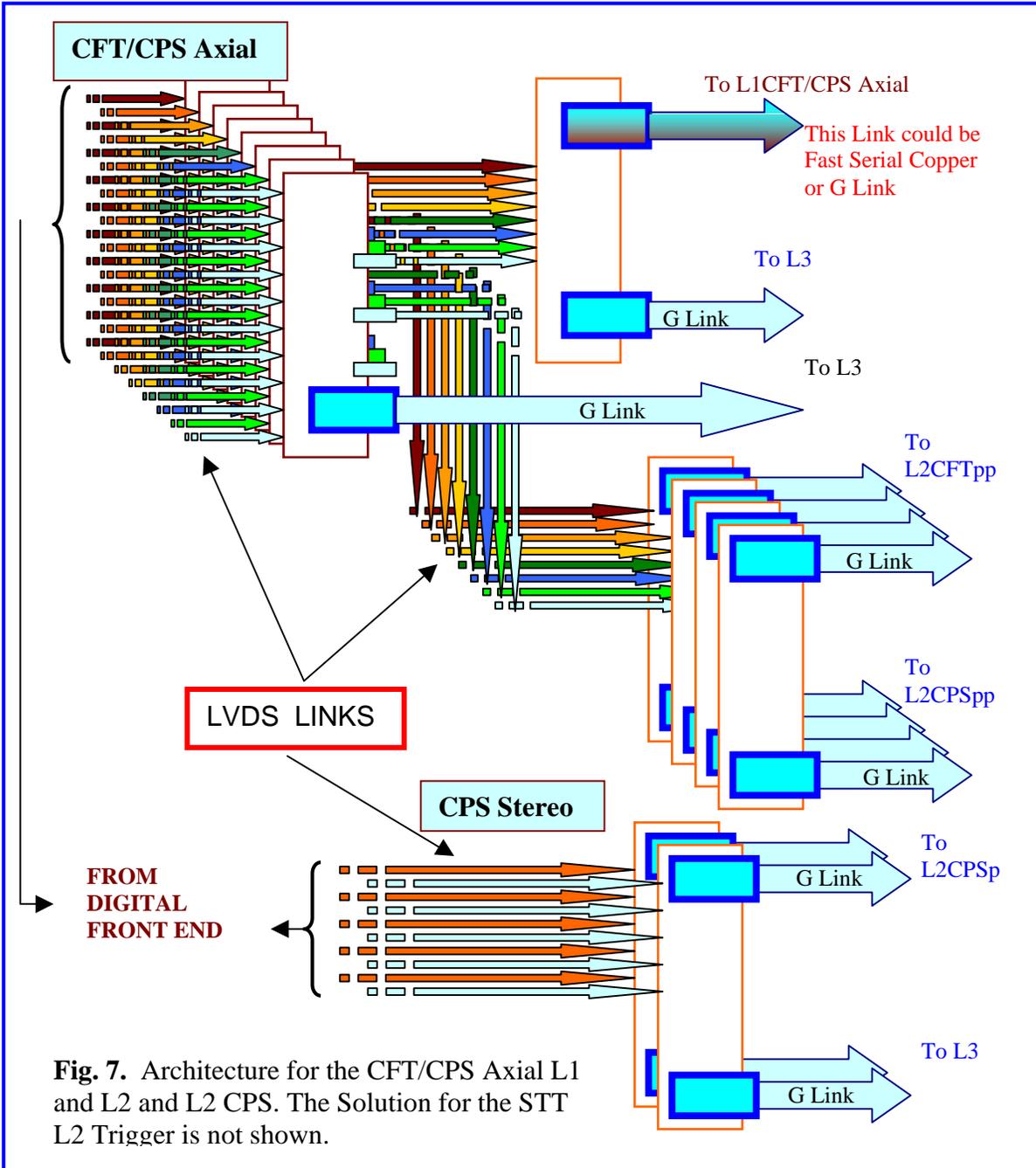
The new System Architecture takes advantage of the minimum set of building blocks integrated into the four types of boards described in the previous section. The architecture is extremely simple and yet very powerful, as we will show. It uses the fact that the information generated by a:

- Single Channel Daughter card is available simultaneously at three outputs: two LVDS links and one G Link or one Fast Serial Copper Link
- Dual Channel Daughter can be available simultaneously at six outputs: four LVDS links and at a dual set of G Links and/or Fast Serial Copper Links

These arrangements make possible to find independent solutions for the hardware architecture serving the CFTpp and the STTpp which have completely different geometry. One of the LVDS links from a half Digital Front End is used to serve the CFT/CPS Axial triggers while the other LVDS can serve the STTpp system. A general block diagram of the envisioned architecture is shown in Fig.6. The general diagram is followed by more detailed block diagrams for the major components.

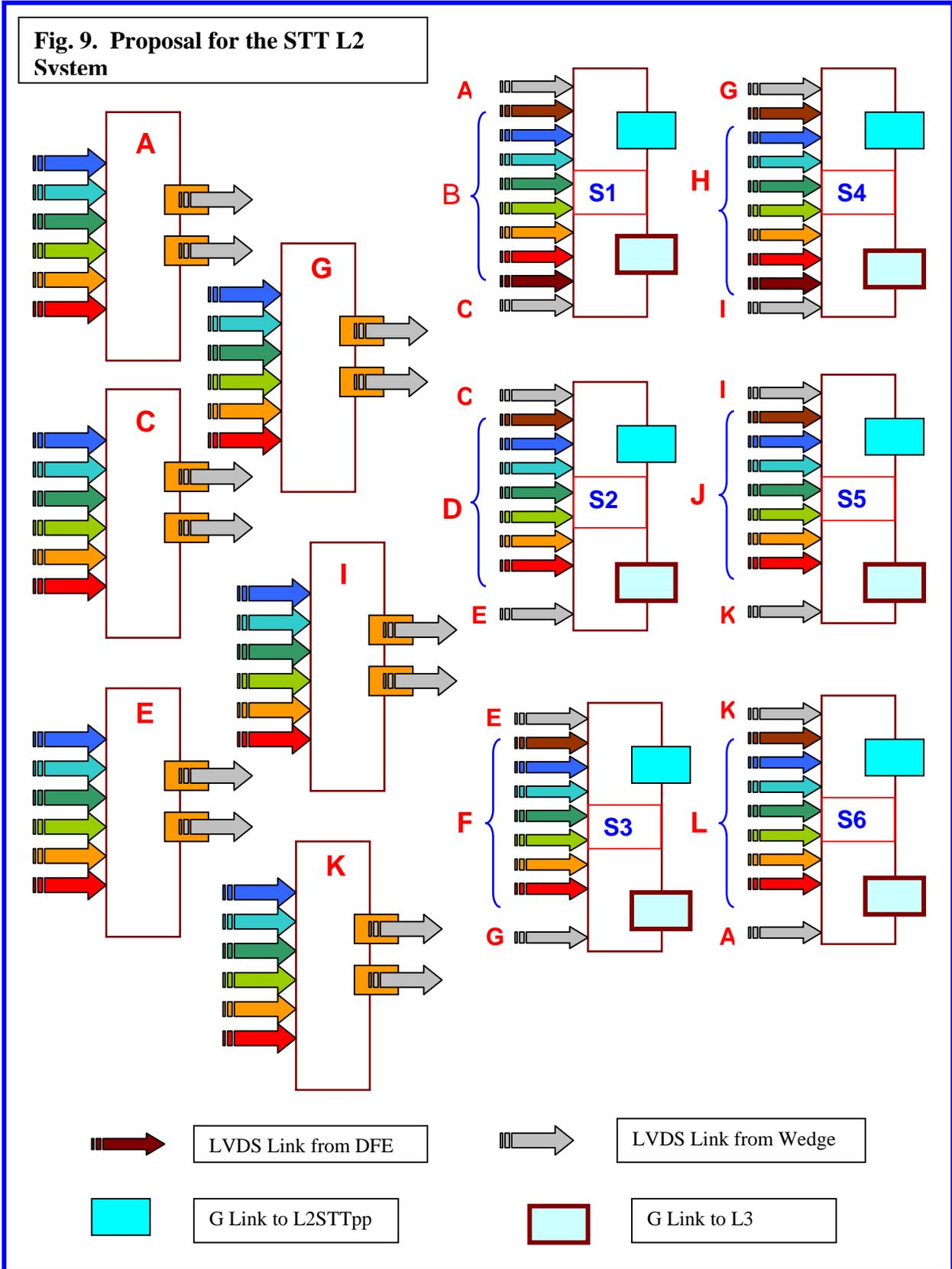
Of all the subsystems, the Broadcaster system serving the central portion of the detector is the most complex. It deals with L1 CFT/CPS Axial, L2 CFT, L2 CPS and L2 STT. Because the L2 STT Trigger is not completely defined at this time, two detailed block diagrams are generated. The first deals with the CFT and CPS and it is shown in Fig. 7 , the second shows a possible solution for the STTpp in Fig. 9.





**Fig. 7.** Architecture for the CFT/CPS Axial L1 and L2 and L2 CPS. The Solution for the STT L2 Trigger is not shown.





## Conclusions

The present DØ Note shows how a complete Front End/Broadcaster System can be built using Jameison Olsen design of the Digital Front End board with some modifications. The architecture here presented for the CFT, CPS and FPS uses the following hardware:

- ❖ **DFE for CFT/CPS Axial.**- 40 Digital Front End boards (dual daughter cards) with 3 (4)<sup>^</sup> LVDS Links and 2 (2) Fast Serial Copper Link
- ❖ **DFE for CPS Stereo.**- 10 Digital Front End boards (single or dual daughter cards) with 2 (4) LVDS Links and 0 (2) Fast Serial Copper Link
- ❖ **DFE for FPS .-** 32 Digital Front End boards (single or dual daughter cards) with 2 (4) LVDS Links and 0 (2) Fast Serial Copper Link
- ❖ 8 Digital Broadcasters Type 1 or Type 3 with 2 (4) LVDS Links and 1 (2) G Links
- ❖ 6 Digital Broadcasters Type 1 or Type 3 with 1 (4) LVDS Links and 2 (2) G Links
- ❖ 2 Digital Broadcaster Type 2 with 1 (1) G Link and 1 (1) Fast Serial Copper Link (Trigger Manager on the Platform)

**OR\***

- ❖ 2 Digital Broadcaster Type 3 with 2 (2) G Links (Trigger Manager on the Moving Counting House)

for a total of **82** Digital Boards, **346** LVDS Links and either a combination of **82** Fast Serial Copper Links and **22** G Links or **80** Fast Serial Copper Links and **20** G Links.

If the solution presented here for the STTpp is adopted, we must add

- ❖ 6 Digital Broadcasters Type 1 or Type 3 with 2 (4) LVDS Links and 0 (2) G Links
- ❖ 6 Digital Broadcasters Type 1 or Type 3 with 0 (4) LVDS Links and 2 (2) G Links

for a total of **94** Digital Boards **358** LVDS Links and either a combination of **82** Fast Serial Copper Links and **34** G Links or **80** Fast Serial Copper Links and **32** G Links.

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<sup>^</sup> Numbers in parenthesis shown the maximum possible for this type of card. Numbers in front of the parenthesis are the actually used for the system.

\* If the L1 CPS requires a quadrant match with the Calorimeter timing constraints make it necessary to locate the L1 Trigger Manager for the CFT/CPS Axial on the Moving Counting House.