DØ NOTE 3626

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NEW HARDWARE, NEW PROTOCOLS!

THE POSSIBILITY OF USING THE DIGITAL BOARD AS THE BASIS FOR THE DESIGN OF THE BROADCASTER AND THE SUBSTITUTION OF THE SERIAL COPPER LINK BY A LVDS LINK REQUIRES NEW PROTOCOLS TO COMMUNICATED BETWEEN THE DIGITAL BOARDS AND THE BROADCASTER

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Tempus fugit

Introduction

It was known for long time that the Front End Boards containing analog and digital electronics for the CFT were to dense and dissipated a great deal of heat. This heat was very difficult to extract from the "crate" where the boards were located. A solution to the problem was to separate the analog and the digital parts. This solution was suggested by several people [1] and accepted by the group as a viable alternative to the original design. In the past week, Jameison Olsen and John Anderson suggested to use the new Digital Front End Board as the basis for the design of the Broadcaster Board. This DØ Note investigates the implications of such a design change.

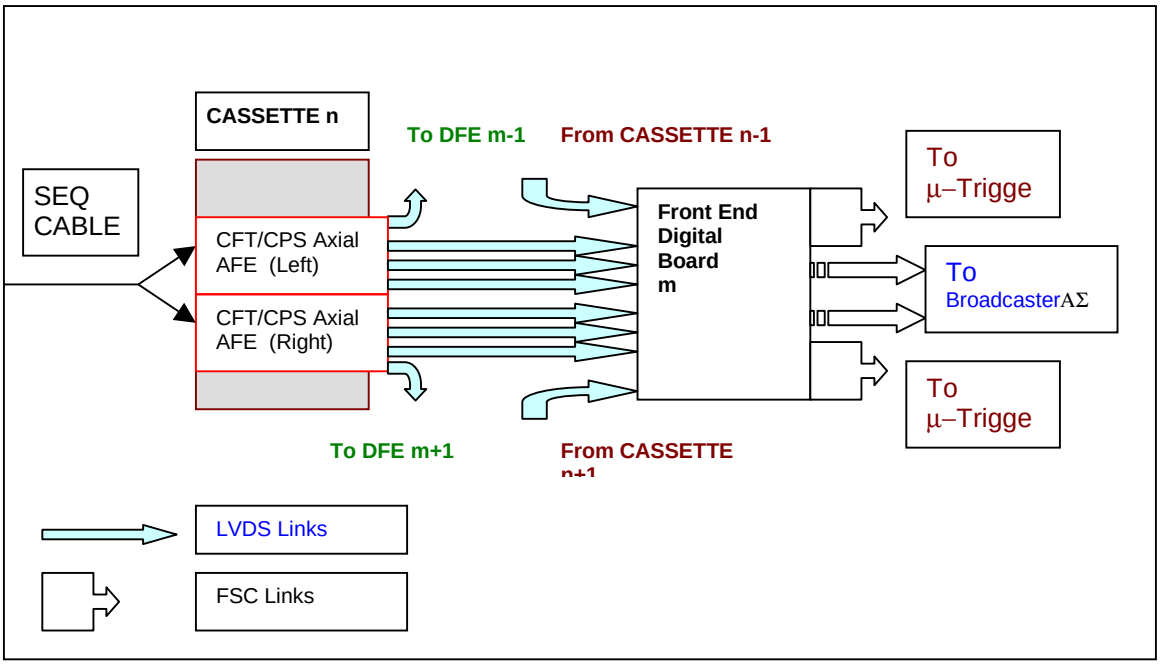
If the DFE Board design is used in the Broadcaster, *why not used the same general design to implement the L1 Trigger Manager used by the CFT/CPS Axial and the FPS?* I propose that we do just that, and this DØ Note will present the pros and cons of such approach.

The Digital Front end board

First Approach

The original design of the Digital Front End Board (DFE) as presented by Jameison served two Analog Front End Boards (AFE). A conceptual block diagram of the DFE and

Figure 1.- Block diagram of the Front End electronics broken into separated PC Boards: one set to handle the analog signals and their conversion to digital and one set dedicated to digital signal processing.



the two AFE, which it serves, is shown in Fig. 1.

In this design the communication with the Broadcaster was achieved via two [2] Serial Copper Fast Links (SCFL) of the same kin as the muon system uses. Allowing for a maximum of ten SCFLs inputs for a Broadcaster, the system architecture for the Trigger System became quite expensive. A block diagram for the CFT/CPS Axial Trigger System is shown in Fig. 2.

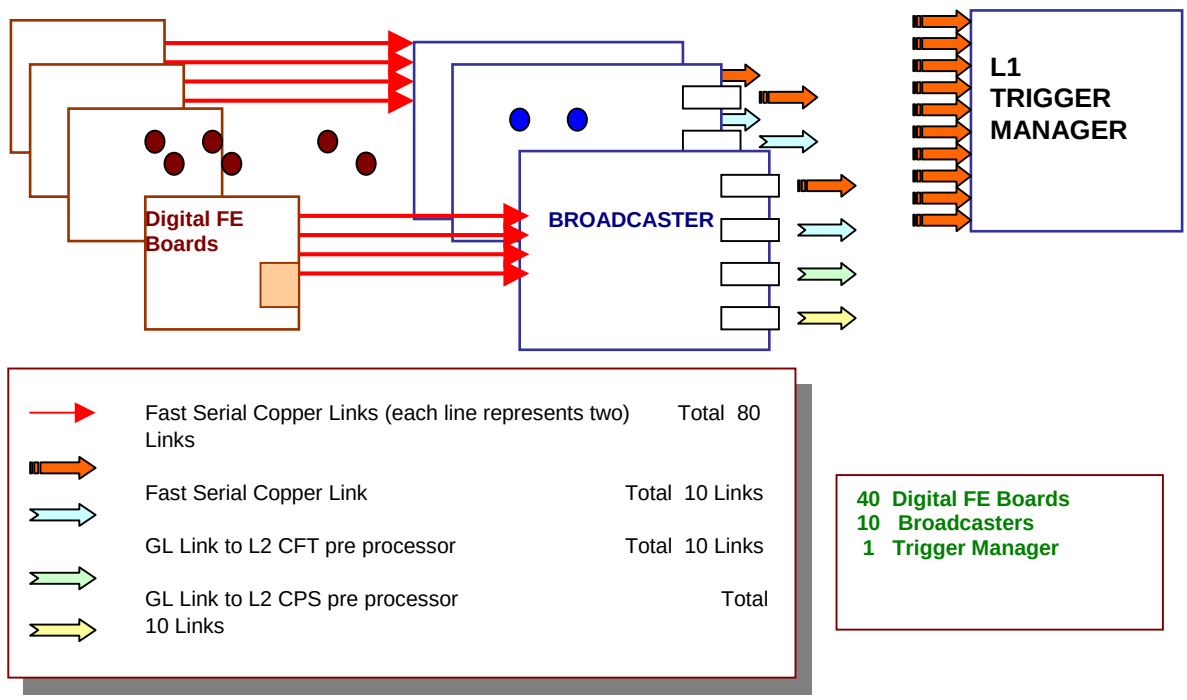


Fig. 2 Block diagram showing the relationships between the Digital Front End Boards and the Broadcaster and L1 Trigger Manager Boards.

Inclusion of the Pt sign: first modification of the DFE Board

After this proposal was made a real disastrous situation was discovered: the communication protocols between the Broadcaster and the L1 CFT/CPS Trigger Manager did not allowed for inclusion of the sign of the Pt! To provide sign information, the bandwidth of the link between the Broadcaster and the L1 CFT/CPS Trigger Manager needs to be double. With the limitations imposed by the Fast Serial Copper Link, this implies to double the number of links between Front End Boards and Broadcaster and between Broadcaster and L1 CFT/CPS Trigger Manager. One link to transfer information concerning tracks with positive Pt and another parallel link to take care of the tracks with

negative Pt. Consequently, the total number of Fast Serial Copper Links went from ninety to one hundred eighty!

In conversations with Jameison it was decided that a minor modification in the Digital Front End Board and in the Broadcaster boards could reduced drastically the amount of links required. By changing the nature of the links between the Digital Front End Board and the Broadcaster from Fast Serial Copper Links to LVDS the number of required links was reduced to the original numbers. With this change the System Architecture is the same as the original shown in Fig. 2, the only that is required is to change the links represented by simple red arrows from Fast Serial Copper Links to LVDS.

New Protocol for transfers between Front End and Broadcaster

Changes in hardware often imply other changes as well. In this instance, the change in the hardware moving information across boards requires a change in the protocol defining these transfers of information. The LVDS is capable of transferring 28 bits of data per clock while the Fast Serial Copper Link is able to transfer only 16 data bits in the same clock, this is a possible increase of bandwidth of 175%. Keep in mind that in some cases the same physical link is used to send L1 and L2 from the Digital Front End Boards to the Broadcaster. Thus, both protocols are affected.

The proposed protocol to use for transfers between the Digital Front End Boards and the Broadcaster Boards is shown on Fig. 3. Data transfer is implemented using frames of 28 bits each divided into 24 bits of data and 4 control bits.

The meaning of the four control bits is as follows:

B24 (PAR)	Odd parity of the first 24 bits of the frame
B25 (S)	1 to mark the first frame of a record, 0 otherwise
B26 (E)	1 to mark the last frame of a record, 0 otherwise
B27 (D)	1 to mark frames with event data, 0 for test data

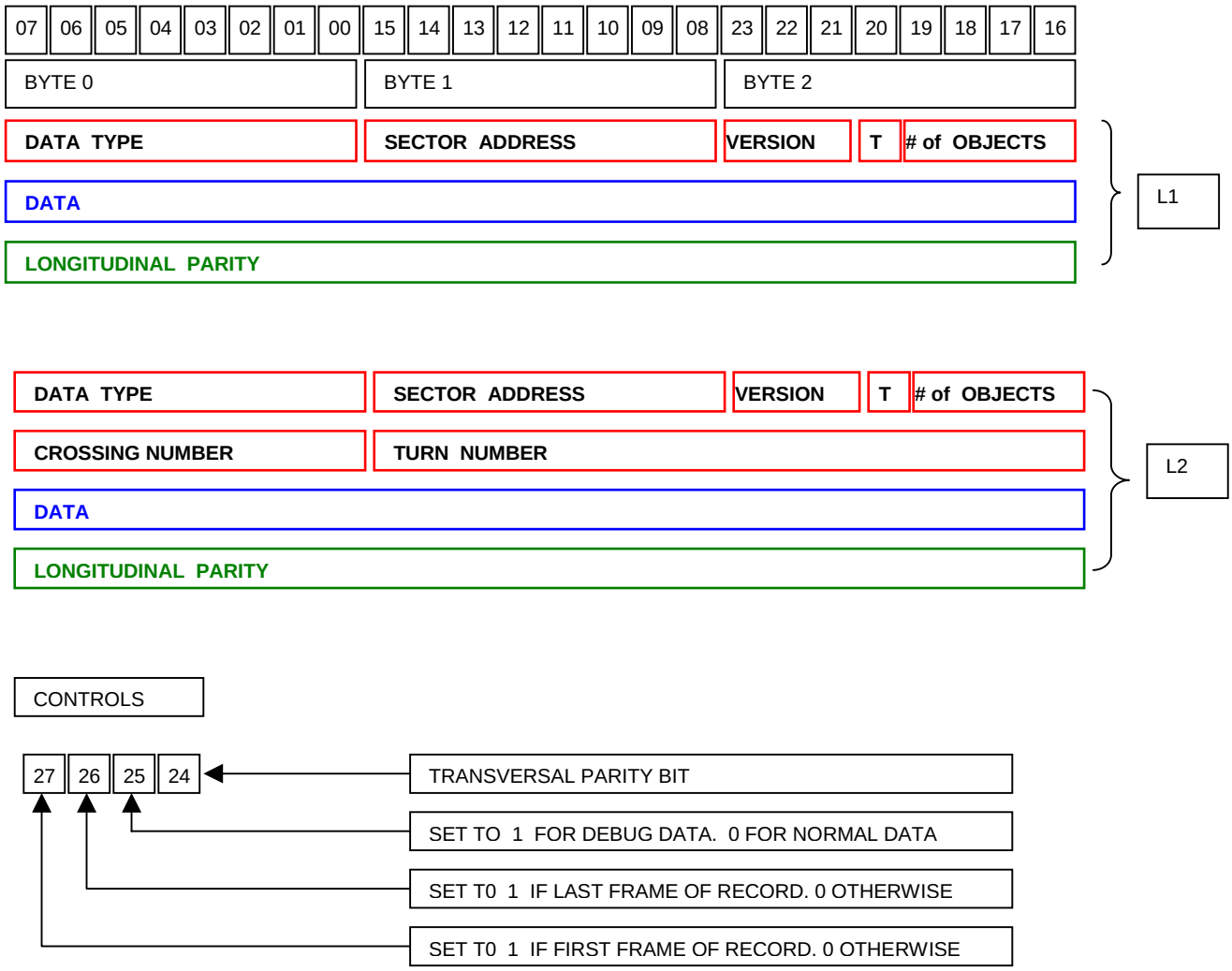
With this arrangement, we can generate a very robust and fast protocol. The first frame of every record (B25 = 1) is reserved to send information describing the record, it is a "Heather Frame". The last frame of every record (B26 = 1), the "Trailer Frame", is an especial frame dedicated to transfer the longitudinal parity of the preceding frames of the record. The second frame of the record has different meaning depending if the data to be transferred is L1 or L2 data. This difference is presented below.

As shown in the figure, the first frame of any record is reserved for a minimal head. This Header consists of three bytes. The first byte (Data Type Code) encodes the type of

information that the particular record carries. Its code permits to distinguish between L1 data and L2 data, CFT, CPS and FPS. The proposed codes are:

- 1 0 1 0 0 1 0 1 — L1 CFT /CPS axial
- 1 0 1 0 0 0 1 0 — L1 FPS
- 1 0 1 0 1 0 0 0 — L1 Forward Proton
-
- 0 1 0 0 0 1 0 1 — L2 CFT
- 0 1 0 0 1 0 1 0 — L2 CPS Axial
- 0 1 0 1 1 1 0 1 — L2 STT
- 0 1 0 1 0 0 1 0 — L2 CPS Stereo
- 0 1 0 0 0 0 1 0 — L2 FPS

Figure 3 .- Protocol to follow for transfer of data through the LVDS Links.



The second byte gives the local address of the FE Board. The two bytes combined act as a unique ID code.

The third byte gives is divided into three fields. The first field has three bits and describes the "Firmware Version" used to generate data, i.e. version used to find tracks. The second field is a single bit used as special tag. The third field of four bits provides information about the length of the record by providing the numbers of data frames that follow. This is redundant information because the end of the record is tagged by B26 high.

The last frame is reserved to provide Longitudinal Parity of the previous frames of the record. Note that the Longitudinal Parity is calculated only for the first 24 bits of each frame. The usage of longitudinal and transversal parity allows for very robust transmission. Because this schema permits to recover any single error and the probability of having double errors in a link is practically nil (less than 10^{-24}) the result is an error free transmission.

Once the protocol is defined, it is necessary to arrange the way the data is presented in the different frames. This is the subject of the following section.

Bit Allocation for L1 DATA transfers

For the purpose of this DØ Note I will consider two types of L1 data transfer: CFT/CPS Axial FPS

L1 CFT/CPS AXIAL DATA

A minimum of 122 bits is needed to transfer information from the DFE to the Broadcaster. This transfer must be made in 132ns in 7 clocks (137 if a Sync code is sent with each record).

- 72 bits of information related to tracks:
  - 3 bits Number of tracks in a given tagged Pt bin for a maximum of 6
  - four possible unsigned Pt bins or eight signed Pt bins
  - three possible PreShower tagging, i.e. No PS associated, Low Threshold or High Threshold PreShower cluster associated with the track
- for a minimum of 72 bits if information regarding the Pt bin (one of four), its sign and the PreShower tagging is implied in the position of the partial record.
- 6 bits of information for a possible isolated track as follows:
  - 1 bit for valid track
  - 1 bit for sign
  - 2 bits to indicated if there is a PS cluster associated with the track and its threshold
  - 2 bits to indicate the Pt range of the track

- 8 bits to indicate the number of scintillation fibers hits in the event
- 4 bits to give the possible number of photon candidates
- 8 bits to indicate the type of information transferred
- 8 bit to give the geographical address of the sector
- 16 (minimum) bits for tagging the transmission integrity (longitudinal parity)
-

This is eight bits more (24 if a Sync code is used) than what the Fast Serial Link can offer. On the other hand, this number of bits is far below of the number of bits (196) that a full record of seven frames of 28 bits can accommodate using the LVDS.

Figure 4.- Bit Fields allocation for L1 CFT/CPS Axial data transfers between the Digital Front End boards and the Broadcaster using LVDS Links

BYTE 0								BYTE 1								BYTE 2							
07	06	05	04	03	02	01	00	15	14	13	12	11	10	09	08	23	22	21	20	19	18	17	16
DATA TYPE								**SECTOR ADDRESS**								**VERSION**			**T**	**# of OBJECTS**			
0	Pt1 + N	0	Pt1 - N	0	Pt1 + H	0	Pt1 - H									0	Pt1 + L			0	Pt1 - L		
0	Pt2 + N	0	Pt2 - N	0	Pt2 + H	0	Pt2 - H									0	Pt2 + L			0	Pt2 - L		
0	Pt3 + N	0	Pt3 - N	0	Pt3 + H	0	Pt3 - H									0	Pt3 + L			0	Pt3 - L		
0	Pt4 + N	0	Pt4 - N	0	Pt4 + H	0	Pt4 - H									0	Pt4 + L			0	Pt4 - L		
ISOLATED TRACK				Σ Pt of TRACKS		# γ										TOTAL NUMBER OF HITS							
Longitudinal Parity																							

The bit allocation for this type of data is shown in Fig. 4.

In accordance with agreement to report a maximum of six tracks per Pt bin from any 4.5^0 sector, the fields allocated for a particular tagged signed Pt are 3 bit deep.

The maximum number of photons to be reported is 3, this requires the allocation of a field of two bits.

There are eight bits allocated for the total number of fibers hit, I think this number is really too high. The field under the name of ΣPt of all tracks in a 4.5^0 sector requires some explanation. It really reports a number between 0 and 15 obtained using the following algorithm:

For each track
    Subtract 5 to the Pt of the track
If the result is 0 or less than 0 record 0, otherwise record the result
Sum all the resulting recorded values of the tracks

If the result is equal or greater than 15 report 15, otherwise report the Sum value

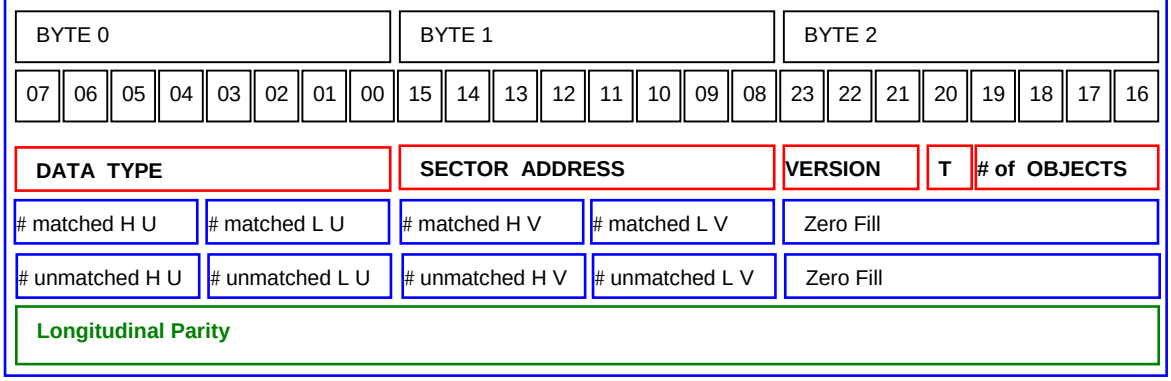
The field reporting the possible Isolate Track is arranged as follows:

- V Valid bit; set to 1 if there is an Isolated Track
- H Set to 1 if there is a High Threshold Cluster associated with the track
- L Set to 1 if there is a Low Threshold Cluster associated with the track
- S Sign bit; set to 1 if the sign of the Pt of the track is negative
- Pt Pt bin; two bits giving the Pt range to which the track belongs

L1 FPS DATA

The amount of information is very small in comparison with the previous case. This permits to use only two data frames as shown in Fig. 5

Figure 5.- Bit Fields allocation for L1 FPS data transfers between the Digital Front End boards and the Broadcaster using LVDS Links



Bit Allocation for L2 DATA transfers between Fe and broadcaster

There are several types of L2 data that the Digital Front End Boards transfer to the Broadcaster. The following cases are presented:

- CFT Data to the L2CFTpp
- CPS Axial Data to the L2CPSpp
- CPS Stereo Data to the L2CPSpp
- FPS Data to the L2FPSpp

For each of the four cases listed, a very important situation must be taken into consideration: there is no data to be reported by the Digital Board. In this case, the record consists of only the frames with Header information (beginning of record) and the

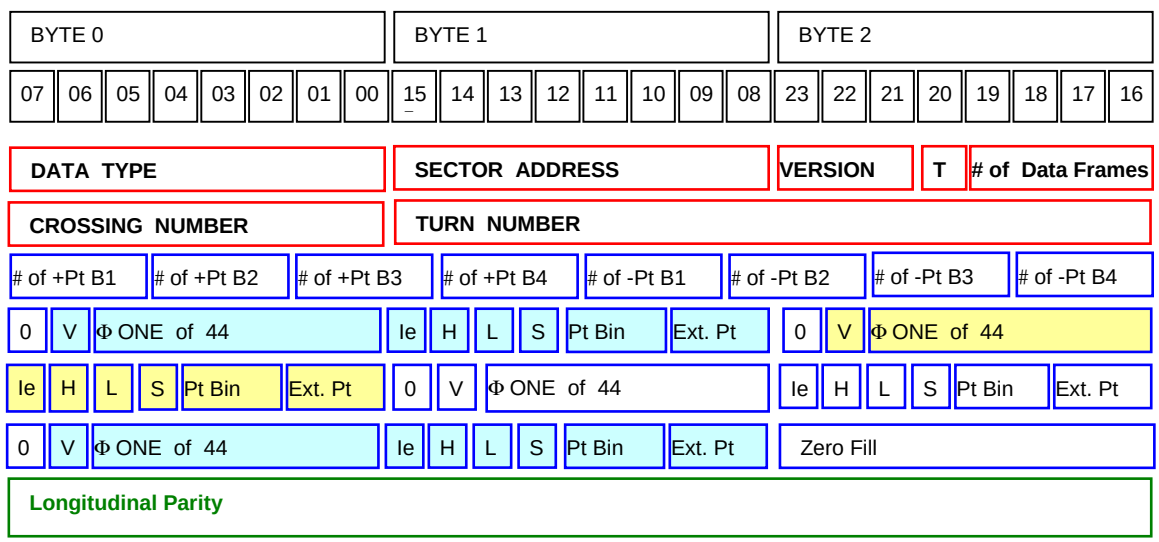
Longitudinal Parity (end of record). This minimal transfer is necessary because each Broadcaster expect information from all the Digital boards allocated to it.

L2CFT DATA

Two possible situations can be present: there are one or more tracks in the 4.5^0 sector, or there are no tracks in the sector. Figure 6 shows the general case where some tracks are reported. To make the example more meaningful, four tracks are reported.

Note that in this case the "Number of Data Frames that Follow" can not be less than two. This is because the first frame of data (F3) carries a special kin of information: the number of tracks found in each Pt bin.

Figure 6.- Bit Fields allocation for L2 CFT data transfers between the Digital Front End boards and the Broadcaster using LVDS Links. Case for multiple Tracks (four as example).



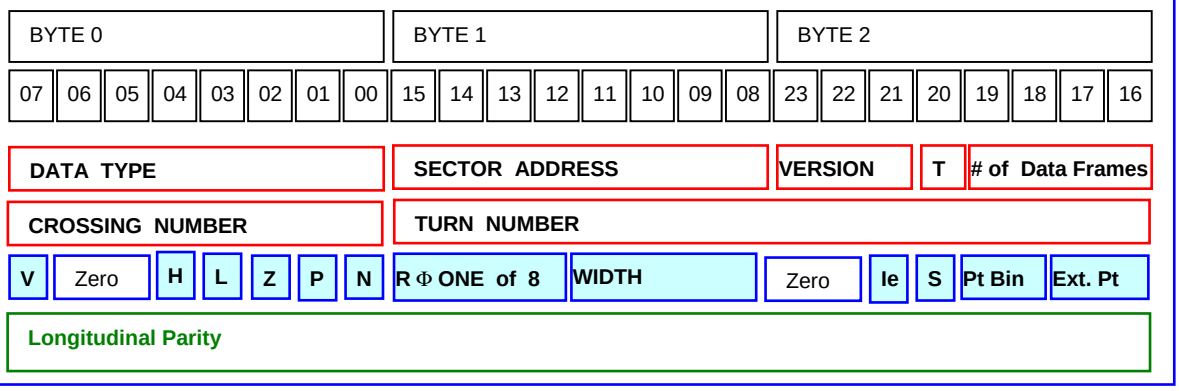
The meaning of the data fields is as follows:

V	valid track. This bit is set if there is a valid track.
Φ Value	the relative address of the eight layer doublet that belongs to the track.
Ie	if set the track is an Isolated electron. No more than one track in the sector can be an Isolated electron.
H	if set the track is correlated with a High Threshold PreShower cluster
L	if set the track is correlated with a Low Threshold PreShower cluster
S	sign of the Pt of the particle
Pt bin	Pt of the track; one of the four possible ranges
Ext. Pt	a value used to provide finer Pt rangesCPS Axial Data to the L2CPS pre processors

L2CPS AXIAL DATA

The data required by the L2CPSpp from the Digital board is shown on Fig. 7 with the meaning of the different fields listed below it.

Figure 7.- Bit Fields allocation for L2 CPS Axial data transfers between the Digital Front End boards and the Broadcaster using LVDS Links.



- **V** set if a valid cluster information follows
- **H** if set the cluster is a High Threshold cluster
- **L** if set the cluster is a Low Threshold cluster
- **CLUSTER ADDRESS** Includes four fields;
  - **Z** gives information about the Z position of the cluster; North/ South
  - **P** if set the cluster starts in the previous sector
  - **N** if set the cluster starts in the next sector
  - **R. Φ** relative address of the first element of the cluster within the proper sector
- **WIDTH** Number of elements in the cluster (maximum is 8)

If the cluster is associated with a track then the following fields have information, otherwise these fields are all zero

- **S** sign of the Pt of the track associated with the cluster
- **Pt bin** Pt of the track; one of the four possible ranges
- **Ext. Pt** a value used to provide finer Pt ranges

A cluster could be associated with a track of low Pt such that the track was not reported in the CFT information to the L2CFTpp. In this situation, the associated track parameters will be reported in this record. A cluster could be associated with more than one track. If more than one track is associated with the cluster then: for each associated track that was reported in the CFT information to the L2CFTpp, the cluster information is repeated with the information of each track

L2CPS STEREO DATA

In the case of Stereo information, the reporting is very similar to the previous case. In this case there is not tracks associated with a cluster and it is necessary to distinguish between the orientation of the strips of the PreShower detectors. The two orientations are named U and V. The data field allocation for this case is presented in Fig. 8. Data to the L2CPS pre processors

Figure 8.- Bit Fields allocation for L2 CPS Stereo data transfers between the Digital Front End boards and the Broadcaster using LVDS Links.

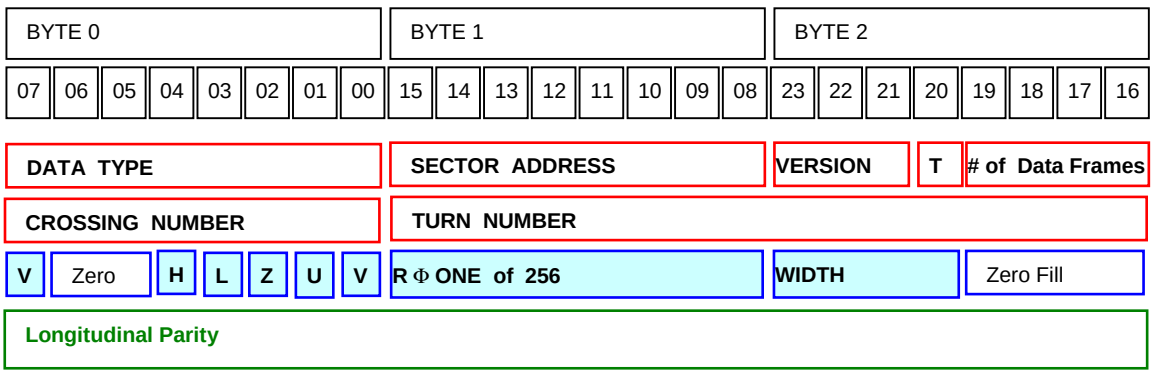
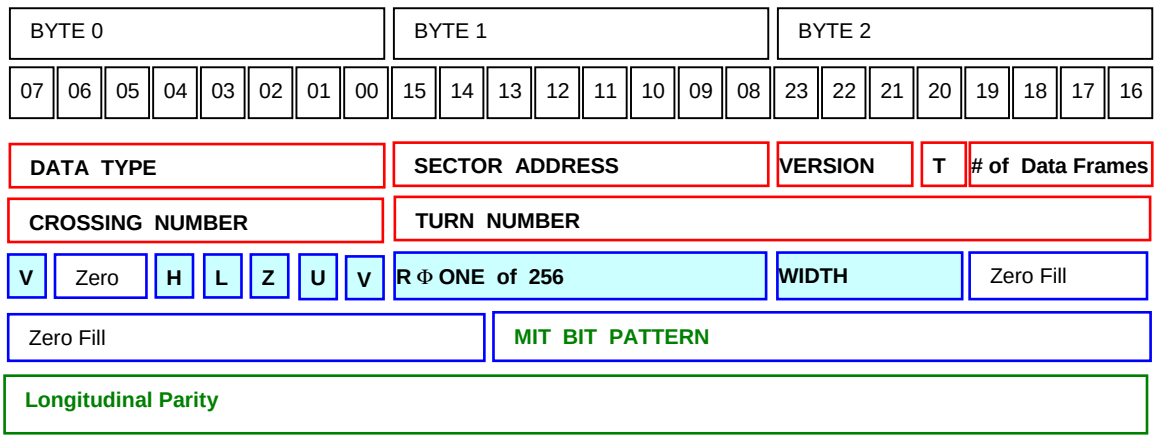


Figure 9.- Bit Fields allocation for L2 FPS Stereo data transfers between the Digital Front End boards and the Broadcaster using LVDS Links.



L2FPS DATA

The data required by the L2FPSpp is very similar to the CPS Stereo data. A mayor difference is that the L2FPSpp needs the correlation between clusters in the PS detectors located before and after the showering material. This data is given as a "MIT Bit Pattern" generated in the "before" detector. The data fields assignment is shown in Fig. 9.

Using the DFE board as a broadcaster board: second MODIFICATION

A functional block diagram of the Broadcaster was presented in the January Design Review. At that time, the possibility of utilizing the Digital Front End Board for its implementation was not yet considered. This Functional Block Diagram is presented in Fig. 10.

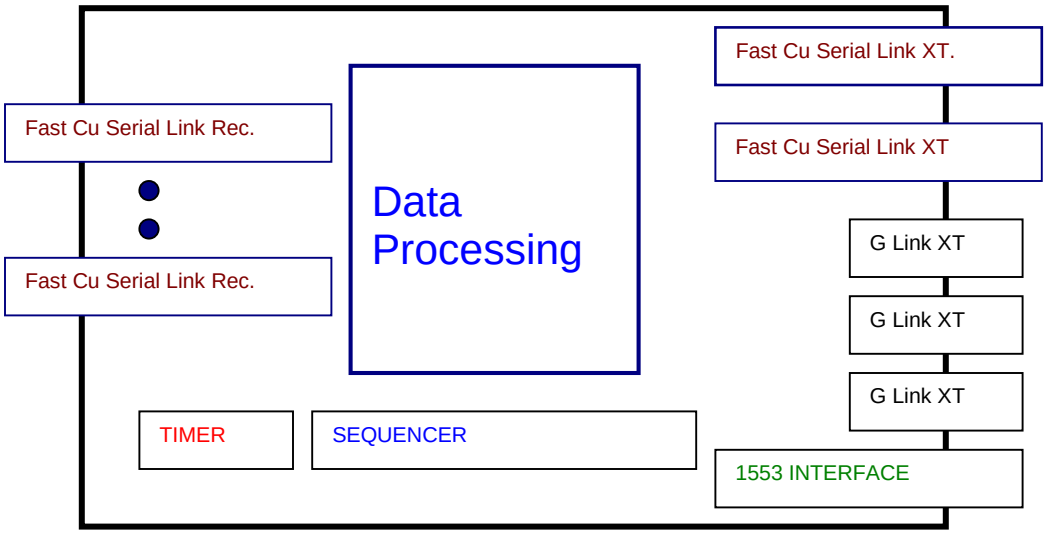


FIG. 10. Functional Block Diagram of the

The I/O channels are as follows:

- 10 Fast Copper Serial Links — Inputs from FE
- 2 Fast Copper Serial Link — Output to L1Trigger Manager (two are needed to provide the Pt sign information)
- 2 G Links Transmitters — Output to L2 FIC
- 1G Link Transmitter — Output to L3
- 1 1553 Interface — Back Plane Connection

The logic represented by the Functional Blocks "Data Processing", "Sequencer" and "Timer" are implemented using high end FPGAs.

At the same Technical Review, a new design of the Front End Electronics was shown. The design of the Digital Front End board is particularly interesting. The design of these boards calls for two Daughter Boards to implement function specific logic while the common logic is implemented directly in the board. In the case of the Digital Front End Boards for the CFT/CPS Axial, each Daughter Board implements the Track Finding, Pt Sorting and Cluster Finding/Track Matching algorithms originally implemented in the digital portion of the FE Board. The breaking of the bulk of the logic into two separated Daughter Boards working in parallel is a logical result of the fact that one DFEB serves two adjacent Analog FE Boards as shown on Fig. 1.

A comparison of Fig. 10 and Fig. 11 shows that there are enough similarities between them to suggest implementing the Broadcaster with a Digital Front End Board. The differences in algorithms being taken up by different firmware in the Daughter Boards and

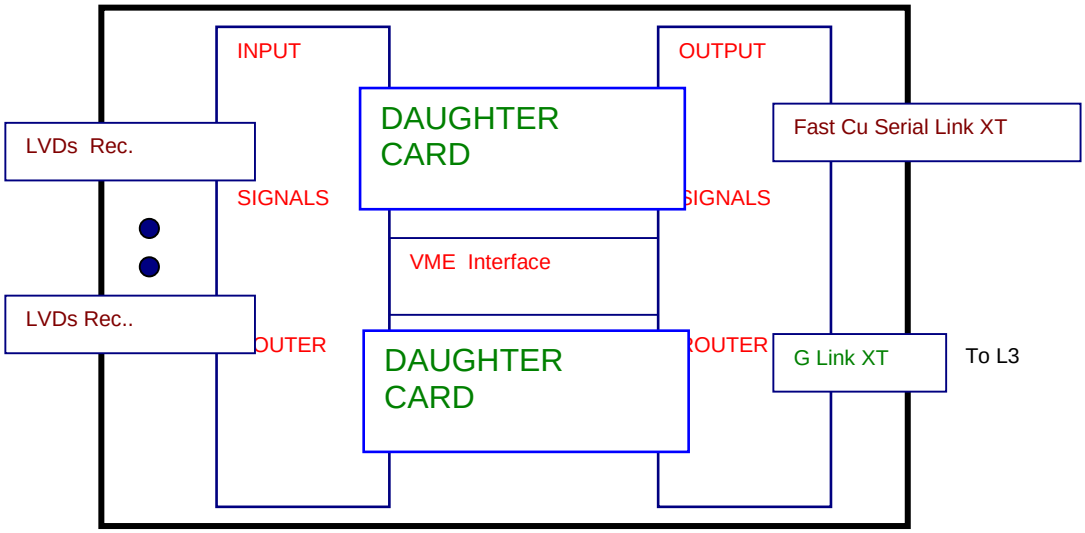


Fig. 11. Functional Block Diagram of the Digital Front End Board.

the 1553 interface substituted by a VME interface.. This is the suggestion made by Jameison Olsen and John Anderson. However, changing firmware only is not sufficient; to make a Broadcaster Board of a Digital Front End Board it is necessary to make changes in the I/O of the board to satisfy the needs of the Broadcaster. To increase the number of input LVDS links from eight to ten is not a very difficult task. To increase the number of output links from one Fast Copper Serial Link and one G Link to two Fast Copper Links and three G Links is quite more difficult. Not only the amount of real state required for the I/O increases by almost a factor of three, the complexity of the routing of the signals that need to reach each output link became far more complex. This difficulty can be circumvented by using different daughter boards for the routing of signals in the final stage to the necessary output links. The two flavors of the board will look something like what it is sketched on Fig. 12.

The information that the L1 Trigger Manager for the CFT/CPS Axial receives and the number of bits required is summarized as follows:

- number of tracks found organized by Pt bin, Sign and type of PS tagging
  4 (bits for # of Tracks) * 4 (# of Pt bins) * 2(sign) * 3 (PS tags) = **96 bits**
- 5 possible Isolated Tracks with the following information
  5 *(Pt bin (2 bits) + Sign (1bit) + eISO (1bit) + PS tag (2bits)) = **30 bits**
- number of possible photons with a maximum of eight (4 bits) = **4 bits**
- number of total fibers with signal with a maximum possible of 4,800 (13 bits) although this number could be scaled by a factor of 32 needing **8 bits** only

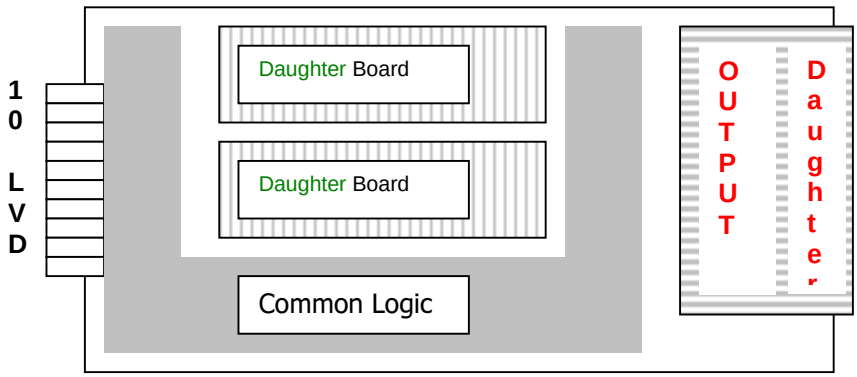


Fig. 12. The modified Digital Board. The Mother Board has 10 LVD Inputs and all common logic. The Daughter Boards take care of the different "flavors".

Note that no information about North/South is given. This implies that a minimum of 138 bits is required by the L1CFT Trigger Manager. This exceeds the maximum of 112 bits (without longitudinal parity) that a Fast Copper Serial Link can transfer in 132ns! Thus the need to use two Serial Links between each Broadcaster Board and the L1Trigger Manager. This will increases the number of data bits to be transfer from each Broadcaster to the L1CFT Trigger Manager to a comfortable 192 plus 32 bits for longitudinal parity. This solution also increases the number of L1CFT Trigger Manager Boards of the muon type by a factor of two. A better solution is to send the information from the Broadcaster to the CFT Trigger Manager via a LVD link. This gives an effective bandwidth of 6*24 = 144 bits per 132ns which is six bits more than what it is needed.

These changes result in a single Digital Mother Board whose functionality is defined by the type of Daughter Boards and firmware used. So far, we have described a system with two flavors of Digital Boards:

the Digital Front End Board characterized by
two Daughter Boards with function-specific firmware
an output Daughter Board with **one** LVD link and **one** G Link
the Broadcaster characterized by
one Daughter Board with function-specific firmware
an output Daughter Board with **one** LVD link and **three** G Link

There are two major problems with this implementation. On one hand the MTM card accepts only Fast Copper Serial Links, on the other hand the possibility of accommodating three G Links in the output of the Digital Mother Card is very improbable. There must be a better solution.

Using the DFE board as a L1 Trigger Manager board

A careful look at the implementation of the L1 Muon Trigger Manager boards and at the Digital Board as described above shows many similarities between them. This strongly suggests the possibility to implement many of the functions of the L1CFT Trigger Manager using the Digital Board. Although all functions required by the Trigger Manager to manipulate data can be easily implemented in the Daughter Boards, the -Trigger Manager has also the required logic connections to work as a Geographical Sector. The problems enumerated in the previous paragraph are circumvented if we use a Broadcaster Digital board to perform many of the functions that the μ-Trigger Manager board does and we relegate the function of the later to communicate with the Trigger Framework an to perform the necessary functions of a Geographical Sector.

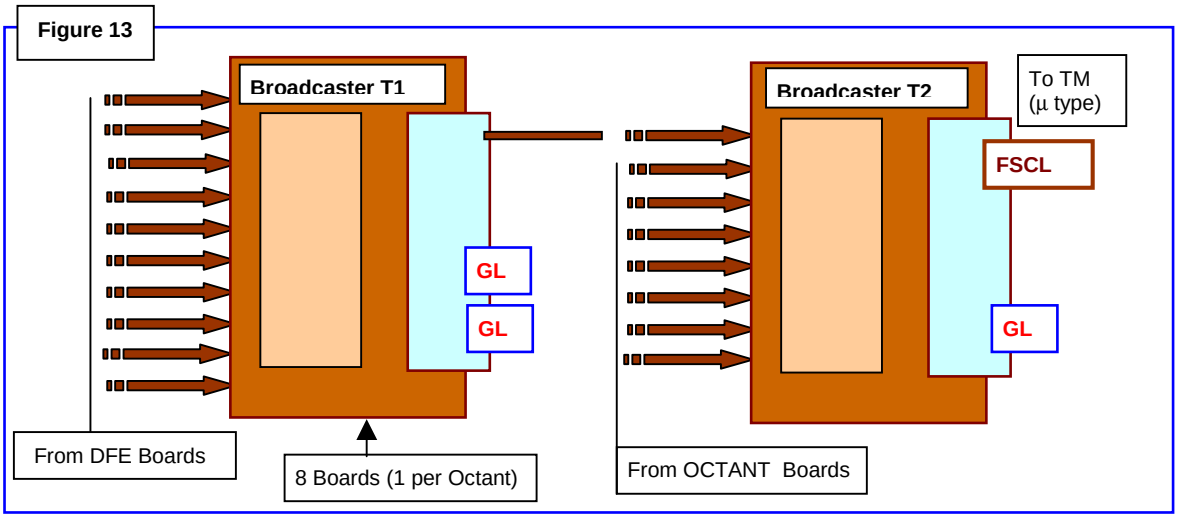
If such a solution is implemented, the CFT, PS and FP acquisition system and Trigger is drastically simplified. It can be implemented using only one type of board in three flavors. Each flavor is defined by the type of Daughter Boards. These are:

- Digital Front End
  - Two Function-specific Daughter Cards
  - One Output Daughter Card with four LVD links and two Fast Serial Copper Links
- Broadcaster T1
  - One Function-specific double Daughter Card
  - One Output Daughter Card with one or more LVD links and two G Links
- Broadcaster T2
  - One Function-specific double Daughter Card
  - One Output Daughter Card with one or more LVD links, one G Link and one Fast Serial Copper Link

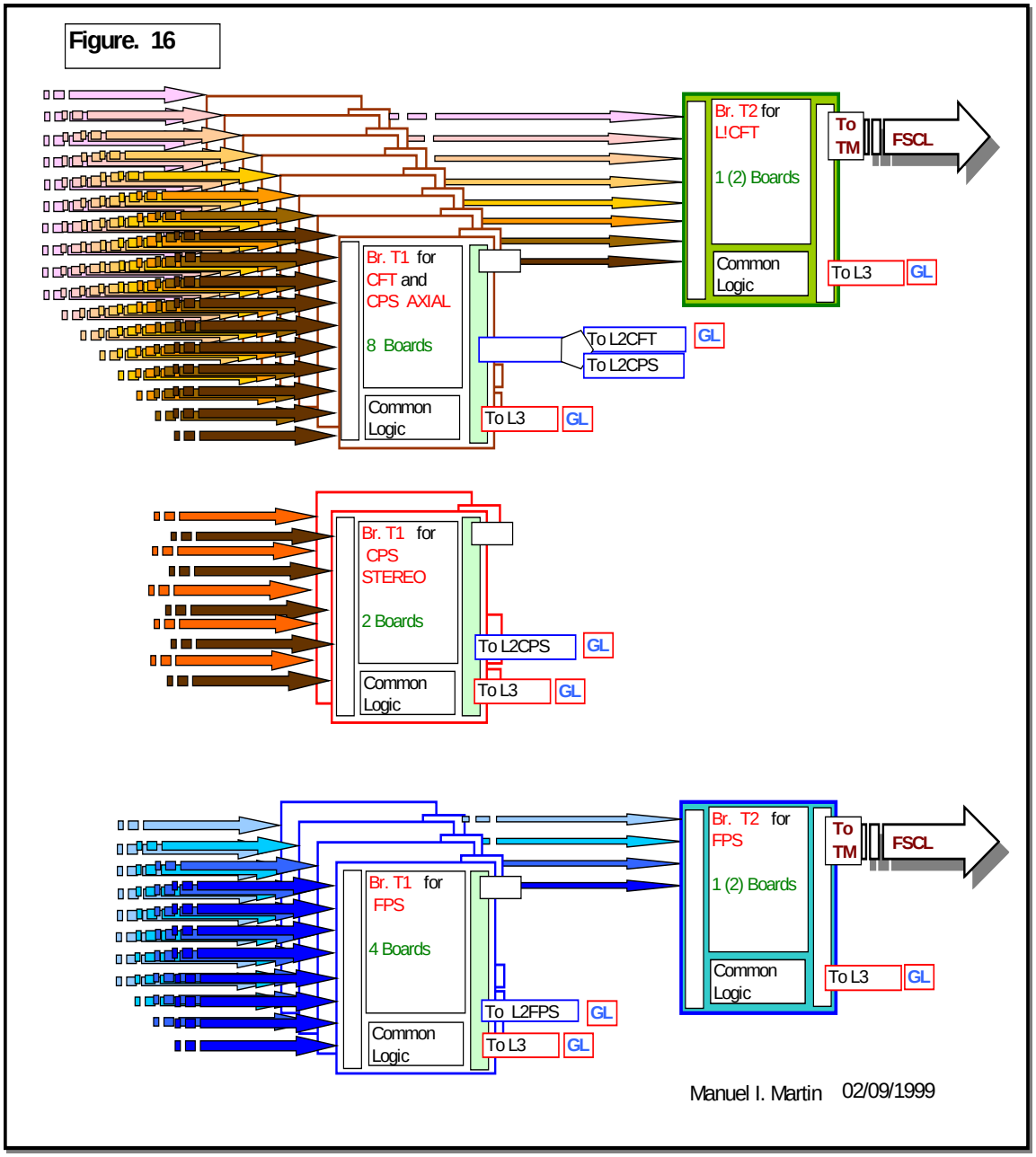
In all cases, the input to the board consists of up to ten LVD Links. In the case that some input/output links are not used, only the specific hardware necessary to implement the used links will be installed.

The Broadcaster system for the L1CFT/CPS Axial implemented using Broadcaster

Figure 13



Cards type T1 and T2 is shown in Fig. 13. Fig. 14 shows the complete Broadcaster System for the CFT, CPS and FPS using the same type of boards. Note that the information sent to L2CFT and L2CPS Axial is exactly the same, the pre-processors will need to sort out which information they need to use.



A break down of the different subsystems and their hardware requirements is as follows:

CFT/CPS Axial

- 40 Digital Front End Boards each of wich has
  - 8 LVD input links to serve two Analog Front End Boards
  - 2 Fast Serial Copper output links to send information to the μ-L1 Trigger
  - 2 LVD output links to serve one fifth of one Broadcaster
- 8 Broadcasters type T1, each serving an octant and having
  - 10 LVDs input links serving 5 Digital Front End boards
  - 1 LVD output link serving an eighth of the L1CFT Trigger Manager
  - 1 G Link with an optical splitter serving the L2CFT and L2CPS pre processor
  - 1 G Link serving the L3
- 1 Broadcasters type T2, each having
  - 8 LVDs input links serving 8 Broadcasters type T1
  - 1 Fast Serial Copper Link serving one μ-type Trigger Manager
  - 1 G Link serving the L3

CPS Stereo

- 5 Digital Front End boards each having
  - 8 LVD input links to serve two Analog Front End Boards
  - 2 LVD output links to serve one fifth of one Broadcaster
- 2 Broadcasters type T1 each serving two quadrants and having
  - 5 LVDs input links serving 5 Broadcasters type T1
  - 1 G Link output to the L2CPS pre processor
  - 1 G Link output to the L3

FPS

- 32 Digital Front End boards each having
  - 8 LVD input links to serve two Analog Front End Boards
  - 2 LVD output links to serve one fourth of one Broadcaster
- 4 Broadcasters type T1 each serving one quadrant and having
  - 8 LVD input links to serve fourth Digital Front End boards
  - 1 LVD output links to serve one fourth of the L1FPS
  - 1 G Link output to the L2FPS pre processor
  - 1 G Link output to the L3
- 1 Broadcasters type T2 having
  - 4 LVDs input links serving 4 Broadcasters type T1
  - 1 Fast Serial Copper Link serving one μ-type Trigger Manager
  - 1 G Link serving the L3

Thus, the total resources needed for the Broadcaster System for the CFT, CPS and FPS are:

16 Broadcasters type T1
2 Broadcasters type T2
1 Crate (Broadcaster Crate)

1 Crate Control Boards with VME
12 LVD Links
2 Fast Serial Copper Links
38 G Links

A possible organization of the boards in this crate is shown in Fig. 17. With the L1CFT/CPS Axial and the L1FPS Broadcaster type T2 Boards included.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
CONTROL	L1CFTTM	L1FPSTM	BCFTCPSA	BCFTCPSA	BCFTCPSA	BCFTCPSA	BCFTCPSA	BCFTCPSA	BCFTCPSA	BCFTCPSA	BFPS	BFPS	BFPS	BFPS	BCPSS	BCPSS			

Figure 14. Possible Broadcaster Crate organization.
with L1CFT/CPS Axial and the L1FPS included!

This does not include neither the Forward Proton nor the STT Systems

Following Good Engineering Practice, or a better way to send information to the Framework

The usage of electrical conductors for data transfers between self contained systems is a sure way to courtship disaster. One thing I learned: *design to avoid problems, in particular noise and ground loop problems, if you want to have success.* To use numerous copper links between "self-contained" systems is not the best way to deal with noise and it will most surly create big ground loops. This is the mayor problem that I find with the existing scheme (using the μ Trigger Manager Card): the usage of a copper links between electronics located in the Platform and these located in the Moving Counting House. These are the flat cables used to send information from the Trigger Manager to the Framework. This problem can be totally eliminated with a more conservative design.

"Change the links between the m-type Trigger Manager boards and the Trigger Framework to G Links !!!"