

ID	Task Name	Duration	Start	Finish	Predecessors	Constraint	WBS	Resource Names
2179	TRIGGER SYSTEM	265.2 w	10/2/95	2/5/01		As Soon As		
2180	Framework	202 w	1/2/96	2/2/00		As Soon As		
2181	Foundation Module Board Design	36 w	1/2/96	9/12/96		Start No Ear	1.4.1.1(0.1)	k\$[0.53]
2182	Design the Derivative Boards	78 w	6/19/96	1/21/98	2181SS+24 w	As Soon As f	1.4.1.1(0.1)	EEU141,k\$[0.53]
2183	Circuit Board Layout Finished	0 w	1/21/98	1/21/98	2182	As Soon As		
2184	FPGA Code for Foundation Module	16 w	6/19/96	10/10/96	2181SS+24 w	As Soon As f	1.4.1.1(0.1)	EEU141,k\$[0.53]
2185	FPGA Code for the Derivative Boards	97 w	9/13/96	8/28/98	2184SS+12 w	As Soon As f	1.4.1.1(0.1)	EEU141,k\$[0.53]
2186	L1/L2 Support Equipment	102 w	1/2/96	1/21/98	2181SS	Start No Ear	1.4.1.1(0.1),1.4.1.2.2-1.4.1.2.3,1	EEU141[0.5],k\$[2.88]
2187	Obligate Funds for SCL and Hub System	0.2 w	6/1/99	6/1/99		Start No Ear	1.4.5.5	k\$[1.9],k\$c[0.28]
2188	Prototype Serial Command Link Receiver	141.8 w	12/10/96	10/22/99		Finish No Ea		EEF141
2189	Prototype Serial Command Link Transmitter	141.8 w	12/10/96	10/22/99	2188SS	Finish No Ea		ETF141[0.6]
2190	Build Cards and Assemble L1 Framework	86 w	2/28/97	11/16/98	2182SS+50 %	As Soon As f	1.4.1.1(0.1),1.4.1.2.1,1.4.1.2.4	EEU141[0.5],k\$[6.23]
2191	L1 Framework Testing	11 w	11/17/98	2/17/99	2190	As Soon As f		
2192	L1 Framework Delivered to Fermilab	0 w	12/16/98	12/16/98	2191	As Soon As		
2193	Commission L1 Framework for First User	5.6 w	9/16/99	10/25/99	2188,2189,2192	As Soon As f		
2194	Build Cards for L2 Framework	32 w	4/2/98	11/16/98		Start No Ear	1.4.1.1(0.1),1.4.1.3.1,1.4.1.4.1,1	EEU141[0.5],k\$[3.55]
2195	Assemble L2 Framework	4 w	9/15/99	10/12/99	2194	Start No Ear		
2196	L2 Framework Testing	1 w	10/13/99	10/19/99	2195	As Soon As f		
2197	Commission L2 Framework for First User	12 w	10/26/99	2/2/00	2193	As Soon As f		PhysU141[0.5],EEU141[0.5]
2198	L2 Framework Delivered to Fermilab	0 w	2/2/00	2/2/00	2197	As Soon As		
2199	Trigger Control Software	221.2 w	1/2/96	6/16/00		As Soon As		
2200	Implement L1 Exerciser/Diagnostics with NT	36 w	1/2/96	9/12/96		Start No Ear	1.4.1.1(0.1)	EEU141[0.5],k\$[0.53]
2201	Operate L1 Frame with Trg Mon	90 w	2/28/97	12/16/98	2190SS,2200	As Soon As f	1.4.1.1(0.2)	EEU141,k\$[1.06]
2202	Operate L1 Framework at FNAL	6 w	2/18/99	3/31/99	2191,2201	As Soon As f		EEU141
2203	Operate L2 Framework	12 w	10/20/99	1/27/00	2196,2202	As Soon As f		
2204	Operate Frameworks, L1 Calor, L2 Trigger	12 w	1/28/00	4/20/00	2203	As Soon As f		EEU141
2205	Operate with Rate Control, Servers, Data Logging	8 w	4/21/00	6/16/00	2204	As Soon As f		
2206	Level 1 Calorimeter Trigger	210.4 w	10/1/96	1/8/01		As Soon As		
2207	Determine Specifications	123 w	10/1/96	4/2/99		As Soon As f	1.4.3.1.1(0.15)	PhysU143[0.5],EEU143,k\$[0.1],k\$c[0.02]
2208	Design Cal to L2 and L3 Readout	20 w	4/5/99	8/24/99	2207	As Soon As f		PhysU143,EEU143[0.5],k\$c[0.35]
2209	Build 20% Cal to L2 and L3 Readout	12 w	5/22/00	8/15/00	2197,2208	Start No Ear		PhysU143,EEU143[0.5]
2210	Procure VRB Cards and Controller	1 w	2/7/00	2/11/00		Start No Ear	1.4.3.1.8,1.4.3.1.9	k\$[0.73]
2211	M3- Cal Readout Available to L2	0 w	8/15/00	8/15/00	2209	As Soon As		
2212	Design and Build Quadrant Signal	56 w	8/25/99	10/11/00	2208,2209	As Soon As		EEU143,k\$[0.35],k\$c[0.1]
2213	Modify Trigger Pickoffs	32 w	3/1/00	10/13/00	2207	Start No Ear	1.4.3.1.1(0.15),1.4.3.1.5	EEU143,PhysU143,k\$[0.52],k\$c[0.15]
2214	Design and Build TCC Interface	18 w	4/5/99	8/10/99	2207	As Soon As f	1.4.3.1.1(0.15),1.4.3.1.7	EEU143,k\$[0.11],k\$c[0.03]
2215	Construct Timing Hardware	19 w	4/6/00	8/18/00	2214	Start No Ear	1.4.3.1.1(0.15),1.4.3.1.6	EEU143,k\$[0.17],k\$c[0.04]
2216	Commission L1 Cal Trigger	11 w	10/16/00	1/8/01	2215,2209,2212,2213,2214	As Soon As f	1.4.3.1.2	PhysU143[0.5],EEU143[0.5],k\$[0.65],k\$c[0.16]
2217	M3-Calorimeter Level 1 Trigger Commissioned	0 w	1/8/01	1/8/01	2216,2212,2213	As Soon As		
2218	Muon Level 1 Trigger	252.8 w	1/2/96	2/5/01		As Soon As		
2355	Level 1 Central Fiber Tracker	160.2 w	11/3/97	2/5/01		As Soon As		
2356	Specification Stage	23.8 w	11/3/97	5/1/98		Start No Ear		
2357	Acceptance of Specifications	0 d	5/1/98	5/1/98	2356	As Soon As		
2358	Preliminary Design	18 w	2/1/98	6/8/98		As Soon As f		
2359	Design	26 w	6/9/98	12/11/98	2358	As Soon As f		
2360	Design Review	4 w	12/14/98	1/22/99	2359	As Soon As f		
2361	Design Review Completed	0 d	1/22/99	1/22/99	2360	As Soon As		
2362	Finalize Design	15 w	1/25/99	5/7/99	2361	As Soon As f		
2363	Assemble Commission CTT System	11 w	11/13/00	2/5/01	949,983,994	Start No Ear		PhysF143[2],PhysU143[2]
2364	M3-CTT Level 1 Trigger Commissioned	0 w	2/5/01	2/5/01	2363	As Soon As		
2365	M3-L1 Commissioned	0 w	2/5/01	2/5/01	2206,2218,2355	As Soon As		
2366	Level 2 Trigger	265 w	10/2/95	2/2/01		As Soon As		
2367	Michigan State University MOU	0.2 w	6/1/98	6/1/98		Start No Ear	1.4.4.2.1.2,1.4.4.2.1.3(.68),1.4.4	k\$[4.91],k\$c[1.1]
2368	University Of Maryland MOU	0.2 w	6/1/98	6/1/98		Start No Ear	1.4.4.2.2.3(.83),1.4.4.6(0.5)	k\$[1.16],k\$c[0.33]
2369	University Of Illinois-Chicago MOU	0.2 w	6/1/98	6/1/98		Start No Ear	1.4.4.4.1(.33),1.4.4.9(.8)	k\$[0.42],k\$c[0.08]
2370	Foreign Contributions (1.4.4)	0.2 w	6/1/98	6/1/98		Start No Ear	1.4.4.2.1.3(.32)	k\$[0.57],k\$c[0.17]
2371	Develop Conceptual Design	104 w	10/2/95	10/24/97		As Soon As		
2372	Design Overall Architecture	104 w	10/2/95	10/24/97		Start No Ear		PhysU144[0.1]
2373	Deadtime Queuing Simulations	104 w	10/2/95	10/24/97		Start No Ear		PhysU144[0.2]
2374	Overall L2 Rate Simulations	104 w	10/2/95	10/24/97		Start No Ear		PhysF144[0.2],PhysU144[0.2]
2375	Conceptual Design Complete	0 w	10/24/97	10/24/97	2372,2373,2374	As Soon As		
2376	Prepare Common Software Items	120.4 w	1/2/98	6/6/00		As Soon As		
2377	Set up Library Procedures	72 w	1/2/98	6/11/99		Finish No Ea		PhysU144[0.2]
2378	Unpack L2 Output into L3 Structures	44 w	10/1/98	8/24/99		Finish No Ea		PhysU144[0.4]
2379	Code Online Verification Frame	38 w	8/26/99	6/6/00		Start No Ear		PhysU144[0.5]
2380	Manufacture Components	238 w	3/1/96	12/18/00		As Soon As		
2381	Build Processor	238 w	3/1/96	12/18/00		As Soon As		
2382	Initial Design	183.6 w	3/1/96	11/9/99		As Soon As		
2383	Select Prototype Processor	52 w	3/1/96	3/18/97		As Soon As f		EEU144[0.1],PhysU144[0.2]
2384	Simulate Timing Performance	93.2 w	3/1/96	1/20/98	2383SS	As Soon As f		PhysU144[0.2]
2385	Test Code Downloading	15 w	3/19/97	7/2/97	2383	As Soon As f		PhysU144[0.5]
2386	Choose Monitoring Data Path	28 w	3/19/97	10/3/97	2383	As Soon As f		PhysU144[0.1]

ID	Task Name	Duration	Start	Finish	Predecessors	Constraint	WBS	Resource Names
2387	Define COOR Communication	127 w	4/21/97	11/9/99		Finish No Ear		PhysU144[0.2]
2388	Define Input, Output Formats	83 w	4/21/97	12/17/98		As Soon As f		PhysU144[0.1]
2389	Prepare Global TDR	40.2 w	4/21/97	2/13/98		Start No Ear		PhysU144[0.2]
2390	Global Processor TDR Submitted	0 w	2/13/98	2/13/98	2385,2389	As Soon As		
2391	Level 2 Programming and I/O Defined	0 w	11/9/99	11/9/99	2387,2388,2457,2481,2482,2483	As Soon As		
2392	Processor Development/Production	167.8 w	7/28/97	12/18/00		As Soon As		
2393	Receive Prototype PCI Interfaces to Processor	30.2 w	7/28/97	3/11/98	2383	Start No Ear	1.4.4.2.6.1(0.1)	
2394	Receive and Install VME Prototype Processor	3 w	12/1/98	1/4/99	2390,2393	Start No Ear	1.4.4.2.6.2(0.3),1.4.4.9(2)	EEU144,k\$[0.11],k\$c[0.02]
2395	Debug and Operate Alpha Processor	32 w	1/5/99	8/18/99	2394,2439FF,2431FF	As Soon As f	1.4.4.2.1.1,1.4.4.2.6.1(0.9),1.4.4	EEU144,PhysU144[0.2],ETF144[0.25],k\$[0.8],k\$c[0.18]
2396	Alpha Production - first set	44 w	8/19/99	7/12/00	2395	As Soon As f	1.4.4.2.6.3,1.4.4.2.10(.28)	ETF144[0.25],k\$[0.81],k\$c[0.16]
2397	Alpha Production -Remainder	22 w	7/13/00	12/18/00	2396	As Soon As f		
2398	Alpha Cards Received	0 w	12/18/00	12/18/00	2397	Start No Ear		
2399	Build Magic Bus Transceiver	214.6 w	3/1/96	6/30/00		As Soon As		
2400	Conceptual Design of Transceiver Card	90.6 w	3/1/96	12/19/97	2383SS	As Soon As f		PhysU144[0.2]
2401	MBT Specification	60 w	1/2/98	3/18/99	2400	As Soon As f	1.4.4.2.2.1(0.4)	EEU144[0.1],PhysU144[0.25],k\$[0.38],k\$c[0.12]
2402	Finalize MBT Design	0 w	3/18/99	3/18/99	2401	Start No Ear		
2403	Build First Prototype MBT	32 w	7/7/98	3/4/99		As Soon As f	1.4.4.2.2.1(0.6),1.4.4.2.2.2	EEU144,k\$[0.83],k\$c[0.22]
2404	Build Second Prototype MBT	31 w	3/5/99	10/12/99	2403	As Soon As f		
2405	MBT preproduction	12 w	10/13/99	1/20/00	2404	As Soon As f		EEU144
2406	MBT production	23 w	1/21/00	6/30/00	2402,2405	As Soon As f	1.4.4.2.2.3(.17)	k\$[0.22],k\$c[0.06]
2407	MBTs Received	0 w	6/30/00	6/30/00	2406	As Soon As		
2408	Build Second Level Input Computer	112.6 w	9/2/97	12/10/99		As Soon As		
2409	SLIC Specification and TDR	65 w	9/2/97	1/5/99		Start No Ear	1.4.4.2.3.1(0.4)	EEU144[0.5],PhysU144[0.25],k\$[0.48],k\$c[0.14]
2410	Finalize SLIC Conceptual Design	0 w	2/1/99	2/1/99	2409,2417	As Soon As		
2411	Design/Prototype SLIC Mezzanine	41 w	7/2/98	5/4/99		Start No Ear	1.4.4.2.3.1(0.6),1.4.4.2.3.2	EEU144,k\$[0.92],k\$c[0.26]
2412	Design/Prototype SLIC Motherboard	32 w	1/4/99	8/17/99		Start No Ear		
2413	SLIC Mezzanine Production	16 w	8/18/99	12/10/99	2411,2412	As Soon As f		EEU144,k\$[0.92],k\$c[0.26]
2414	SLIC Motherboard Production	16 w	8/18/99	12/10/99	2412	As Soon As f		
2415	SLICs Received	0 w	12/10/99	12/10/99	2414	As Soon As		
2416	Build Serial Command Link Fanout and Cable Input Con	107.2 w	5/1/98	7/3/00		As Soon As		
2417	Specify Fanout and CIC	21 w	5/1/98	9/29/98	2390	Start No Ear	1.4.4.2.4.2	EEU144[0.3],PhysU144[0.25]
2418	Design/Prototype Fanout and CIC	55.2 w	9/30/98	11/10/99	2417	Start No Ear		EEU144[0.3]
2419	Prototype and design complete	0 w	11/10/99	11/10/99	2410,2418	As Soon As		
2420	Test Fanout and CIC Prototypes	27 w	11/11/99	6/5/00	2419	As Soon As f	1.4.4.2.4.1	EEU144[0.3],k\$[0.2],k\$c[0.06]
2421	Fanout/CIC Production	4 w	6/6/00	7/3/00	2420	As Soon As f	1.4.4.2.4.3	k\$[0.61],k\$c[0.14]
2422	Build Fiber Input Converter	70 w	5/1/98	9/28/99		As Soon As		
2423	Specify Converter	12 w	5/1/98	7/27/98	2390	As Soon As f	1.4.4.2.5.1(0.5)	EEU144[0.3],PhysU144[0.25],k\$[0.12]
2424	Design,Prototype Converter	34 w	7/28/98	4/8/99	2423	As Soon As f	1.4.4.2.5.1(0.5),1.4.4.2.5.2	EEU144[0.3],k\$[0.24]
2425	Converter Production	24 w	4/9/99	9/28/99	2424	As Soon As f	1.4.4.2.5.3	k\$[0.6],k\$c[0.02]
2426	Level 2 Component Specs Complete	0 w	3/18/99	3/18/99	2394,2401,2409,2417,2423	As Soon As		
2427	Build Global Processor System	175.6 w	6/2/97	12/18/00		As Soon As		
2428	Develop Control Software/Prototype System	171 w	7/3/97	12/18/00		As Soon As		
2429	Prepare/Test V1 Download/Script Runner	32.6 w	7/3/97	3/5/98	2385	Start No Ear		PhysU144[0.5]
2430	V1.0 Script Runner in non-VME Prototype	0 w	3/5/98	3/5/98	2429	Start No Ear		
2431	Prepare V1 of Administrative Master Code	35.2 w	6/15/98	3/5/99		Finish No Ear		PhysU144[0.7]
2432	Prepare code for single crate data movement	12 w	10/13/99	1/20/00	2395,2431,2404	As Soon As f	1.4.4.8(.2)	EEU144,k\$[0.12],k\$c[0.02]
2433	Establish single crate data movement	4 w	1/21/00	2/17/00	2432	As Soon As f		EEU144
2434	M3-Establish Single Crate Internal Data Movement	0 w	2/17/00	2/17/00	2433	Start No Ear		
2435	Prepare online build code machine	6 w	5/2/00	6/13/00		Start No Ear		
2436	Establish Communication with L1,L2 FW	4 w	7/3/00	7/31/00	2193,2197,2432,2406	As Soon As f		EEU144
2437	Establish Communication with L3	4 w	7/3/00	7/31/00	2436SS	As Soon As f		PhysU144[0.3]
2438	Prepare V2 Administrative Master Code	10 w	6/14/00	8/23/00	2432,2436FF+3 w,2435	As Soon As f		PhysU144
2439	Prepare V2 of Script Runner	9 w	6/14/00	8/16/00	2430,2379,2435	As Soon As f		PhysU144[0.5]
2440	Prepare V3 Admin Master (multiple workers)	4 w	8/24/00	9/21/00	2462,2438	As Soon As f		PhysU144
2441	Prepare Final Admin Master Code	9 w	9/22/00	11/27/00	2440,2445	As Soon As f	1.4.4.3(0.22)	PhysU144[0.5],k\$[0.12],k\$c[0.02]
2442	Prepare Final Script Runner	9 w	10/13/00	12/18/00	2438,2439,2441FF+3 w	As Soon As f		PhysU144
2443	L2 Operating Code Complete	0 w	12/18/00	12/18/00	2438,2442	As Soon As		
2444	Develop Simulation/Monitoring System	168.8 w	6/2/97	10/27/00		As Soon As		
2445	Specify/Establish Monitoring Data Extraction	24 w	8/2/99	2/2/00	2431	As Soon As f		PhysU144
2446	Prepare Monitoring Display	50 w	10/25/99	10/27/00		Start No Ear		PhysU144
2447	Develop/Simulate Trigger Algorithm	156 w	6/2/97	7/28/00		Start No Ear		PhysU144[0.5]
2448	Preprocessor, Global Timing OK in Hwde	0 w	8/23/00	8/23/00	2447,2610,2438,2439	Start No Ear		
2449	Develop Monitoring Histograms	6 w	1/6/00	2/16/00	2447	As Soon As f		PhysU144
2450	Build/Commission Final System	8 w	7/13/00	9/7/00		As Soon As		
2451	Assemble	4 w	7/13/00	8/9/00	2396,2406	As Soon As f	1.4.4.2.9(0.05)	PhysU144,EEU144,k\$[0.02]
2452	Installation at FNAL	4 w	8/10/00	9/7/00	2195,2451	As Soon As f		PhysU144,ETF144
2453	Global Installation Complete	0 w	9/7/00	9/7/00	2452	Start No Ear		
2454	Build Calorimeter Preprocessors	197.8 w	10/30/96	11/1/00		As Soon As		
2455	Design Calorimeter Processor	96.8 w	10/30/96	10/14/98		As Soon As		
2456	Simulate Time Performance	72.8 w	10/30/96	4/24/98		As Soon As f		PhysU144[0.2]
2457	Define Input, Output	63.8 w	10/30/96	2/20/98	2456SS	As Soon As f		PhysU144[0.1]
2458	Prepare TDR	24 w	4/27/98	10/14/98	2389,2456,2457,2465,2467	As Soon As f		PhysU144[0.3]

ID	Task Name	Duration	Start	Finish	Predecessors	Constraint	WBS	Resource Names
2459	<i>Cal TDR Submitted</i>	0 w	10/14/98	10/14/98	2458	As Soon As		
2460	Build Test Calpp System	38.6 w	8/19/99	6/2/00		As Soon As		
2461	Assemble Test Crate	8.6 w	8/19/99	10/19/99	2395,2404	As Soon As f		PhysU144,EEU144,ETF144
2462	Operate Test Crate	19 w	1/21/00	6/2/00	2432,2461	As Soon As f		PhysU144
2463	<i>Calpp Operation</i>	0 w	6/2/00	6/2/00	2462	As Soon As		
2464	Develop L2Cal Algorithms	126.4 w	10/1/97	4/28/00		As Soon As		
2465	Develop/Simulate Jet Alg.	43 w	12/1/97	10/13/98		Start No Ear		
2466	Develop/Simulate Electron Alg.	80 w	12/1/97	7/19/99		Start No Ear		
2467	Develop/Simulate Missing Et Alg.	51 w	10/1/97	10/12/98		As Soon As f		
2468	Establish Jet Alg. With MonteCarlo	75.2 w	10/14/98	4/28/00	2465	As Soon As f		
2469	Establish Electron Alg. With MonteCarlo	38.2 w	7/20/99	4/28/00	2466	As Soon As f		
2470	Develop Cal Monitoring System	83 w	3/8/99	11/1/00		As Soon As		
2471	Develop Monitoring Histograms	28 w	7/20/99	2/17/00	2465,2466,2467	As Soon As f		PhysU144
2472	Specify/Establish Monitoring Data Extraction	45 w	3/8/99	2/4/00	2431	As Soon As f		PhysU144
2473	Prepare Monitoring Display	24 w	5/15/00	11/1/00	2471,2472	Start No Ear		PhysU144
2474	Build/Commission Final System	8 w	7/13/00	9/7/00		As Soon As		
2475	Assemble	4 w	7/13/00	8/9/00	2396,2406	As Soon As f	1.4.4.2.9(0.05)	PhysU144,EEU144,k\$(0.02]
2476	Installation at FNAL	4 w	8/10/00	9/7/00	2475	As Soon As f		PhysU144,ETF144
2477	<i>L2 Cal Installation Complete</i>	0 w	9/7/00	9/7/00	2476	Start No Ear		
2478	Build Muon Preprocessor	190.6 w	2/1/97	12/5/00		As Soon As		
2479	Design/Build Test System	167.6 w	2/1/97	6/21/00		As Soon As		
2480	Select/Receive Test Card	17 w	2/1/97	6/2/97		As Soon As f	1.4.4.5.2	PhysU144[0.2],k\$(0.2]
2481	Define Inputs	8.6 w	6/3/97	8/1/97	2480	As Soon As f		PhysU144[0.1]
2482	Define Communication	15 w	7/2/98	10/16/98		Start No Ear		PhysU144[0.1]
2483	Define Outputs	4 w	9/29/97	10/24/97	2383	Start No Ear		PhysU144[0.1]
2484	Prepare Muon Processor TDR	97 w	7/2/98	6/21/00	2390	As Soon As f		PhysU144[0.25]
2485	<i>Muon TDR Submitted</i>	0 w	6/21/00	6/21/00	2410,2481,2482,2483,2484,2491	As Soon As		
2486	Design FNAL test crate	4 w	2/1/99	2/26/99	2410,2417,2482	As Soon As f	1.4.4.5.1(0.34),1.4.4.5.3	PhysU144[0.1],EEU144[0.25],k\$(0.06),k\$(0.02]
2487	Operate FNAL Test Crate	9 w	4/3/00	6/5/00	2414,2432,2486	As Soon As f		PhysU144,ETF144[0.25]
2488	Assemble Final System	10 w	7/13/00	9/21/00		As Soon As		
2489	Assemble Central Crate	6 w	7/13/00	8/23/00	2396,2406,2414,2421	As Soon As f	1.4.4.5.1(0.33),1.4.4.2.9(0.60)	PhysU144,EEU144,k\$(0.3),k\$(0.06]
2490	Installation at FNAL	4 w	8/24/00	9/21/00	2421,2489	As Soon As f		PhysU144,ETF144
2491	Assemble Forward Crate	6 w	7/13/00	8/23/00	2489SS	As Soon As f		PhysU144
2492	Installation at FNAL	4 w	8/24/00	9/21/00	2491	As Soon As f	1.4.4.5.1(.33)	PhysU144,ETF144,k\$(0.03),k\$(0.01]
2493	<i>L2 Muon Installation Complete</i>	0 w	9/21/00	9/21/00	2490,2492	As Soon As		
2494	Develop Processor Algorithm	189.4 w	2/3/97	11/27/00		As Soon As		
2495	Draft Version of Central Algorithm	28 w	2/3/97	8/19/97	2480SS	As Soon As f		PhysU144
2496	<i>Receive Evaluation DSP</i>	0 w	1/15/99	1/15/99		Start No Ear		
2497	DSP Code Development	119.4 w	6/1/98	10/26/00		As Soon As		
2498	Complete Central Algorithm on Digital Signal Proc.	81 w	1/15/99	8/28/00	2495	As Soon As f		PhysU144
2499	Draft Forward Algorithm	12 w	6/1/98	8/24/98	2495	As Soon As f		PhysU144
2500	Complete Forward Algorithm	58 w	8/26/99	10/26/00	2496,2499	As Soon As f		PhysU144
2501	Develop DSP management code	21 w	4/3/00	8/29/00		Start No Ear		
2502	<i>DSP Operating Code Complete</i>	0 w	10/26/00	10/26/00	2497	As Soon As		
2503	Develop SLIC monitoring code	12 w	8/31/00	11/27/00	2502FF+4 w	Start No Ear		
2504	Develop Alpha Algorithm (Central)	14 w	6/1/00	9/8/00	2499,2495	Start No Ear		
2505	Assemble Full Algorithm	8 w	9/11/00	11/3/00	2487,2498,2504	As Soon As f		PhysU144
2506	Develop Monitoring Histograms	3 w	9/11/00	9/29/00	2504	As Soon As f		PhysU144
2507	Build Simulator	103.2 w	10/30/98	12/5/00		As Soon As		
2508	Design L1 Muon Simulator	18 w	10/30/98	3/22/99		As Soon As f		
2509	Implement L1 Muon Simulator	36 w	3/23/99	12/6/99	2508,2607	As Soon As f		
2510	Integrate Algorithm in simulator	26 w	6/1/00	12/5/00	2499,2607	Start No Ear		PhysU144
2511	Build CTT Preprocessor	161.6 w	6/1/97	9/7/00		As Soon As		
2512	Design Preprocessor	100.8 w	10/1/97	10/18/99		As Soon As		
2513	Develop and Time Trigger Algorithm	90 w	10/1/97	7/30/99		As Soon As f		PhysU144[0.25]
2514	Establish Specifications	23 w	7/2/98	12/15/98		As Soon As f		PhysU144[0.25],EEU144[0.5]
2515	Establish Crate Content	4 w	12/16/98	1/26/99	2514	As Soon As f		PhysU144[0.5]
2516	<i>Submit CTT TDR</i>	0 w	10/18/99	10/18/99	2513,2515	Start No Ear		
2517	Build Final System	8 w	7/13/00	9/7/00		As Soon As		
2518	Assemble Crate	4 w	7/13/00	8/9/00	2396,2406,2425	As Soon As f	1.4.4.6(0.5),1.4.4.2.9(0.05)	PhysU144[0.5],EEU144[0.5],k\$(0.08),k\$(0.02]
2519	Installation at FNAL	4 w	8/10/00	9/7/00	2518	As Soon As f		PhysU144,ETF144
2520	<i>L2 CTT Installation Complete</i>	0 w	9/7/00	9/7/00	2519	As Soon As		
2521	Build Algorithm/Simulator	150 w	6/1/97	6/15/00		As Soon As		
2522	Develop and simulate algorithm	150 w	6/1/97	6/15/00		As Soon As f		PhysU144[0.2]
2523	Tune algorithm on monte carlo	19.2 w	12/14/99	5/9/00	2522SS+50 %	As Soon As f		PhysU144[0.6]
2524	Build PS Preprocessor	168 w	6/2/97	10/23/00		As Soon As		
2525	Design Preprocessor	100.8 w	10/1/97	10/18/99		As Soon As		
2526	Develop and Time Trigger Algorithm	90 w	10/1/97	7/30/99		As Soon As f		PhysU144[0.25]
2527	Establish Specifications	29.5 w	8/17/98	3/29/99		As Soon As f		EEU144[0.25],PhysU144[0.25]
2528	Establish Crate Content	12 w	3/29/99	6/22/99	2527	As Soon As f		PhysU144[0.5]
2529	<i>Submit PS TDR</i>	0 w	10/18/99	10/18/99	2526,2528	Start No Ear		
2530	Build Final System	8 w	7/13/00	9/7/00		As Soon As		

ID	Task Name	Duration	Start	Finish	Predecessors	Constraint	WBS	Resource Names
2531	Assemble Crate	4 w	7/13/00	8/9/00	2396,2406,2425	As Soon As f	1.4.4.7,1.4.4.2.9(0.25)	PhysU144[0.5],EEU144[0.5],k\$[0.17],k\$[0.03]
2532	Installation at FNAL	4 w	8/10/00	9/7/00	2531	As Soon As f		PhysU144,ETF144
2533	L2 PS Installation Complete	0 w	9/7/00	9/7/00	2532	As Soon As		
2534	Build Algorithm/Simulator	168 w	6/2/97	10/23/00		As Soon As		
2535	Develop and simulate algorithm	148 w	6/2/97	6/1/00		Start No Earl		PhysU144[0.2]
2536	Tune Algorithm on Monte Carlo	20 w	6/2/00	10/23/00	2535	As Soon As f		PhysU144[0.6]
2537	Integrate L2 System	99.2 w	2/6/99	2/2/01		As Soon As		
2538	Level 2 Review	0 w	2/6/99	2/6/99	2390,2410,2459	Start No Ear		
2539	Commission Global/Calpp Combination	4 w	12/19/00	1/19/01	2446,2452,2473,2476,2443,2464	Start No Earl		PhysU144[0.8],EEU144[0.4],ETF144
2540	Commission L2 Muon	6 w	12/19/00	2/2/01	2493,2505,2443,2502	As Soon As f		PhysU144[2],ETF144
2541	Commission L2 with CTT, PS	6 w	12/19/00	2/2/01	2520,2533,2443,2522,2535	As Soon As f		
2542	M3-Trigger Level 2 Commissioned	0 w	2/2/01	2/2/01	2539,2540,2541	As Soon As		
2543	Level 3 Trigger	231.2 w	6/3/96	2/5/01		As Soon As		
2544	Purchase Components	218.2 w	6/3/96	10/27/00		As Soon As		
2545	Upgrade 40 Extended VBD Cards	177 w	6/3/96	1/10/00		Finish No Ea	1.4.5.2.1(0.5)	k\$[0.14]
2546	Upgrade 60 Regular VBD Cards	121 w	7/18/97	1/10/00		Finish No Ea	1.4.5.2.1(0.5)	k\$[0.14]
2547	MPM Daughter Cards (Brown Univ. FY98 MOU)	0.2 w	2/24/98	2/24/98		Start No Earl	1.4.5.4.(21)	k\$[0.48],k\$[0.1]
2548	Purchase Readout Control-FY99	24 w	10/1/99	4/3/00		Start No Earl	1.4.5.4.(79)	k\$[1.81],k\$[0.36]
2549	Purchase High Speed Output	24 w	10/1/99	4/3/00		Start No Earl	1.4.5.2.2,1.4.5.3.2	k\$[0.87],k\$[0.16]
2550	Purchase Commissioning Processors	10 w	10/1/99	12/13/99		Start No Earl	1.4.5.3.3(,5),1.4.5.3.4(,5)	k\$[0.1],k\$[0.02]
2551	Purchase Run II Processors	4 w	10/2/00	10/27/00	2550	Start No Earl	1.4.5.3.1,1.4.5.3.3(,5),1.4.5.3.4(,5)	k\$[2.5],k\$[0.5]
2552	Develop/Install Readout Control	224.2 w	6/3/96	12/12/00		As Soon As		
2553	Data Path Operation with Old System	45.2 w	6/3/96	4/30/97		As Soon As		
2554	With New MCH Position	16 w	6/3/96	9/24/96	2545SS	As Soon As f		PhysU145[0.5]
2555	With Upgraded VME Readout Boards	20 w	12/2/96	4/30/97		Start No Earl		PhysU145[0.5]
2556	Readout Control R&D	178 w	11/15/96	6/29/00		As Soon As		
2557	Initial Design	50 w	11/15/96	11/18/97		Start No Earl	1.4.5.1.(,3)	k\$[0.99],k\$[0.15]
2558	Simulation	124 w	11/15/96	5/27/99	2557SS	As Soon As f		PhysU145[0.5]
2559	Develop First Data Path Prototype(VBD,MPM)	78 w	5/16/97	12/9/98	2557SS+24 w,2572	Finish No Ea		PhysU145[0.5]
2560	First System Test at D0 (VBD,MPM,NT)	14 w	11/19/97	3/11/98	2557	As Soon As f		
2561	M3-Trigger Level 3 System Test Complete	0 w	3/11/98	3/11/98	2560	As Soon As		
2562	Final Design	55 w	3/12/98	4/21/99	2561	As Soon As f	1.4.5.1.(,3)	k\$[0.99],k\$[0.15]
2563	M3-Trigger Level 3 TDR Submitted	0 w	4/21/99	4/21/99	2562	As Soon As		
2564	Design and Construct Hardware Components	59 w	4/22/99	6/29/00	2563	As Soon As f	1.4.5.1.(,4)	k\$[1.32],k\$[0.2]
2565	Develop Second Data Path Prototype	46 w	4/22/99	3/29/00	2559,2563	As Soon As f		PhysU145[0.5]
2566	First Hardware System Test at D0	9 w	3/30/00	6/1/00	2565	As Soon As f		PhysU145[0.5],EEF145[0.1]
2567	Second Hardware Test (one full chain)	4 w	6/2/00	6/29/00	2566	As Soon As f		
2568	M3-L3 Operational (One Full Chain)	0 w	6/29/00	6/29/00	2567	As Soon As		
2569	Install Full System	6 w	10/30/00	12/12/00	2567,2576,2544	As Soon As f		PhysU145[0.5],EEF145[0.5]
2570	Develop Operation Software	181 w	6/3/96	2/7/00		As Soon As		
2571	Support Continuous Data Collection at D0	172 w	6/3/96	11/18/99	2545SS	As Soon As f		PhysU145[0.5]
2572	Establish New Protocol	24 w	6/3/96	11/19/96	2545SS	As Soon As f		PhysU145[0.5]
2573	Develop L3/DAQ Framework	148 w	6/3/96	6/1/99	2545SS	As Soon As f		PhysU145[0.5]
2574	Run Control and Operation	24 w	5/28/99	11/15/99		Start No Earl		
2575	Develop Monitoring/Diagnostic Control	181 w	6/3/96	2/7/00	2545SS	As Soon As f		PhysU145[0.5]
2576	M3-L3 Online Software Complete	0 w	11/18/99	11/18/99	2571,2572,2573,2574	As Soon As		
2577	Level 3 Filtering Software	198.6 w	2/3/97	2/5/01		As Soon As		
2578	Develop L3 Filtering Framework	36 w	6/3/97	2/26/98		Start No Earl		PhysU145[1.25]
2579	Development of L3 Data Base (Constants,Trigger)	64 w	10/2/98	1/31/00		Start No Earl		
2580	Platform Support for Code	102 w	6/1/98	6/23/00		As Soon As		
2581	Initial NT Release Procedures	40 w	6/1/98	3/25/99		Start No Earl		PhysU145[0.4],ETF145
2582	NT Release Procedures Completion	37 w	9/22/99	6/23/00	2581FS+25 w	As Soon As f		
2583	Port Initial Code to NT	4 w	3/26/99	4/22/99	2581	As Soon As f		PhysU145[0.1],ETF145
2584	Geometry/Constant	57 w	5/18/99	7/12/00		As Soon As		
2585	Define Download Method	16 w	5/18/99	9/9/99		Start No Earl		PhysF145,PhysU145
2586	Develop constants for download	41 w	9/10/99	7/12/00	2585	As Soon As f		
2587	Unpacking Issues	143 w	8/18/97	7/13/00		As Soon As		
2588	Unpack Base Classes	129 w	8/18/97	4/4/00		Start No Earl		PhysU145
2589	L2 Inputs Into L3 Defined	0 w	4/4/00	4/4/00	2388,2588	As Soon As		
2590	Develop raw data packer	23 w	1/3/00	6/12/00		Start No Earl		
2591	Availability of MC Raw Data	0 w	6/12/00	6/12/00	2588,2590	Start No Ear		
2592	Implement Subdetector Unpacking	14 w	4/5/00	7/13/00	2578,2588	As Soon As f		PhysU145
2593	Develop Filter Tools	198 w	2/3/97	1/31/01		As Soon As		
2594	Tool Parameter Format	21 w	2/3/97	6/30/97		As Soon As f		PhysU145
2595	Tool Parameter Format Defined	0 w	6/30/97	6/30/97	2594	Start No Ear		
2596	Develop algorithms	79 w	11/18/98	6/30/00	2595	Start No Earl		PhysU145[8]
2597	Implement L3 Algorithms	24 w	7/14/00	1/8/01	2578,2581,2585,2592,2596	As Soon As f		PhysU145[2.5]
2598	Optimize, test, tune parameters	29 w	7/3/00	1/31/01	2596	As Soon As f		PhysU145[2.5]
2599	Provide Executables	83.2 w	6/2/99	2/5/01		As Soon As		
2600	First Downloadable Executable Available	6 w	6/2/99	7/14/99	2573,2578,2583	As Soon As f		PhysU145[1.5]
2601	M3-First Downloadable Executable Available	0 w	7/14/99	7/14/99	2600	As Soon As		
2602	Cosmic Ray Executable Available	12 w	2/1/00	4/24/00	2579,2585,2600	As Soon As f		PhysU145[1.5]

DO Upgrade Schedule
Trigger

ID	Task Name	Duration	Start	Finish	Predecessors	Constraint	WBS	Resource Names
2603	Runtime Executable Available	4 w	1/9/01	2/5/01	2582,2597,2602	As Soon As f		PhysU145[1.5]
2604	L1/L2/L3 Simulator	100 w	10/15/98	10/25/00		As Soon As f		
2605	Development of Trigparse Replacement	46 w	6/1/99	5/5/00		Start No Earl		PhysU145[0.25]
2606	Develop COOR_SIM	23 w	11/10/99	5/4/00	2387	As Soon As f		PhysU145[0.25]
2607	Design Simulation Framework	20 w	10/15/98	3/19/99		Start No Earl		PhysU145
2608	Design and Implement Data Chunks	60 w	10/15/98	1/14/00	2607SS	Start No Earl		PhysU145[2]
2609	Finalize Ntuple, Chunks, and Monte Carlo Inputs	9 w	1/17/00	3/17/00	2607,2608	As Soon As f		PhysU145[2]
2610	First Version Simulation	9 w	1/17/00	3/17/00	2609SS	As Soon As f		PhysU145[2]
2611	Integrate L1 and L2 Simulation Prototypes with I/O	12 w	5/8/00	8/1/00	2605,2606,2609,2610	As Soon As f		PhysU145
2612	Finalize L1 and L2 Simulations	12 w	8/2/00	10/25/00	2611	As Soon As f		PhysU145
2613	Integrate L3 Algorithms	4 w	7/5/00	8/1/00	2611SS+8 w	As Soon As f		PhysU145