

Design Specifications Master Document for the Electronic Mixing Box System

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for the D0 Electronics Group

This short note outlines the general and overall specifications for the Electronics Mixer Box System. The Mixer Box, MB, System is built by the Electronic Systems Engineering Department of the Computing Division at Fermilab. The customer is the Electronics Group of the D0 Detector Department of the Particle Physics Division. The system is installed as part of the D0 Upgrade for Run II.

This document is the master document and takes precedence over all other statements and specifications that may be found in those documents referenced herein.

1 Introduction

The scintillating fibers of the Central Fiber Tracker, CFT, are arranged on the surfaces of eight barrels. These fibers are gathered into ribbons, each of which has two layers of 128 fibers. Each ribbon has a single connector to a clear-fiber light-guide. This light guide transmits the light to its cassette end where it is split into two 128-fiber connectors that plug into the top of a cassette. Each Analog Front End, AFE, board therefore sees signals arranged by order of phi in each of the eight layers.

The trigger requires that the fiber channels be arranged into trigger sectors, which are wedges of all eight layers (nine with the central preshower) in phi. The rearrangement of fiber channels from ribbons to trigger sectors is done by the Mixer Box System.

The ribbons are arranged on the detector into a five-fold symmetry, and each of the five parts is called a Super Sector. The pattern of wave-guide bundles from each Super Sector is identical and the pattern of destination cassettes is identical. Therefore the system design can concentrate on the details within a single Super Sector, and duplicate that design five times for each of the five Super Sectors.

Each beam crossing, or 132ns, 40,960 signal bits must be moved from the AFE boards to the DFE boards. The Mixing Box system is between these sets of boards and must sort the bits from the order out of the AFE boards and into the order needed for the DFE boards. The bit rate for the system is 40,960bits every 132ns, which equals 310 Gigabits per second.

The input signals for each Super Sector of the Mixer Box System are input over 64 individual links. Please see figure 1. The output signals destined for the DFE boards are output over 48 independent links. One third of these output links are fanned out to two outputs making the total number of output links 64.

Each Super Sector is composed of four mixer boards. Please see figure 2. Five groups of four boards reside in a single crate containing the entire system. Each of the four boards within a Super Sector has identical layout and hardware components. Each has 16 input links and 12 independent output links. Four of the output links are fanned out to two links making the total output link count 16. Each of these boards has two connections to a crate back plane. One for sending signals off the board and the other for receiving signals onto the board.

2 Latency, Clock Generation and Clock Distribution

A primary constraint on the Mixer Box System is the latency of the signals within the system. The track lists generated in the DFE boards must be received by the Muon L1 processors within the drift time of the muon PDT's. After a collision, a particle must travel up to a meter before passing through a scintillating fiber where light is generated. This light must propagate to the end of the fiber which can be up to 2.5 meters and then transit the length of a clear fiber wave guide, which can be as long as 11 meters. At the cassette the light is converted into an electrical signal in the VLPC and transmitted to the AFE board. On this board, it is discriminated and the logic signal is transmitted of a high speed link to the Mixer Box. At the mixer box the signals are sorted and sent on to the Digital front-end board. On this board the signals are processed and tracks found, a track list generated and then forwarded on to the muon level 1 system. All of this must be accomplished before the tracks in the muon chambers have drifted to their readout electronics and forwarded to the muon trigger. This entire time is of the order of 800ns. When the signal propagation and latency times for the rest of the system are added up, the mixer box must have a latency of six or fewer 53MHz clock ticks.

A complete set of data for one beam crossing arrives at the mixer box every beam crossing or 132ns. Within this 132ns are 7 ticks of the 53MHz accelerator clock. One seventh of the data arrives on each clock tick. A requirement of the Mixer Box System is, "All the bits which arrive together on the

same clock tick must transit the system together and be transmitted out of the system together on the same but a later clock tick."

As discussed below each board has 16 input links from AFE boards, and a four-board set makes up a Super Sector. Each of the 16 input link receivers per board has a 53MHz clock associated with it. This clock was generated at the sender, the AFE board and propagated over the link. One of these 16 input clocks, on one of the four boards in each super sector set, will be used to generate a super-sector-master-clock, SSMC. This SSMC will then be distributed to all boards in the super sector. On each board, it will be used to clock the various logic devices. For this to work the input links must guarantee an absolute phase difference across the set of 320 links of less than $\pm 3\text{ns}$.

3 Functional Outline of Mixer Board

The Central Fiber Trackers fiber channels are routed from the detector and into VLPC cassettes. The channels for one super sector are routed into a set of 8 cassettes. The relative layout of each of the super sectors is the same. Figure 3 shows a schematic top view of the set of eight cassettes in a super sector in both the top and bottom halves of the figure. The cassettes are numbered 1 through 8. In addition, each cassette contains 8 modules numbered 1 through 8 from front to back. The top half of the figure illustrates how the signals are brought to the top of the cassette. The signals are grouped into 8 connectors that span the width of the cassette. Each connector has 128 signals. The numbers in the figure for each connector indicate the layer, A through H, and the signal numbers. The signal numbers for the group An for example is fibers $(n*64-63)$ through $(n*64)$. From the figure, it is seen that Cassette 1, Module 1 has fiber groups A1 and A2 plugged into its warm end connector. This translates into fiber numbers 1 through 128 for the A-layer.

Two AFE boards are mounted on each cassette and each receives half of the signals. The right-hand-board receives for example A1, A3, A5 and so on, while the left-hand-board receives A2, A4, A6 and so on. The smaller boxes in the lower half of the figure shows the makeup of the high-speed output links from the AFE to the mixer box. The signals in the links are no longer contiguous but are now mixed, one of the links is for example A1 and A3 and another link from the other AFE is A2 and A4. The fiber numbers carried over the A1-A3 link are then 1 through 62 and 129 through 192. This unavoidable mixing must be unmixed in the mixer box. It also has the consequence that more signals must be passed over the back plane between mixer boards.

The five-fold symmetry of the system allowed the problem to be split into 5 equal parts, one for each super sector. There is no smaller complete symmetry. Some of the layers however have smaller symmetries, which can be taken advantage of in the mixer box. Layer E has the most symmetries. This layer does not require any signal sharing across mixing boards and very little sorting within each board. Layer A has half the number of signals as E and has some of its symmetry. Layer A must pass over the back plane only because of the AFE mixing mentioned above. The other layers have symmetries or groupings into pairs of layers. This can be seen from the figure. Layers F and D completely fill

two cassettes, as do the layer pairs; C/G, B/H, and F/D. These layer pairs share a pair of cassettes. These cassettes are filled in reverse order. One of the layers, for example the B layer in the cassette pair 7 and 8, is placed in ascending order from front to back and the other, in this case the H layer is placed in descending order. It should also be noted that in the case of the B/H pair and for the F/D pair there are links with contain data from both layers. These links are highlighted in the figure.

The DFE boards expect the input data over eight links per board. Six of these links are from an adjacent trigger sector pair, trigger sectors N and N+1.¹ The other two are one from the next neighbor sector, N+2, and the previous sector neighbor, N-1. These six links are designated by the colors, green, orange, purple, yellow, blue and red. The first three colors are for trigger sector N and the second three for N+1. The link from the next neighbor, N+2 above, is a second copy of its green link. And the link from the previous neighbor, N-1, is a second copy of its red link.

On each MB board, three sorts must take place. On arrival the data from each input link must be registered with the input link clock and then synchronized to the system clock. Then, for the first sort, the data must be sorted from input board to output board. This sort requires some of the data to be passed from one board to the next via the back plane. After the data arrives on the proper board for output, the second sort arranges the data according to DFE board destination. Finally, the third sort arranges the data into the proper color link for each DFE board.

4 Hardware Description

The Mixer Box system is composed of a single crate with 20 mixer boards in slots 2 through 21 and 1 control board located in slot 1. This is a 6U high by 280mm deep VME style crate with a custom back plane. The crate, crate controller, power supplies and low voltage power supplies are supplied by the D0 Electronics Group. The custom crate back plane and mixer box boards are designed and built by CD/ESE. The schedule, prototype board and total board counts are given in separate documents.² The crate controller board is the same board now under development for use in the DFE crates. The specifications and a prototype board will be given to ESE as soon as they become available.

The crate is located on the D0 detector central platform. It is the bottom crate in rack PC04.

5 Input and Output Specification

The mixer box receives different types of input over its input links. Each link has a link clock and data. The link clocks were discussed above. The data in each link consists of signal bits from the fiber tracker and central preshower and control bits.

5.1 Data Bits

The complete specification of the data bits on each link is contained in a separate set of documents. The official repository of the definition of each bit

over each link for each clock tic for both input and output is a large Excel Workbook.³ The information within this spreadsheet is stored in two forms. Much of the data is stored as entries into spread sheet cells. Other of the data is embedded in the algorithms and detailed coding in the Visual Basic code used by the spreadsheet. This document will be time stamped and stored in file form, in multiple places, with at least one copy available on a public server for all to see and review. The original document and any further revisions must be approved by both groups working on the system.

Another spreadsheet titled, "Mixing Box General Design," contains much of the I/O information, but at the groups-of-bits level, and does not address the time slices for the bits.⁴ This document should be detailed enough for most interested persons, and should be read before reading the above detailed document.

It must be noted that the fiber numbering used in this document and the documents referenced here which further define the MB system use a different fiber (and preshower strip) numbering system than that used by the detector. For the detector the fibers (strips) numbering covers the entire detector. In the MB the numbering is only within a single Super Sector. The numbering convention is in fact a relative numbering within a super sector. A further complication is that Trigger Sector 1, TS1, is in the middle of Supper Sector 1, SS1, which results in a half SS offset between the two systems. Figure 4 gives a partial translation between the two systems.

A major consideration is, "How complete and final is this list of inputs?" Are the inputs and outputs as documented above correct? How much correction of errors must be built into the MB design? What if the I/O is correct but future considerations require a change? What if errors in the rest of the CCT system require that the MB design be changed? There are designed in safety factors in both the input AFE boards and the output DFE boards which greatly reduce the possibility of needing the modify the MB system. In the present design, spare fibers are transferred at the borders of each trigger sector. This provision allows for any as built alignment errors which might require different fibers be transferred near the trigger sector edges. Therefor any measurement errors in the building or installation process will not effect the mixer design. The bits are gathered up on the AFE board into CPLD chips for format before transmission. The AFE board has an inter-CPLD bus that can be used to shift some small number of bits from one link to another. All of the input links on the DFE board are shared between the several processor FPGA chips, which are the computation engines. Some number of bits can be shifted here as well. Finally, the MB system itself will contain several CPLD and FPGA chips. The routing inside these chips is strictly firmware and can be modified non-destructively at any time after production of the system. In summary we can and should consider the design final and build minimal excess capacity into the MB hardware.

The control bits are also specified for the entire CTT system in a separate document.⁵

5.2 Control Bits

The information that needs to be present on the DFE boards is:

No.	Name	Bit Type
-	53MHz Clock	LVDS Link Clock
-	7.6MHz Clock	Line 28 (21)
1	First Period in a Turn Marker	Embedded bit
2	Sync Gap Marker (no L1 Accepts)	Embedded bit
3	Cosmic Gap Marker	Embedded bit
4	BEAM-396	Embedded bit
5	L1 Accept	Embedded bit
6	Diagnostic Mode	Embedded bit
7	Reset	Embedded bit

The first two lines above are considered part of the clock and are discussed in that section. The seven 'embedded bits' are the control bits. A number is assigned to each but for use in defining the bit locations in reference 3 and other documents. Each of these bits changes value at most once each 132ns crossing. Therefore each bit can be encoded within one time slice on one line for each crossing.

A given MB board will in general receive its sixteen LVDS links from several source boards. Thus, the possibility exists that a single board will receive non-identical sets of command bits. Each board will create a local embedded command bit by performing an OR of this command bit over the entire set of input links. This set of local embedded command bits will be used to control its mode of operation. This set will also be transmitted on its output links. It will in addition, generate a set of 'embedded command status bits' for each embedded command bit. Each status bit is created by performing an XOR of the command bit over the entire set of inputs for that bit. It will also create a 'summary embedded command status bit' by forming an OR of all the status bits.

Fifteen of the input links carry 128 bits of data in a total of 140 bit buckets. That leaves 12 buckets available for the 7 control bits. The location of these 7 bits on each input line is defined in reference 3, with the following restriction. Each control bit must arrive on each of the input links in the same time slice. The control bits are removed from the 'input link data stream' at the front end of the board. They are routed to a central place and the 'output set of control and status bits' are formed. These output bits are then routed to the back of the board and feed into the logic forming the BLUE and ORANGE links. Each of these links has 136 bit buckets out of 189 filled with data. The output bits locations on these links is also defined within reference 3. The status and control bits into each DFE mother board must reside in the three least significant bit positions of the ORANGE and BLUE links.⁶

The Diagnostic Mode control bit above is introduced on the AFE boards. The CTT system is designed with a wide range of diagnostic capabilities. The slow monitoring and control system is used to broadcast to all the hardware the detailed diagnostic setup to use at all points in the system. The AFE boards are

then instructed to generate the Diagnostic Mode bit at the appropriate times. As each element in the system receives this bit, it acts accordingly. However, the Diagnostic Mode bit is always ignored unless the Cosmic gap Marker is TRUE. This ensures that the overall control over the mode of the system originates within the Trigger Framework. The response of the MB to the diagnostic mode command is undefined at this time.

6 Figures

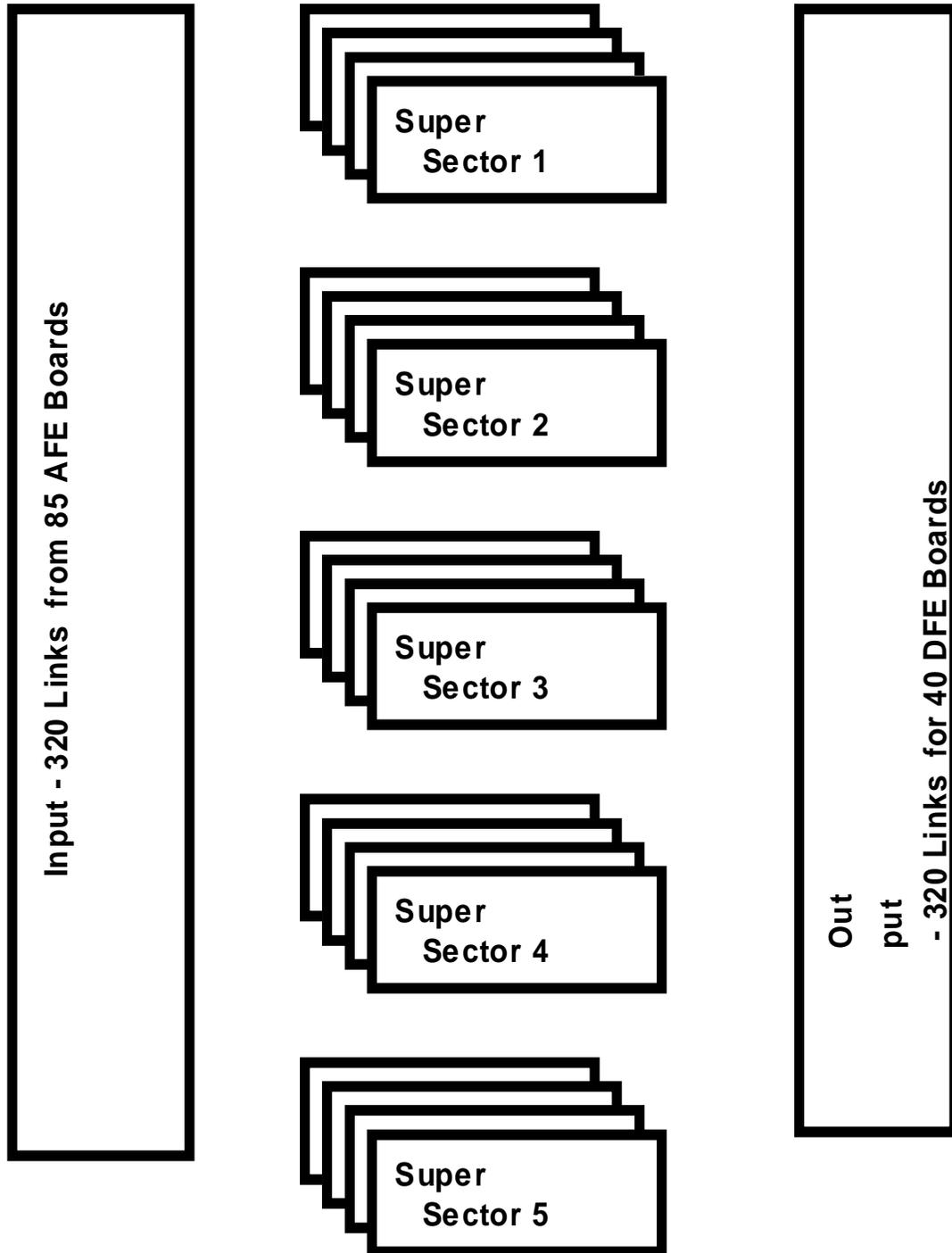


Figure 1 - Diagram of the Mixer Box System, showing the five Super Sectors, each with four boards, and the input and output links.

one Super Sector- 4 Boards

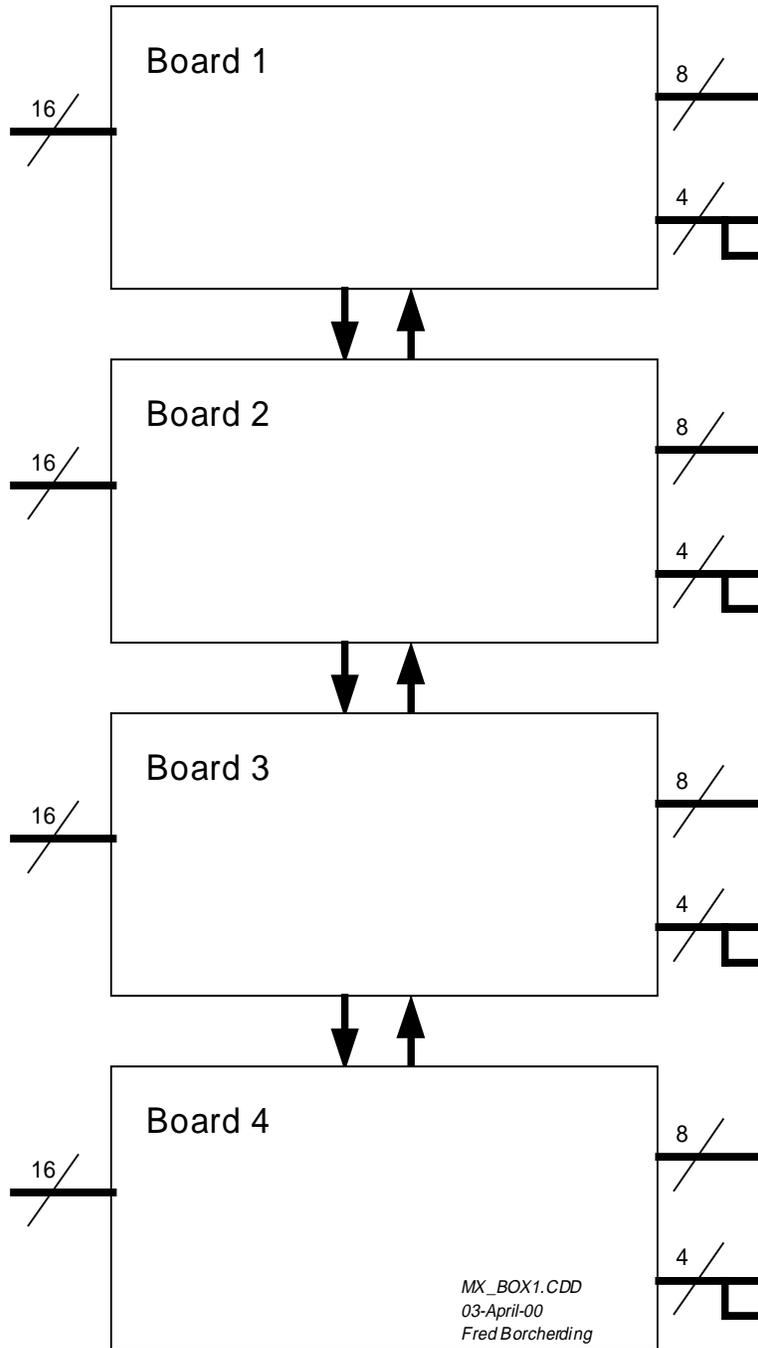
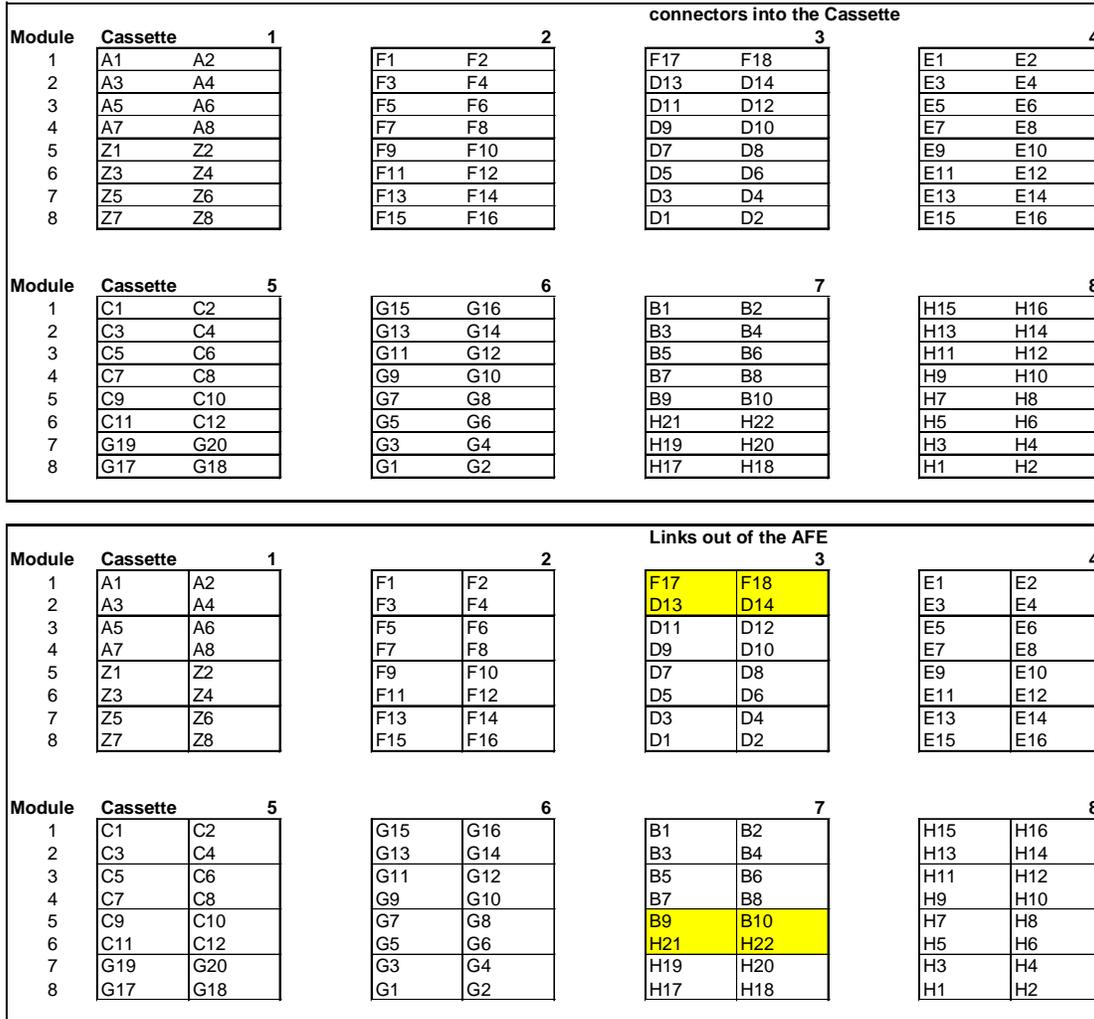


Figure 2 - Diagram of 1/5th of the Mixer Box System or one Super Sector. Each Super sector is composed of four mixer boards. Each board has 16 input links and 16 output links.



NOTE: Each link has 64 channels
 for example A1 is layer A, channels 1 through 64
 Mn is Layer M, channels [64(n-1)+1] through 64n]

Figure 3 - Schematic of the arrangement of fibers into the top of the eight Cassettes within a Super Sector. In the top half the fiber cable connectors are represented by the smaller boxes, in the bottom half the digital links out of the AFE boards are represented by the smaller boxes. Each symbol represents a group of 64 channels. [Copied from "Mixing Boards xxxx.xls", which is the source document.]

TS #									
SS #	Min	Max							
1	73	8							
2	9	24							
3	25	40							
4	41	56							
5	57	72							

Fiber #									
	Layer A		Layer B		Layer C		Layer D		
SS #	Min	Max	Min	Max	Min	Max	Min	Max	
1	2305	256	2881	320	3457	384	4033	448	
2	257	768	321	960	385	1152	449	1344	
3	769	1280	961	1600	1153	1920	1345	2240	
4	1281	1792	1601	2240	1921	2688	2241	3136	
5	1793	2304	2241	2880	2689	3456	3137	4032	
MB #	1	512	1	640	1	768	1	896	

Fiber #									
	Layer E		Layer F		Layer G		Layer H		
SS #	Min	Max	Min	Max	Min	Max	Min	Max	
1	4609	512	5185	576	5761	640	6337	704	
2	513	1536	577	1728	641	1920	705	2112	
3	1537	2560	1729	2880	1921	3200	2113	3520	
4	2561	3584	2881	4032	3201	4480	3521	4928	
5	3585	4608	4033	5184	4481	5760	4929	6336	
MB #	1	1024	1	1152	1	1280	1	1408	

Figure 4 - Tables giving the translation of fiber numbers between detector numbers and MB numbers. The top table shows the boundary TS within each SS. The two bottom tables show the correspondence between the two fiber numberings. For each layer the detector number for the first and last fiber within each SS is given, in the first 5 rows. In the bottom row is given the first and last MB fiber numbering for that layer.

¹ Reference to JO DFE board inputs, "990105a.doc", ...

² Reference to Schedule showing prototype numbers.

³ Reference to big mother spread sheet

⁴ Reference to FB's MB spread sheet "Mixing Box General Design"

⁵ "Control Signals for the SMT Electronics and the CTT Electronics Systems", Fred Borcharding Personal Note of May 5, 2000.

⁶ "Including Framing, Status and Control bits in the LVDS links to the DFE", Jamieson T. Olsen, Personal Engineering Note No. 20000209a of February 9, 2000.