REV.	DESCRIPTION	DRAWN	DATE
		APPD.	DATE
B.	REDUCED CIRCUIT WIDTH IN WARM INTERCEPT REGION, CREATED STAGGERED BIAS VIA ARRAY, INCREASED SIGNAL TRACE PITCH MID-CIRCUIT.	M. MATULIK	05/01/98
C.	RESTORED WARM INTERCEPT REGION WIDTH, INCREASED POWER TAIL WIDTH.	M. MATULIK	01/13/99
D.	INCREASED LENGTH BY 0.250 INCHES FOR BACKSIDE BIAS CONTACT POSITIONING	M. MATULIK	02/11/99
E.	REDUCED LENGTH BY 0.100, REDIMENSIONED DRAWING.	M. MATULIK	05/28/99

J2:01, PS03 J2:02, PS04 J2:03, PS02 J2:04, PS01

J2:05, PS06 J2:06, PS05 J2:07, PS07 J2:08, PS08

J1:03, PS02
J1:07, PS06
J1:11, CH13
J1:15, CH17
J1:19, CH24
J1:23, BIAS
J1:27, CH25
J1:31, CH32
J1:35, CH36
J1:39, CH41
J1:43, CH48

J1:01, CAL01
J1:05, PS04
J1:09, PS08
J1:13, CH12
J1:17, CH16
J1:21, CH21
J1:25, CH28
J1:29, CH33
J1:33, CH37
J1:37, CH44
J1:41, BIAS

J1:02, CAL01
J1:06, PS03
J1:10, PS07
J1:14, CH11
J1:18, CH18
J1:22, CH23
J1:26, CH27
J1:30, CH34
J1:34, BIAS
J1:38, CH35
J1:42, CH42

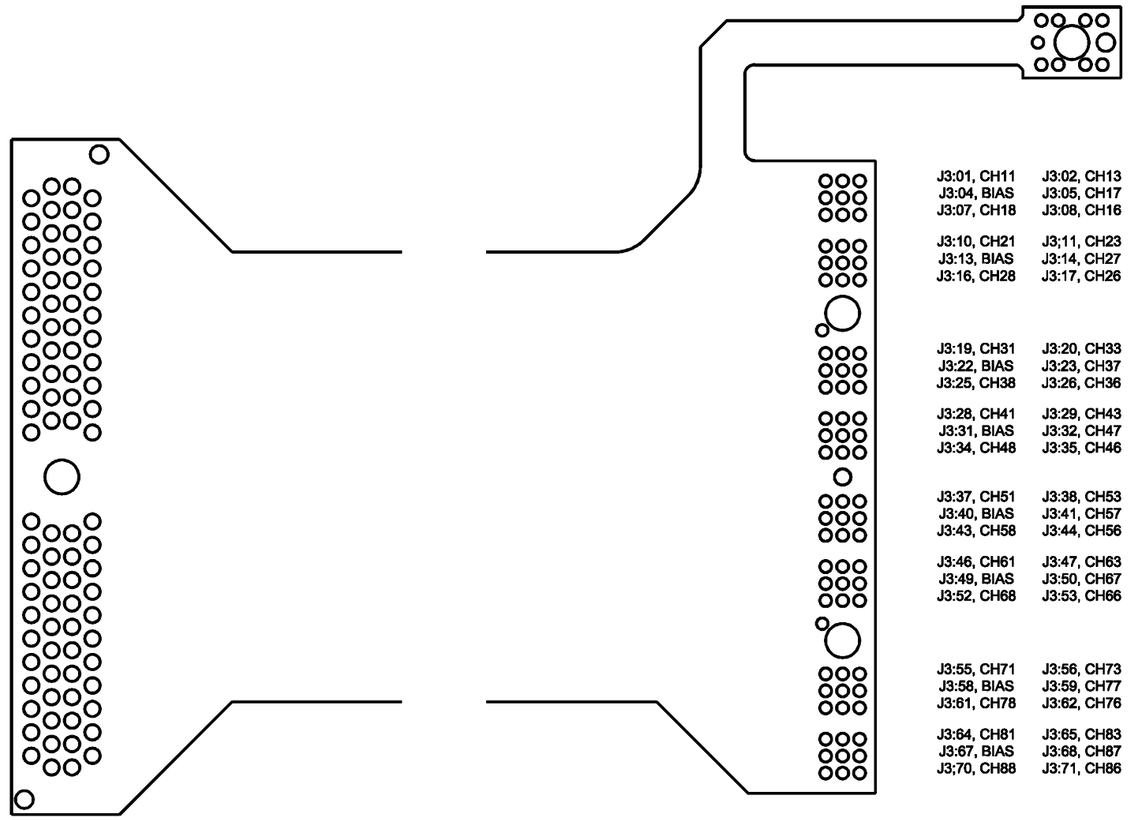
J1:04, PS01
J1:08, PS05
J1:12, CH14
J1:16, BIAS
J1:20, CH15
J1:24, CH22
J1:28, CH26
J1:32, CH31
J1:36, CH38
J1:40, CH43
J1:44, CH47

J1:45, CH46
J1:49, CH51
J1:53, CH58
J1:57, CH63
J1:61, CH67
J1:65, CH74
J1:69, BIAS
J1:73, CH75
J1:77, CH82
J1:81, CH86
J1:85

J1:47, CH54
J1:51, BIAS
J1:55, CH55
J1:59, CH62
J1:63, CH66
J1:67, CH71
J1:71, CH78
J1:75, CH83
J1:79, CH87
J1:83
J1:87. CAL02

J1:48, CH53
J1:52, CH57
J1:56, CH64
J1:60, BIAS
J1:64, CH65
J1:68, CH72
J1:72, CH76
J1:76, CH81
J1:80, CH88
J1:84
J1:88, CAL02

J1:46, CH45
J1:50, CH52
J1:54, CH56
J1:58, CH61
J1:62, CH68
J1:66, CH73
J1:70, CH77
J1:74, CH84
J1:78, BIAS
J1:82, CH85
J1:86



J3:01, CH11 J3:02, CH13 J3:03, CH14
J3:04, BIAS J3:05, CH17 J3:06, CH12
J3:07, CH18 J3:08, CH16 J3:09, CH15

J3:10, CH21 J3;11, CH23 J3:12, CH24
J3:13, BIAS J3:14, CH27 J3:15, CH22
J3:16, CH28 J3:17, CH26 J3:18, CH25

J3:19, CH31 J3:20, CH33 J3:21, CH34
J3:22, BIAS J3:23, CH37 J3:24, CH32
J3:25, CH38 J3:26, CH36 J3:27, CH35

J3:28, CH41 J3:29, CH43 J3:30, CH44
J3:31, BIAS J3:32, CH47 J3:33, CH42
J3:34, CH48 J3:35, CH46 J3:36, CH45

J3:37, CH51 J3:38, CH53 J3:39, CH54
J3:40, BIAS J3:41, CH57 J3:42, CH52
J3:43, CH58 J3:44, CH56 J3:45, CH55

J3:46, CH61 J3:47, CH63 J3:48, CH64
J3:49, BIAS J3:50, CH67 J3:51, CH62
J3:52, CH68 J3:53, CH66 J3:54, CH65

J3:55, CH71 J3:56, CH73 J3:57, CH74
J3:58, BIAS J3:59, CH77 J3:60, CH72
J3:61, CH78 J3:62, CH76 J3:63, CH75

J3:64, CH81 J3:65, CH83 J3:66, CH84
J3:67, BIAS J3:68, CH87 J3:69, CH82
J3;70, CH88 J3:71, CH86 J3:72, CH85

D:\PROJECT\VLPC\V64_J

ITEM	PART NUMBER	DESCRIPTION OR SIZE	QTY

PARTS LIST

UNLESS OTHERWISE SPEC.				
		ORIGINATOR	M. Matulik	01/03/97
		DRAWN BY	M. Matulik	01/03/97
		CHECKED BY		
		APPROVED BY		
		USED ON -		
		MATERIAL -		

FERMI NATIONAL ACCELERATOR LABORATORY
UNITED STATES DEPARTMENT OF ENERGY

VLPC 64 Channel Readout Cable

Model J
Right Hand
Connector Pad Identification

SCALE	FILMED	DRAWING NUMBER	Sheet 3 of 4	REV.
		3823.113-MB-330202		E